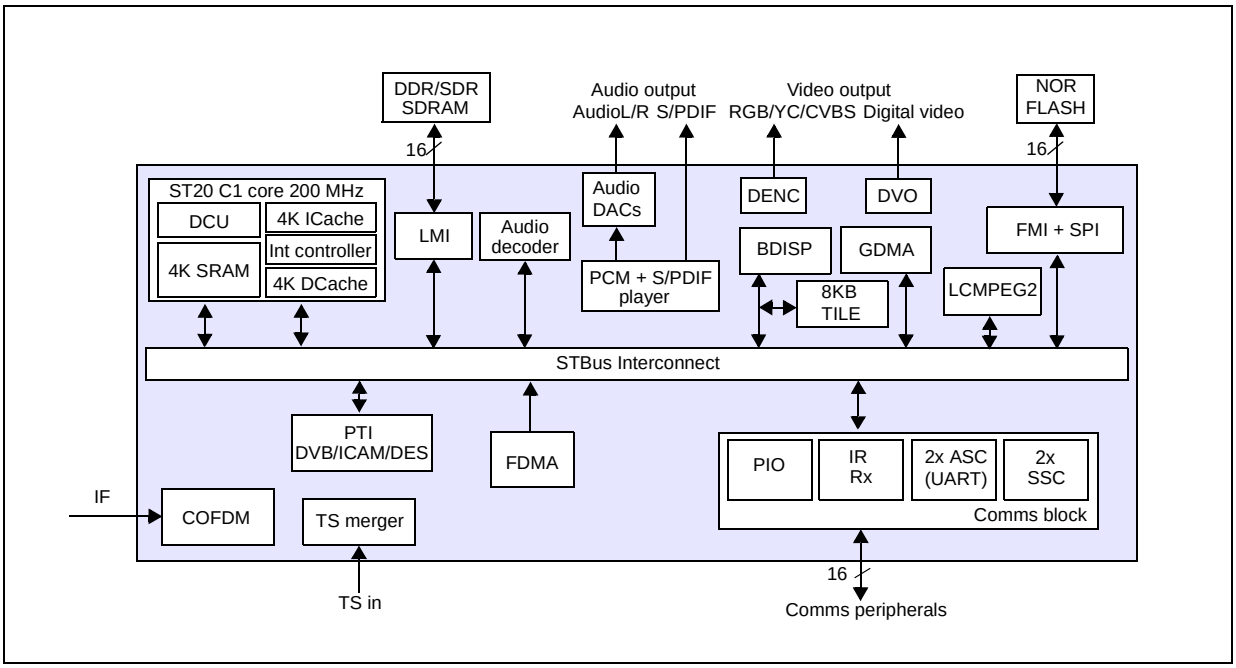
STi5167

Low-cost interactive set-top box with advanced features

Data Brief

Features

- Enhanced ST20 32-bit VL-RISC CPU
- Unified memory interface
  - up to 133 MHz, 16-bit wide SDR SDRAM,
  - up to 166 MHz, 16-bit wide DDR SDRAM
- Programmable Flash memory interface
- Demodulator compatible with I and Q or IF inputs for tuner interface
- Channel management
- Digital carrier, timing & symbol recovery loops
- Decoding
  - QPSK - 16 QAM - 64 QAM constellations
- MPEG-2 MP@ML video decoder
- Graphics and display
  - 3 display planes
  - 2D paced blitter engine with fill function
- Programmable transport interface (PTI)
  - single transport stream input for DVB
- Central DMA controller
- Advanced security ready
  - compatible with latest CA requirement
- PAL/NTSC/SECAM encoder
  - RGB, CVBS, Y/C and YUV outputs with four 10-bit DAC outputs.
- Audio subsystem
  - simultaneous MPEG audio decode and output of Dolby streams on S/PDIF
  - IEC958/IEC1937 digital audio output interface
  - integrated stereo audio DAC
- On-chip peripherals
  - ASC (UART) with Tx and Rx FIFOs
  - 3 banks of 8-bit programmable I/O
  - integrated VCXO
- JTAG/TAP interface
- Package
  - 15 mm x 15mm PBGA 240 0.8 mm pitch



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1 Description

1.1 General

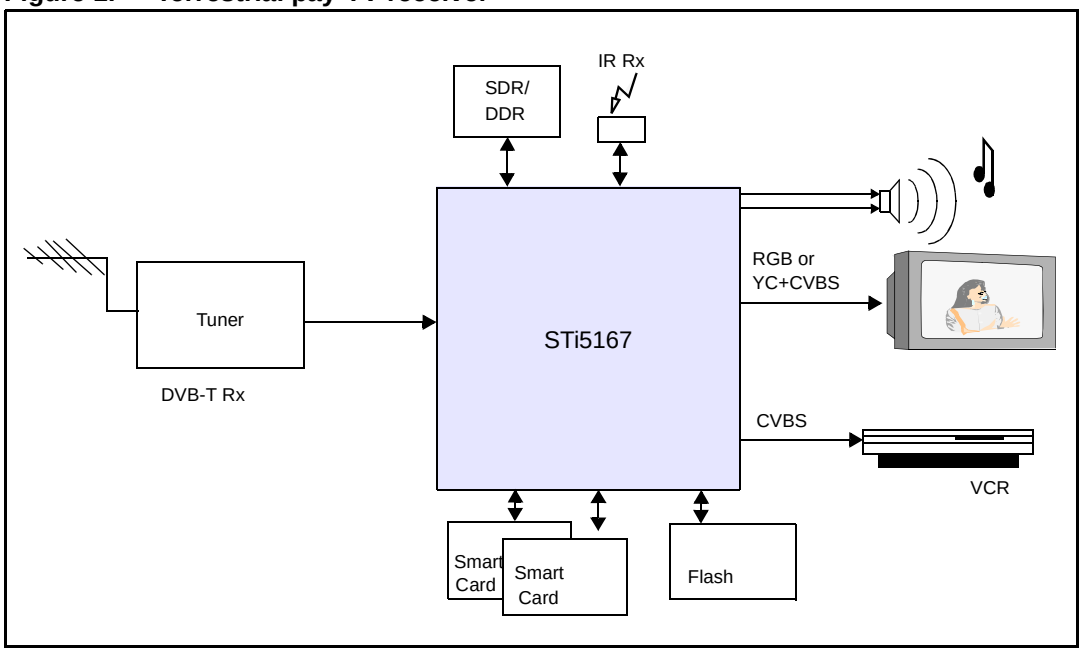
The STi5167 is the latest in the family of STBus set-top box ICs providing high-performance, low-cost system-on-chip (SoC) for MPEG processing in digital terrestrial STBs. It is derived from the STi5107, with the addition of a DVB-T COFDM demodulator and supports multiple platforms using a unified architecture. STi5167 is compatible with the latest CA advanced security specifications.

The STi5167 delivers enhanced performance with respect to previous devices. Main memory is based upon a single 16-bit external SDR or DDR SDRAM.

The display architecture of the devices is based upon a high performance blitter engine that supports CLUT8 and RGB16STi5167 formats for background, video and OSD/graphics displays. It makes the porting of middleware easier with improved rendering.

1.2 Application

Figure 1. Terrestrial pay-TV receiver



The STi5167 is designed for CA applications with embedded HW security.

Its BGA package allows the use of a simple 2-layer PCB, with all signals and power supplies being routed through the top PCB layer. This leaves the bottom PCB layer dedicated to the ground plane and JTAG connections.

To reduce the system pin complexity, the following conditions apply:

- either SDR and DDR SDRAM memory interface available
- serial or parallel Flash interfaces for program storage (HW selection for serial or parallel Flash boot)
- FMI interface with NAND Flash support
- serial TS input port
- two UARTs
- two smart card interfaces
- HW security support option
- digital video output port (exclusive with other features)

1.3 Main features

- Enhanced ST20 32-bit VL-RISC CPU
  - 200 MHz, single cycle cache, 4 Kbyte instruction cache, 4 Kbyte data cache, 4 Kbyte SRAM
- Local memory interface
  - up to 133 MHz, 16-bit wide SDR SDRAM,
  - up to 166 MHz, 16-bit wide DDR SDRAM
- Programmable Flash memory interface
  - 3 separately configurable banks, 8/16-bits wide
  - SRAM, peripheral, Flash, SFlash™ support
- Demodulator compatible with I and Q or IF inputs for tuner interface
  - wide range carrier tracking loop for offset recovery
  - dual analog to digital conversion
  - signal strength indicator dedicated ADC
  - dual $\Sigma\Delta$ digital split AGC for RF and BB
- Channel management
  - NorDig Unified Specification (v1.0.2) capable
  - dynamic fading compatible
  - channel reception quality indicator
  - out of guard interval echo synchronization
  - impulsive noise rejection capable
  - flexible fully-integrated digital channel filter with outstanding adjacent channel rejection capability
- Digital carrier, timing & symbol recovery loops
- Decoding
  - 2 K, 4 K, 8 K FFT length
  - 5, 6, 7 and 8 MHz channel bandwidth
  - 1/4, 1/8, 1/16, 1/32 guard interval length
  - QPSK - 16 QAM - 64 QAM constellations
  - hierarchical capability
  - Viterbi soft decoder rate 1/2
  - supports puncture rates 1/2, 2/3, 3/4, 5/6, 7/8
  - Reed-Solomon decoder
  - energy dispersal descrambler
- Programmable transport interface (PTI)
  - single transport stream input
  - support for DVB transport streams
  - integrated DVB, ICAM descramblers
- MPEG-2 MP@ML video decoder
  - fully programmable horizontal and vertical SRCs

- Graphics and display
  - three display planes
  - 8 bpp CLUT graphics, 256 x 30 bits (AYCbCr) CLUT entries. 16 bpp true color graphics, RGB565, ARGB1555, ARGB4444 formats. Link-list control
  - alpha blending, anti-aliasing, anti-flutter, anti-flicker filters
  - 2D paced blitter engine with fill function
  - blitter based display compositor
  - digital video output: compliant with CCIR 656
- PAL/NTSC/SECAM encoder
  - RGB, CVBS, Y/C and YUV outputs with four 10-bit DAC outputs. RGB/CVBS or YUV/CVBS or YC/CVBS
  - encoding of CGMS closed caption, Teletext, WSS and VPS
- Audio subsystem
  - MPEG-1 layers I/II
  - simultaneous MPEG audio decode and output of Dolby streams on S/PDIF
  - IEC958/IEC1937 digital audio output interface
  - integrated stereo audio DAC system
- NAND Flash support for basic timeshift and instant replay
- Central DMA controller
- On-chip peripherals
  - two ASCs (UARTs) with Tx and Rx FIFOs
  - three banks of 8-bit parallel I/O
  - two smartcard interfaces and clock generator
  - SPI for serial Flash support
  - two SSCs for I^2C/SPI master/slave interfaces
  - infrared receiver
  - integrated VCXO
  - low-power/RTC/watchdog controller
  - flexible clock generation to operate with 27 MHz or 30 MHz external reference
  - GP ADC for key control
- Advanced security ready
  - compatible with latest CA requirement
- JTAG/TAP interface
- Package
  - 15 mm x 15 mm PBGA 240 0.8 mm pitch.

2 Ordering information

Table 1. Ordering information

Order code	Packaging
STi5167KBB	15 mm x 15 mm PBGA 240 0.8 mm pitch
STi5167ZBB	15 mm x 15 mm PBGA 240 0.8 mm pitch

3 Revision history

Table 2. Document revision history

Date	Revision	Changes
05-March-2009	1	Initial release
01-Apr-2009	2	Memory interface values updated.
10-Apr-2009	3	Memory interface (SDR SDRAM) new update.

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