



STHV748

5-level, ± 90 V, 2 A high-speed pulser with four independent channels

Preliminary data

Features

- High-density ultrasound transmitter
- 0 to ± 90 V output voltage
- Up to 20 MHz operating frequency
- Low-power, high-voltage drivers
- 2 independently supplied half bridges for each channel in pulse wave (PW) mode
 - 5-level output waveform
 - ± 2 A source and sink current
 - Down to 20 ps jitter
 - Anti-cross conduction function
 - Low 2nd harmonic distortion
 - Fine-tuning on propagation delay
- Fully integrated clamping-to-ground function
 - 6 Ω synchronous active clamp
 - Anti-leakage on output node
- Dedicated half bridge for continuous wave (CW) mode on each
 - Down to 0.1 W power consumption
 - ± 0.6 A source and sink current
 - Down to 10 ps jitter
- Fully integrated HV receiver switch
 - 13.5 Ω on resistance
 - HV MOS topology to minimize current consumption
 - Up to 300 MHz BW
- 2.4 V to 3.6 V CMOS logic interface
- Auxiliary integrated circuits
 - Noise blocking diodes
 - Fully self-biasing architecture
 - Anti-memory effect for all internal HV nodes
 - Thermal protection
 - Stand by function
- Latch-up free due to HV SOI technology
- Very few external passive components needed



Applications

- Medical ultrasound imaging
- Pulse waveform generator
- NDT ultrasound transmission
- Piezoelectric transducers driver

Description

This monolithic, high-voltage, high-speed pulser generator features four independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive or MEMS transducers. The device comprises a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes and high-power P-channel and N-channel MOSFETs as output stage for each channel, clamping-to-ground circuitry, anti-leakage, anti-memory effect block, thermal sensor and HV receiver switch (HVR_SW) which guarantees a strong decoupling during transmission phase. Moreover the STHV748 includes self biasing and thermal shutdown blocks (see [Figure 1](#)).

Each channel can support up to five active output levels with two half bridges. The output stage of each channel is able to provide ± 2 A peak output current. In order to reduce power dissipation during continuous wave mode, the peak current is limited to 0.6 A (a dedicated half bridge is used).

Table 1. Device summary

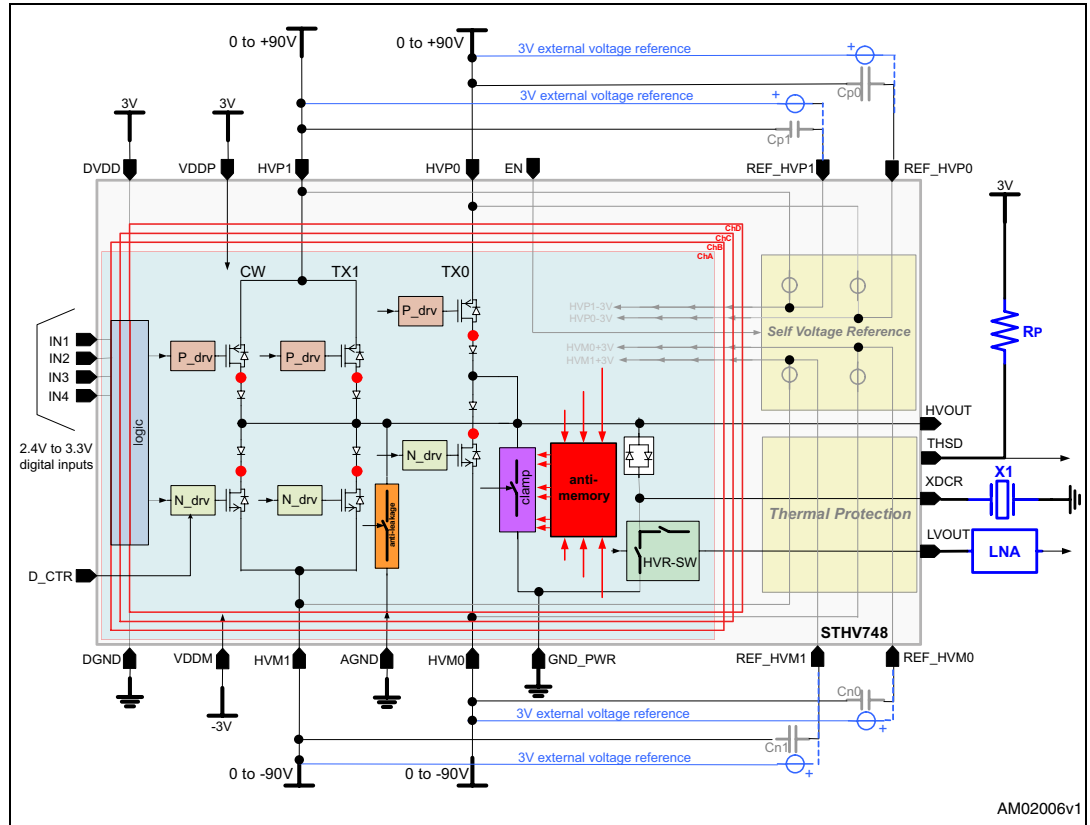
| Order code | Package | Packaging |
|------------|---------|---------------|
| STHV748QTR | QFN64 | Tape and reel |

Contents

- 1 Typical application circuit 3**
- 2 Pin settings 4**
 - 2.1 Connection 4
 - 2.2 Description 4
 - 2.3 Additional pin description 6
- 3 Truth table and single channel block description 7**
- 4 Typical supply reference setting 8**
- 5 Electrical data 9**
 - 5.1 Absolute maximum ratings 9
- 6 Operating supply voltages and average currents 10**
 - 6.1 Digital inputs 11
 - 6.2 Output signals 11
- 7 Electrical characteristics 12**
- 8 Timings 15**
- 9 Package mechanical data 18**
- 10 Revision history 21**

1 Typical application circuit

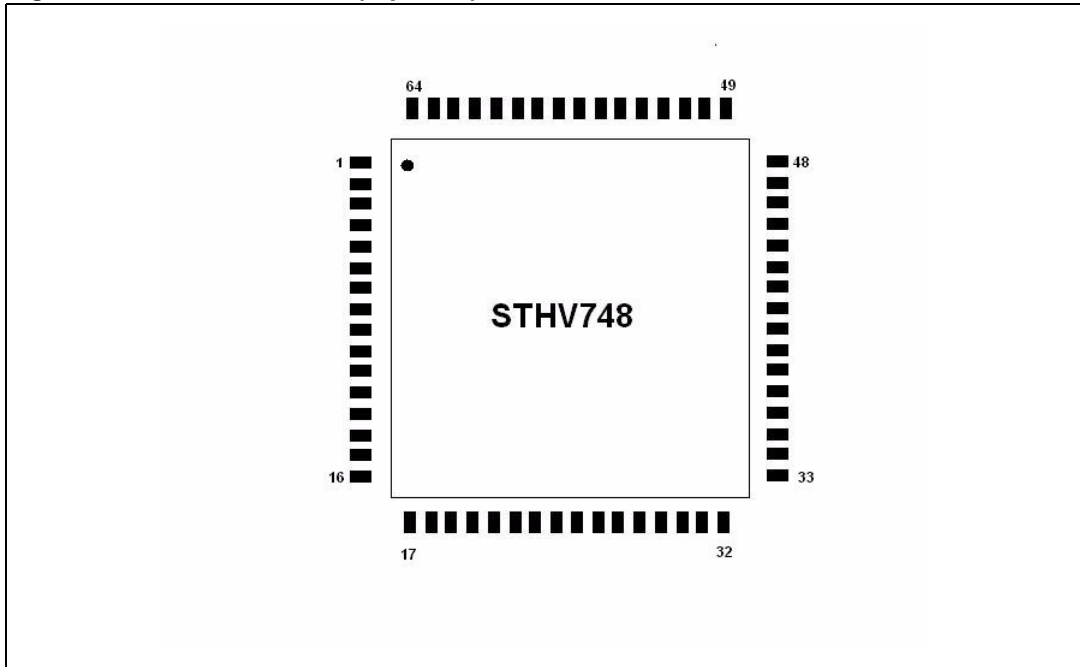
Figure 1. Typical application circuit



2 Pin settings

2.1 Connection

Figure 2. Pin connection (top view)



Note: 0.25 mm X 100 V maximum voltage between abutted pins

2.2 Description

Table 2. Pin description (P = power, A = analog, D = digital)

| Pin N | Name | Function | IN/OUT | Type |
|-------|----------|---|--------|------|
| 1 | AGND | Signal ground | I | A |
| 2 | REF_HVM1 | Supply for low side 1 gate driver | I | P |
| 3 | HVM1_A | Negative high-voltage supply 1 channel A | I | P |
| 4 | HVM0_A | Negative high-voltage supply 0 channel A | I | P |
| 5 | HVOUT_A | Channel A, high-voltage output before noise blocking diodes | O | P |
| 6 | HVP0_A | Positive high-voltage supply 0 channel A | I | P |
| 7 | REF_HVP1 | Supply for high side 1 gate driver | I | P |
| 8 | HVP1_A | Positive high-voltage supply 1 channel A | I | P |
| 9 | HVP1_B | Positive high-voltage supply 1 channel B | I | P |
| 10 | REF_HVP0 | Supply for high side 0 gate driver | I | P |
| 11 | HVP0_B | Positive high-voltage supply 0 channel B | I | P |

Table 2. Pin description (P = power, A = analog, D = digital) (continued)

| Pin N | Name | Function | IN/OUT | Type |
|-------|----------|---|--------|------|
| 12 | HVOUT_B | Channel B, high-voltage output before noise blocking diodes | O | P |
| 13 | HVM0_B | Negative high-voltage supply 0 channel B | I | P |
| 14 | HVM1_B | Negative high-voltage supply 1 channel B | I | P |
| 15 | REF_HVM0 | Supply for low side 0 gate driver | I | P |
| 16 | D_CTR | Delay control | I | A |
| 17 | IN4 | Input signal shared | I | D |
| 18 | IN1_B | Input signal channel B | I | D |
| 19 | IN2_B | Input signal channel B | I | D |
| 20 | IN3_B | Input signal channel B | I | D |
| 21 | VDDP | Positive low-voltage supply | I | A |
| 22 | GND_PWR | Power ground | I | P |
| 23 | XDCR_B | Channel B, high-voltage output | O | P |
| 24 | LVOUT_B | Channel B, low-voltage output | O | A |
| 25 | LVOUT_C | Channel C, low-voltage output | O | A |
| 26 | XDCR_C | Channel C, high-voltage output | O | P |
| 27 | GND_PWR | Power ground | I | P |
| 28 | VDDM | Negative low-voltage supply | I | A |
| 29 | IN3_C | Input signal channel C | I | D |
| 30 | IN2_C | Input signal channel C | I | D |
| 31 | IN1_C | Input signal channel C | I | D |
| 32 | THSD | Thermal shutdown pin | I/O | D |
| 33 | AGND | Signal ground | I | A |
| 34 | REF_HVM1 | Supply for low side 1 gate driver | I | P |
| 35 | HVM1_C | Negative high-voltage supply 1 channel C | I | P |
| 36 | HVM0_C | Negative high-voltage supply 0 channel C | I | P |
| 37 | HVOUT_C | Channel C, high-voltage output before noise blocking diodes | O | P |
| 38 | HVP0_C | Positive high-voltage supply 0 channel C | I | P |
| 39 | REF_HVP1 | Supply for high side 1 gate driver | I | P |
| 40 | HVP1_C | Positive high-voltage supply 1 channel C | I | P |
| 41 | HVP1_D | Positive high-voltage supply 1 channel D | I | P |
| 42 | REF_HVP0 | Supply for high side 0 gate driver | I | P |
| 43 | HVP0_D | Positive high-voltage supply 0 channel D | I | P |
| 44 | HVOUT_D | Channel D, high-voltage output before noise blocking diodes | O | P |

Table 2. Pin description (P = power, A = analog, D = digital) (continued)

| Pin N | Name | Function | IN/OUT | Type |
|-------|-------------|--|--------|------|
| 45 | HVM0_D | Negative high-voltage supply 0 channel D | I | P |
| 46 | HVM1_D | Negative high-voltage supply 1 channel D | I | P |
| 47 | REF_HVM0 | Supply for low side 0 gate driver | I | P |
| 48 | DGND | Logic ground | I | A |
| 49 | DVDD | Positive logic supply | I | A |
| 50 | IN1_D | Input signal channel D | I | D |
| 51 | IN2_D | Input signal channel D | I | D |
| 52 | IN3_D | Input signal channel D | I | D |
| 53 | VDDP | Positive low-voltage supply | I | A |
| 54 | GND_PWR | Power ground | I | P |
| 55 | XDCR_D | Channel D, high-voltage output | O | P |
| 56 | LVOUT_D | Channel D, low-voltage output | O | A |
| 57 | LVOUT_A | Channel A, low-voltage output | O | A |
| 58 | XDCR_A | Channel A, high-voltage output | O | P |
| 59 | GND_PWR | Power ground | I | P |
| 60 | VDDM | Negative low-voltage supply | I | A |
| 61 | IN3_A | Input signal channel A | I | D |
| 62 | IN2_A | Input signal channel A | I | D |
| 63 | IN1_A | Input signal channel A | I | D |
| 64 | EN | Enable internal supply generators | I | D |
| | Exposed-Pad | Substrate | I | P |

2.3 Additional pin description

EN allows minimizing the power consumption. If EN=0, the self voltage reference is not supplied. Supplying reference externally the total power consumption is reduced.

THSD is a thermal flag. The output stage of THSD pin is a Nch-MOS open-drain, so this necessary to connect external pull-up resistance ($R_p \geq 10 \text{ k}\Omega$) to positive low-voltage supply (see [Figure 1](#)). If the internal temperature overtakes 160 °C, THSD goes down and put all the channels in HZ state. Externally forcing THSD to positive low-voltage supply, the thermal protection will be disabled.

D_CTR can be used to optimize 2nd HD performances by tuning the fall propagation delay (tdf - see table 9). If D_CTR is equal to ground tdf has the nominal value. If D_CTR is being varied from 2 V to 4.2 V tdf can be changed from -1ns to +600 ps respect to the nominal value.

EXPOSED-PAD is internally connected to the substrate. It can be floating or connected to a 100 V capacitance toward ground in order to reduce noise during the receiving phase.

3 Truth table and single channel block description

Figure 3. Single channel block description

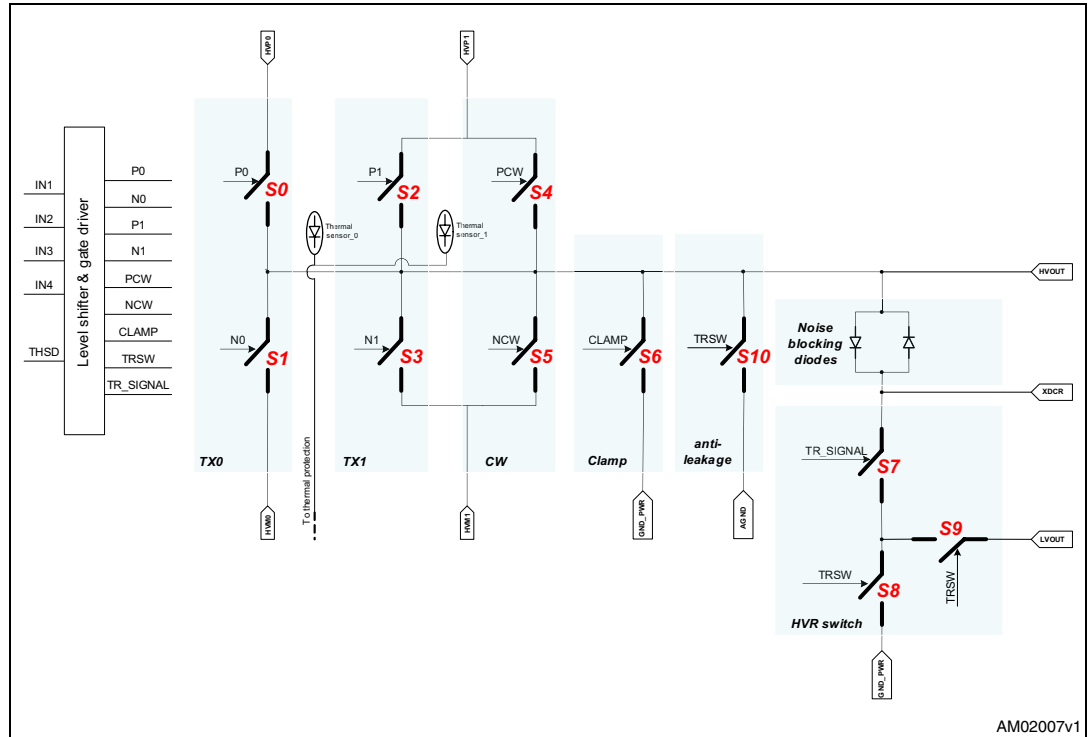


Table 3. Truth table for one channel

| Global | | Per channel | | | State | Switches internal state | | | | | | | | | |
|--------|-----|-------------|-----|-----|-------------------|-------------------------|----|----|----|----|----|----|----|----|----|
| THSD | IN4 | IN3 | IN2 | IN1 | | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
| 1 | x | x | 0 | 0 | Clamp | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | HVM0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | HVP0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | x | 0 | 1 | 1 | HVR_SW | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | HVP1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | HZ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | HVR_SW | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | Max HVM0 and HVM1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | Max HVP0 and HVP1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | CW HVM1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | CW HVP1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | x | x | x | x | HZ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

4 Typical supply reference setting

Table 4. Typical supply reference setting

| Symbol | External supply mode | Self supply mode |
|----------|----------------------------------|----------------------|
| EN | 0 | 1 |
| Cp0, Cp1 | Not used | 47 nF ⁽¹⁾ |
| Cn0, Cn1 | Not used | 9 nF ⁽¹⁾ |
| REF_HVP# | Has to be connected to HVP# -3 V | Not used |
| REF_HVM# | Has to be connected to HVM# +3 V | Not used |

1. In Self supply mode 30 μs after EN edge to charge external capacitance are needed.

5 Electrical data

5.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------|--|----------------------------|------|
| AGND | Analog ground reference ⁽¹⁾ | 0 | V |
| DGND | Digital ground | -300 to 300 | mV |
| GND_PWR | Power ground | -1.2 to 1.2 | V |
| VDDP | Positive supply voltage | -0.3 to 3.9 | V |
| VDDM | Negative supply voltage | 0.3 to -3.9 | V |
| DVDD | Positive logic voltage | -0.3 to 3.9 | V |
| HVP0 | TX0 high-voltage positive supply | 0 to 95 | V |
| HVP1 | TX1 high-voltage positive supply | ≤ HVP0 | V |
| HVM0 | TX0 high-voltage negative supply | 0 to -95 | V |
| HVM1 | TX1 high-voltage negative supply | ≥ HVM0 | V |
| REF_HVP# | High-voltage positive gate supply | -0.3 < HVP - REF_HVP < 3.3 | V |
| REF_HVM# | High-voltage negative gate supply | -0.3 < REF_HVM - HVM < 3.3 | V |
| XDCR | High-voltage output | -95 to 95 | V |
| HVOUT | High-voltage output before noise blocking diodes | -95 to 95 | V |
| LVOUT | Low-voltage output | -1 to 1 | V |
| DIG I/O | Digital input specified in tab 1 | -0.3 to DVDD + 0.3 | V |
| D_CTR | Delay control | -0.3 to 4.6 | V |
| T _{OP} | Operating temperature range | -40 to 125 | °C |
| T _{STG} | Storage temperature range | -65 to 150 | °C |

1. AGND is considered like "ground reference" for all fallen voltages.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 6.

| Symbol | Parameter | Value | Unit |
|--------------------|---------------------------------|-------------------|------|
| R _{th,JA} | Thermal resistance junction-amb | 30 ⁽¹⁾ | °C/W |

1. This value is given for a two layer PCB (252P) and it's strongly sensitive to PCB layout. Increasing the number of PCB layer or adding heat singer vias this number degree (reduce)

6 Operating supply voltages and average currents (a)

Table 7. Supply voltages

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|-----------------------------------|------------------------------|------|-----|-------------------|-------|
| VDDP | Positive supply voltage | | 2.7 | 3 | 3.6 | V |
| I _{VDDP} | Positive supply current | PW mode ⁽¹⁾ | | | 3 | mA |
| I _{VDDP_Q} | | Stand-by mode ⁽²⁾ | | | 1 | µA |
| VDDM | Negative supply voltage | | -2.7 | -3 | -3.6 | V |
| I _{VDDM} | Negative supply current | PW mode | | | 2 | mA |
| I _{VDDM_Q} | | Stand-by mode | | | 1 | µA |
| DVDD | Positive logic voltage | | 2.4 | 3 | min(3.6,VDDP+0.3) | V |
| I _{DVD} | Logic supply current | PW mode | | | 10 | µA |
| I _{DVD_Q} | | Stand-by mode | 55 | 65 | 80 | µA |
| HVP | High-voltage positive supply | | 0 | | 90 | V |
| I _{HVP} | HV positive supply current | PW mode | | | 50 | mA |
| I _{HVP_Q} | | Stand-by mode | | | 1 | µA |
| HVM | High-voltage negative supply | | -90 | | 0 | V |
| I _{HVM} | HV negative supply current | PW mode | | | 45 | mA |
| I _{HVM_Q} | | Stand-by mode | | | 1 | µA |
| HVP-REF_HVP | High-voltage positive gate supply | | 2.7 | 3 | 3.3 | V |
| I _{REF_HVP} | HV positive REF current | PW mode | | | 7 | mA |
| I _{REF_HVP_Q} | | Stand-by mode | 200 | 300 | 400 | µA |
| REF_HVM-HVM | High-voltage negative gate supply | | 2.7 | 3 | 3.3 | V |
| I _{REF_HVM} | HV negative REF current | PW mode | | | 3 | mA |
| I _{REF_HVM_Q} | | Stand-by mode | 200 | 300 | 400 | µA |
| AGND | Ground reference | | | 0 | | V |
| I _{AGND} | Analog ground current | PW mode | | | 700 | µA |
| I _{AGND_Q} | | Stand-by mode | | | 1 | µA |
| GND_PWR | Power ground reference | | | 0 | | V |
| I _{GND_PWR} | PWR ground current | PC mode ⁽³⁾ | | | 20 | mA |
| I _{GND_PWR_Q} | | Stand-by mode | | | 1 | µA |
| D_CTR | Delay control | | 0 | | 4.2 | V |

1. In PW pulse wave mode the average current is measured over 5 periods (see Figure 5)
2. In Stand-by mode all channels are in HZ.
3. In PC pulse cancellation mode the average current is measured over 1 period (see Figure 6)

a. Operation conditions, unless otherwise specified, only A channel on, no load, HV=90V, TX0 and TX1 on, EN=0.

6.1 Digital inputs

Table 8. Digital inputs

| Symbol | Parameter | Min. | Max. | Units |
|------------------------------------|--------------------------|---------|---------|-------|
| IN1_#, IN2_#, IN3_#, IN4, EN, THSD | Input logic high-voltage | 0.8DVDD | DVDD | V |
| IN1_#, IN2_#, IN3_#, IN4, EN, THSD | Input logic low-voltage | 0 | 0.2DVDD | V |

6.2 Output signals

Table 9. Output signals

| Symbol | Parameter | Min. | Max. | Units |
|--------|--|------|------|-------|
| HVOUT | High-voltage output before noise blocking diodes | -90 | 90 | V |
| XDCR | High-voltage output | -90 | 90 | V |
| LVOUT | Low-voltage output | -1 | 1 | V |
| THSD | Thermal shutdown pin | 0 | 3 | V |

7 Electrical characteristics

Table 10. Static electrical characteristics ⁽¹⁾

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------|---|---|---------|------|---------|--------------|
| I_N | Saturation current S1 – S3 | HVP# =10V, HVM# =-10V, HVOUT=0V | 1.18 | 1.28 | 1.40 | A |
| | | HVP# =25V, HVM# =-25V, HVOUT=0V | | 1.70 | | A |
| I_P | Saturation current S0 – S2 | HVP# =10V, HVM# =-10V, HVOUT=0V | 1.12 | 1.26 | 1.42 | A |
| | | HVP# =25V, HVM# =-25V, HVOUT=0V | | 1.70 | | A |
| I_{NCW} | Saturation current S5 | HVP1=10V, HVM1=-10V, HVOUT=0V | 315 | 350 | 400 | mA |
| I_{PCW} | Saturation current S4 | HVP1=10V, HVM1=-10V, HVOUT=0V | 415 | 480 | 575 | mA |
| I_{CL} | Positive saturation current S6 (Pch) | HVOUT=10V | 1.25 | 1.54 | 2 | A |
| | | HVOUT=25V | | TBD | | A |
| | Negative saturation current S6 (Nch) | HVOUT=10V | 1.32 | 1.59 | 2 | |
| | | HVOUT=25V | | TBD | | |
| I_L | Output leakage current, per channel | HVP# = 90V, HVM# = -90V, HVOUT=0V | | | 1 | μ A |
| P_{SB} | Power dissipation in stand by mode | HVP# = 90V, HVM# = -90V, HVOUT=0V, EN=0 | | 4 | 4.5 | μ W |
| | | HVP# = 90V, HVM# = -90V, HVOUT=0V | | 126 | 150 | mW |
| P_{RX} | Power dissipation in HVR_SW state | HVP# = 90V, HVM# = -90V, EN=0, all channels in receiving phase | 25 | 30 | 40 | mW |
| V_{REFP} | HVP# - REF_HVP# | HVP# = 90V, HVM# = -90V, HVOUT=0V | 0.8VDDP | | 1.2VDDP | V |
| V_{REFN} | REF_HVM# - HVM# | HVP# = 90V, HVM# = -90V, HVOUT=0V | 0.8VDDP | | 1.2VDDP | V |
| T_{OTP} | Over temperature threshold | HVP# =10V, HVM# =-10V | 130 | 145 | 160 | $^{\circ}$ C |
| T_{HYS} | OTP Hysteresis | HVP# =10V, HVM# =-10V | | 40 | | $^{\circ}$ C |
| C_{HVR_SW} | HVR_SW capacitance | LVOUT=0V | | 40 | | pF |
| $R_{HVR_SW_ON}$ | R_{HVR_SW} on resistance | HVP# =10V, HVM# =-10V, XDCCR=1V, LVOUT=0V | 11.5 | 13.5 | 15.5 | Ω |
| $R_{HVR_SW_OFF}$ | R_{HVR_SW} off resistance | HVP# =10V, HVM# =-10V, XDCCR=1V, LVOUT=0V | 1 | | | G Ω |

Table 10. Static electrical characteristics ⁽¹⁾ (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------------|------------------------------------|---|------|------|------|-------|
| V _{DROP_CW} | Voltage drop between HVP1 and XDCR | HVP# = 10V, HVM# = -10V, I _{SINK_XDCR} = 50mA | 2.62 | 2.79 | 2.96 | V |
| | Voltage drop between XDCR and HVM1 | HVP# = 10V, HVM# = -10V, I _{SOURCE_XDCR} = 50mA | 2.69 | 2.86 | 3.03 | V |

1. Operating conditions, unless otherwise specified, EN = 1, HVP# = 90 V, HVM# = -90 V, VDDP = 3 V, VDDM = -3 V, DVDD = 3 V, T_{ROOM} = 25 °C.

Table 11. AC electrical characteristics (1)

| Symbol | Parameter | Test condition | Min | Typ | Max | Units |
|-------------------------|-------------------------------------|--|-----|-----|-----|------------------|
| f | Maximum output frequency | | 16 | | | MHz |
| | | 50pF//200Ω | | 22 | | MHz |
| f _{CW} | Maximum output frequency CW | HVP1 =5V, HVM1 = -5V, continuous wave mode | 20 | | | MHz |
| f _{BW} | Output frequency BW | HVP1 = 50V, HVM1 = -50V, continuous wave mode, 50pF//200Ω | | 10 | | MHz |
| t _j | Output jitter | | | 20 | | ps, rms |
| t _{j-CW} | CW output jitter | HVP1 =10V, HVM1 = -10V, continuous wave mode | | 5 | | ps, rms |
| t _f | Fall time | | | 28 | 31 | ns |
| t _r | Rise time | | | 28 | 31 | ns |
| t _{dr} | Rise propagation delay | | | 24 | 27 | ns |
| t _{df} | Fall propagation delay | | | 24 | 27 | ns |
| t _{HVR_SW} | HVR_SW turn-on / turn-off time | | | 170 | | ns |
| HD2 | 2 nd harmonic distortion | 1 pulse f = 1.7MHz | | -40 | | dBc |
| | | 1 pulse f = 5MHz | -60 | | -40 | dBc |
| | | 5 pulses f = 1.7MHz | | -40 | | dBc |
| | | 5 pulses f = 5MHz | -60 | | -40 | dBc |
| HD2PC | Pulse cancellation | f = 1.7MHz original and inverted pulse | | -40 | | dBc |
| | | f = 5MHz original and inverted pulse | -60 | | -40 | dBc |
| BVD | Burst voltage drop | 1 st to 128 th pulse HVP1 = 10V, HVM1 = -10V | | 2 | | % |
| P _{D-CW} | Power dissipation, per channel | CW mode, f = 5MHz, HVP1 = 5V, HVM1 = -5V, no load | | | 70 | mW |
| HVR_SW _{SPIKE} | HVR_SW spike on XDRCR and LVOUT | | | 100 | | mV _{pp} |
| X _{TALK} | Cross talk between channels. | Ampl(2ch)/Ampl(1ch), 50pF//200Ω | | -40 | | db |

1. Operating conditions, unless otherwise specified, HVP# = 90V, HVM# = -90V, VDDP = 3V, VDDM = -3V, DVDD = 3V, EN = 0, (HVP-REF_HVP) = 3V, (REF_HVM-HVM) = 3V, XDRCR load C = 300pF//R = 100Ω, LVOUT load C = 20pF//200Ω, T_{ROOM} = 25 °C.

8 Timings

Figure 4. t_r , t_f , t_{dr} and t_{df} descriptions

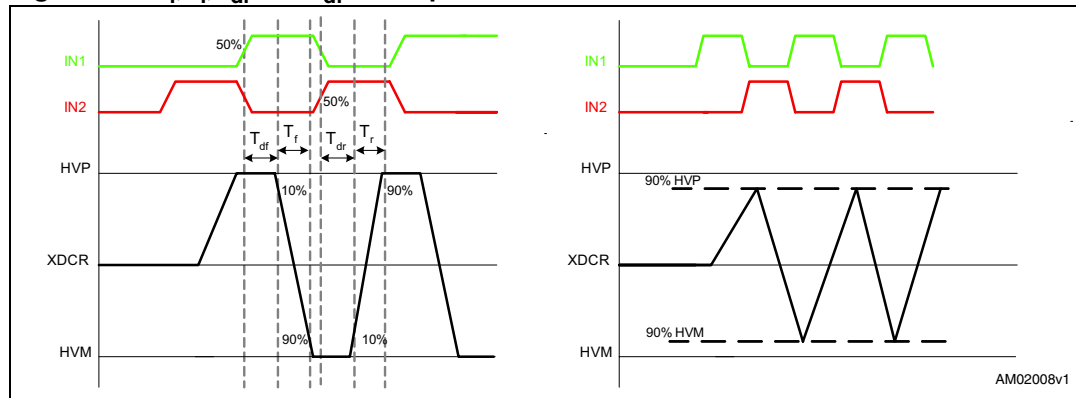


Figure 5. PW example 5 periods, HVP0 = 90 V HVM0 = -90 V, T=200 ns, T_{tx} =1.2 μ s

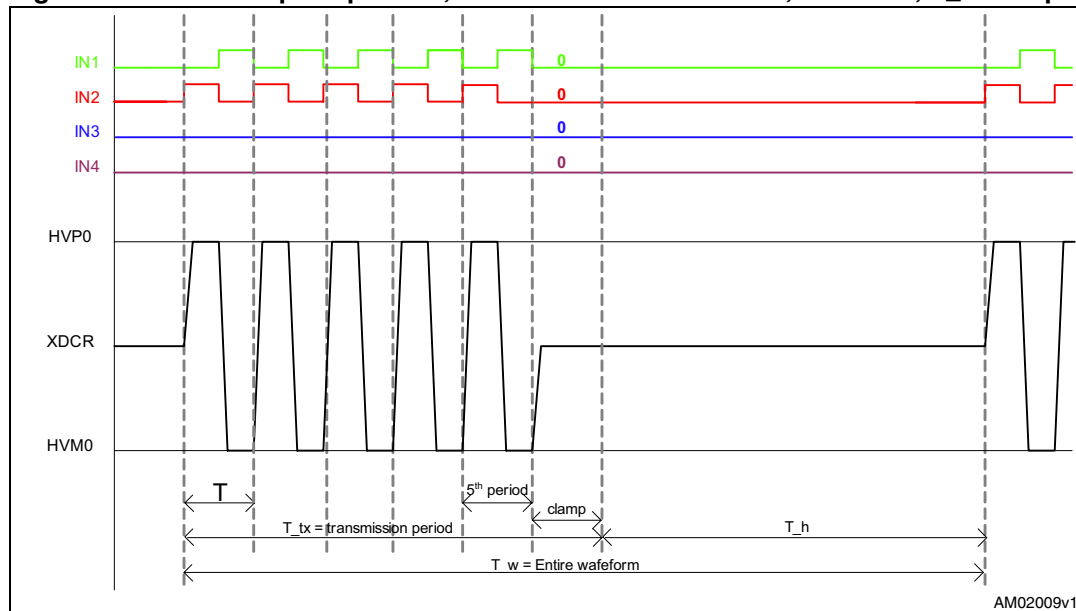


Figure 6. PW and HD2 example (HVP0=80V, HVM0=-80 V load 300 pF/100 Ω)

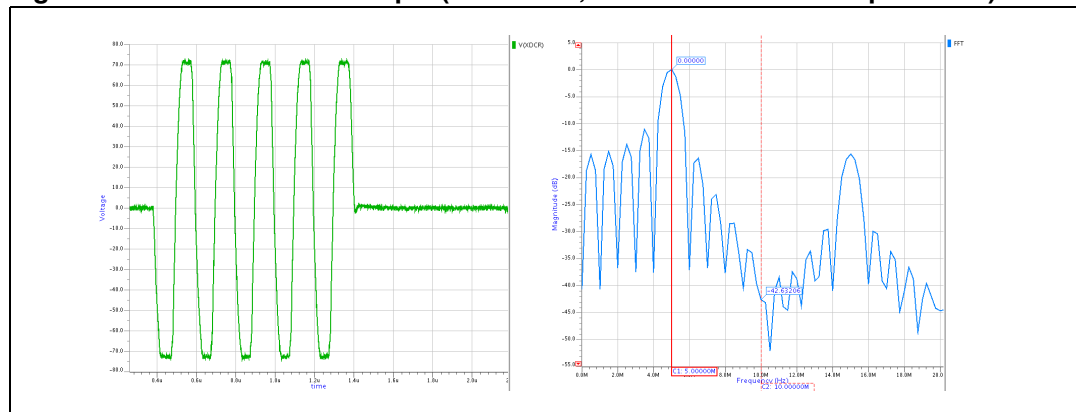
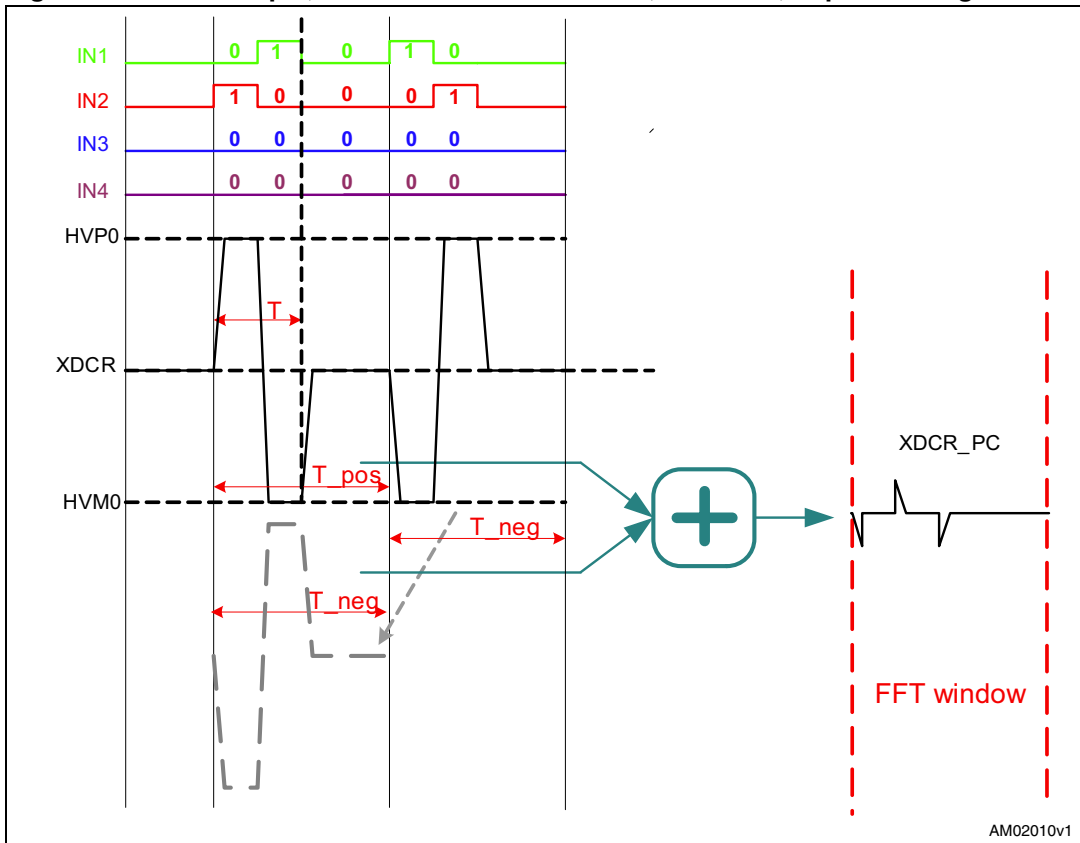


Figure 7. PC example, HVP0 = 90 V HVM0 = -90 V, T=200 ns, T_pos= T_neg=400 ns



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Figure 8. PC and HD2 example (HVP0=60 V, HVM0=-60 V load 300 pF//100 Ω)

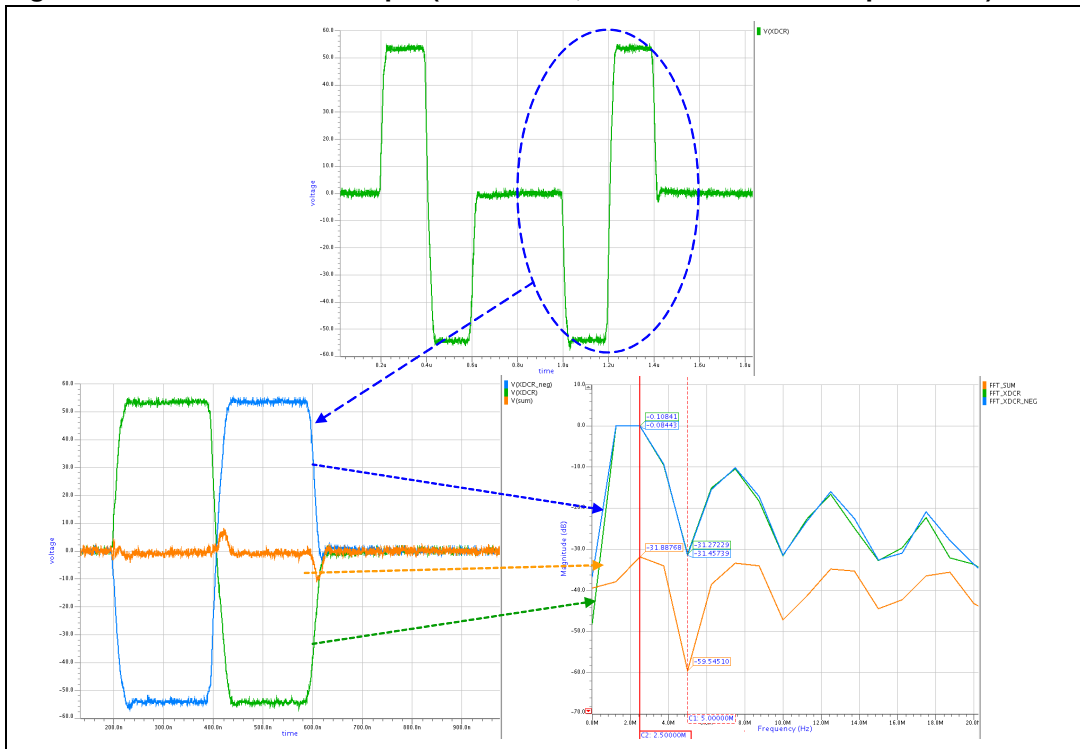


Figure 9. CW mode example, HVP1 = 5 V, HVM1 = 5 V, T = 200 ns, T_tx > 1 ms

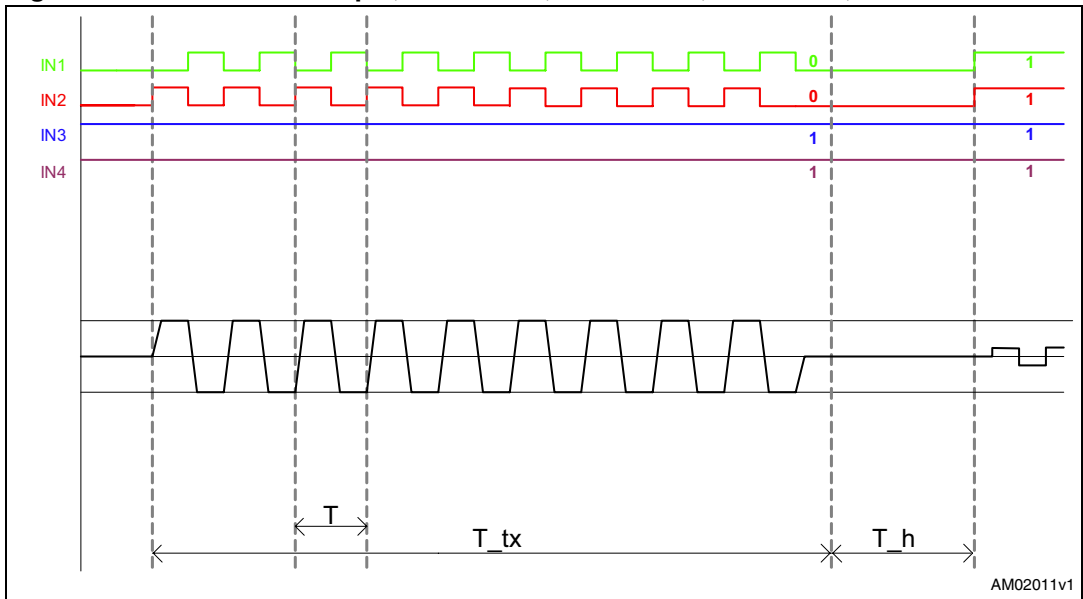
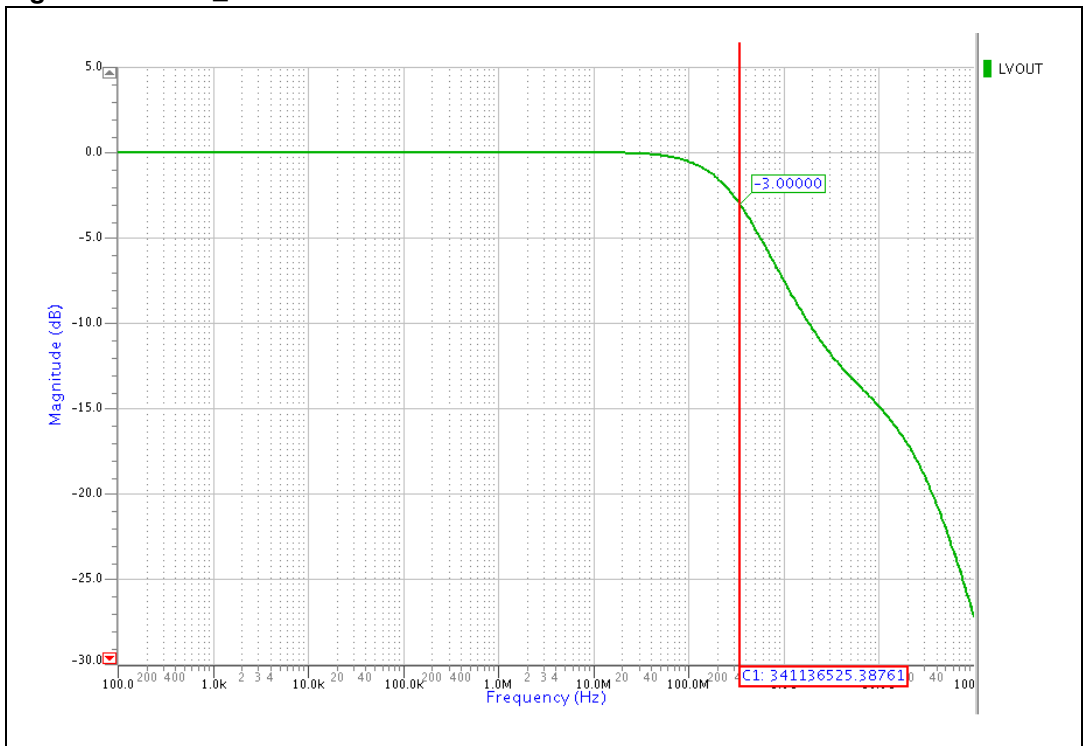


Figure 10. HVR_SW bandwidth



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 12. QFN64 9 x 9 x 1.0 mm 64 pitch 0.50 mechanical data

| Dim | Min. | Typ. | Max. |
|-----|---------------------------|------|------|
| A | 0.8 | 0.9 | 1 |
| A1 | | 0.02 | 0.05 |
| A2 | | 0.65 | 1 |
| A3 | | 0.2 | |
| b | 0.18 | 0.25 | 0.3 |
| D | 8.85 | 9 | 9.15 |
| D1 | | 8.75 | |
| D2 | See exposed pad variation | | |
| E | 8.85 | 9 | 9.15 |
| E1 | | 8.75 | |
| E2 | See exposed pad variation | | |
| e | | 0.5 | |
| L | 0.35 | 0.4 | 0.45 |
| P | | | 0.6 |
| K | | | 12 |
| ddd | | | 0.08 |

Table 13. Exposed-pad variation

| Variation | D2 | | | E2 | | |
|-----------|------|------|------|------|------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 4.1 | 4.25 | 4.4 | 4.1 | 4.25 | 4.4 |
| B | 4.55 | 4.7 | 4.85 | 4.55 | 4.7 | 4.85 |
| C | 6.95 | 7.1 | 7.25 | 6.95 | 7.1 | 7.25 |
| D | 7.15 | 7.3 | 7.45 | 7.15 | 7.3 | 7.45 |

Figure 11. QFN64 9 x 9 x 1.0 mm 64 pitch 0.50 drawing

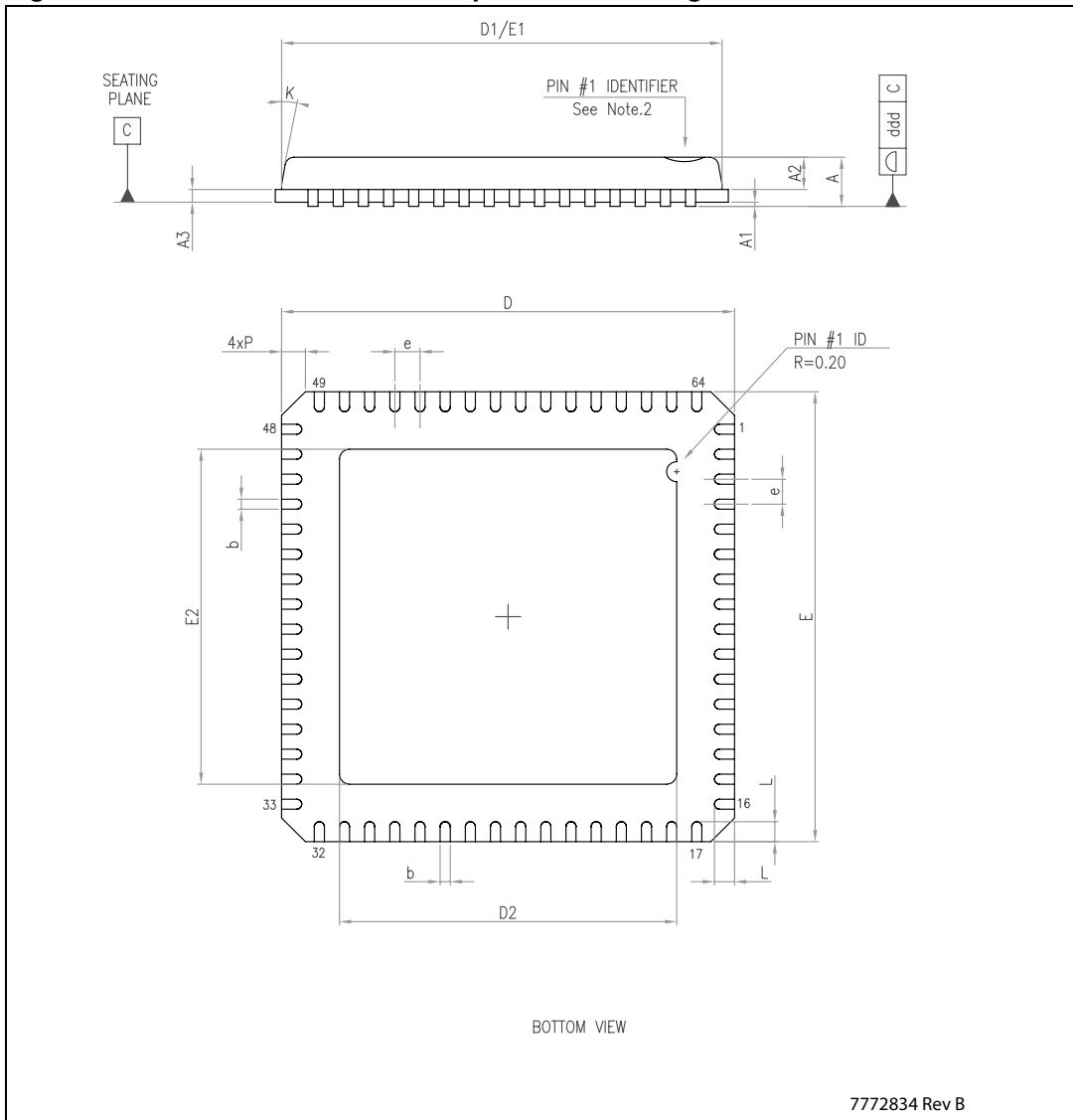
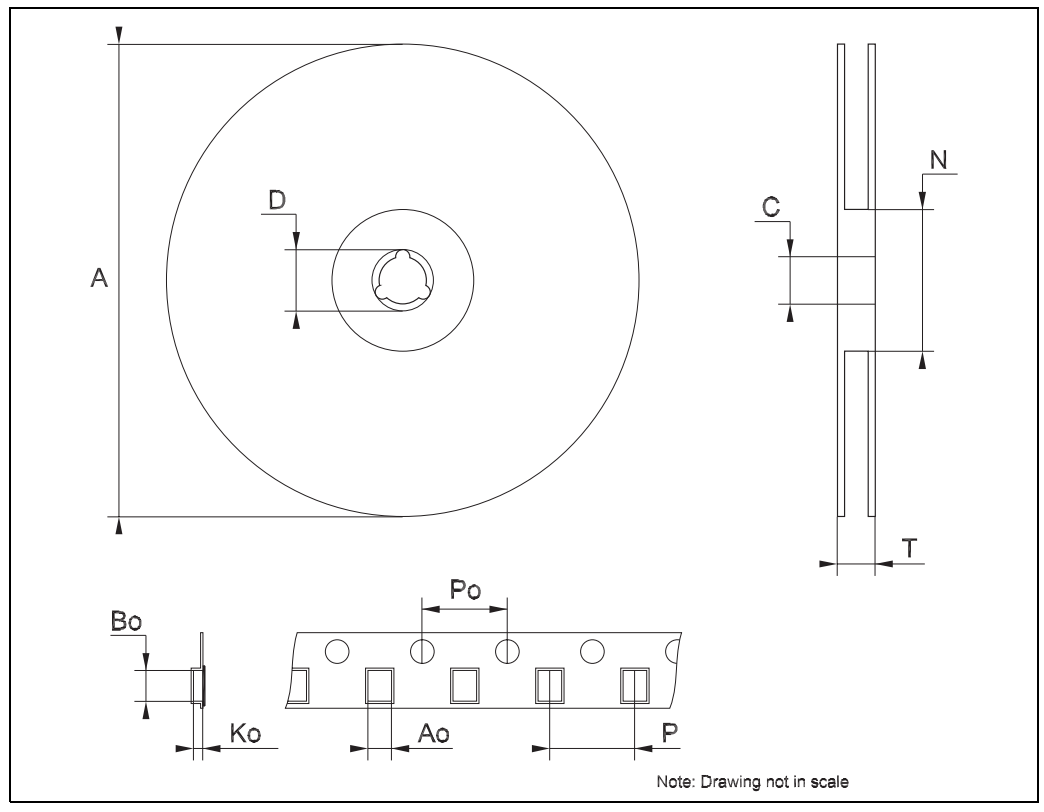


Figure 12. QFN64 9 x 9 x 1.0 mm 64 tape and reel information

| DIM. | mm. | | | inch | | |
|------|-------|-----|-------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 30.4 | | | 1.196 |
| Ao | 12.25 | | 12.45 | 0482 | | 0.490 |
| Bo | 12.25 | | 12.45 | 0482 | | 0.490 |
| Ko | 2.1 | | 2.3 | 0.083 | | 0.091 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 15.9 | | 16.1 | 0.626 | | 0.639 |



10 Revision history

Table 14. Document revision history

| Date | Revision | Changes |
|-------------|----------|-----------------|
| 20-Jan-2010 | 1 | Initial release |

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