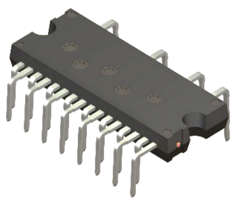
STGIPQ8C60T-HZ

SLLIMM™ nano - 2nd series

IPM, 3-phase inverter, 8 A, 600 V short-circuit rugged IGBTs

Datasheet - production data



N2DIP-26L type Z

Features

- IPM 8 A, 600 V 3-phase IGBT inverter bridge including 3 control ICs for gates driving and freewheeling diodes
- 3.3 V, 5 V and 15 V TTL/CMOS inputs comparators with hysteresis and pull down/pull up resistors
- Internal bootstrap diode
- Optimized for low electromagnetic interference
- Undervoltage lockout
- Short-circuit rugged TFS IGBTs
- Smart shutdown function
- Interlocking function
- Op-amp for advanced current sensing
- Comparator for fault protection against overcurrent
- NTC (UL 1434 CA 2 and 4)
- Isolation rating of 1500 Vrms/min

Applications

- 3-phase inverters for motor drives
- Home appliances such as dishwashers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

Description

This second series of SLLIMM (small low-loss intelligent molded module) nano provides a compact, high performance AC motor drive in a simple, rugged design. It is composed of six improved short-circuit rugged trench gate field-stop IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is designed to allow a better and easy screw on heatsink, it is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPQ8C60T-HZ	GIPQ8C60T-HZ	N2DIP-26L	Tube

Contents

1 Internal schematic and pin description

Figure 1. Internal schematic diagram and pin configuration

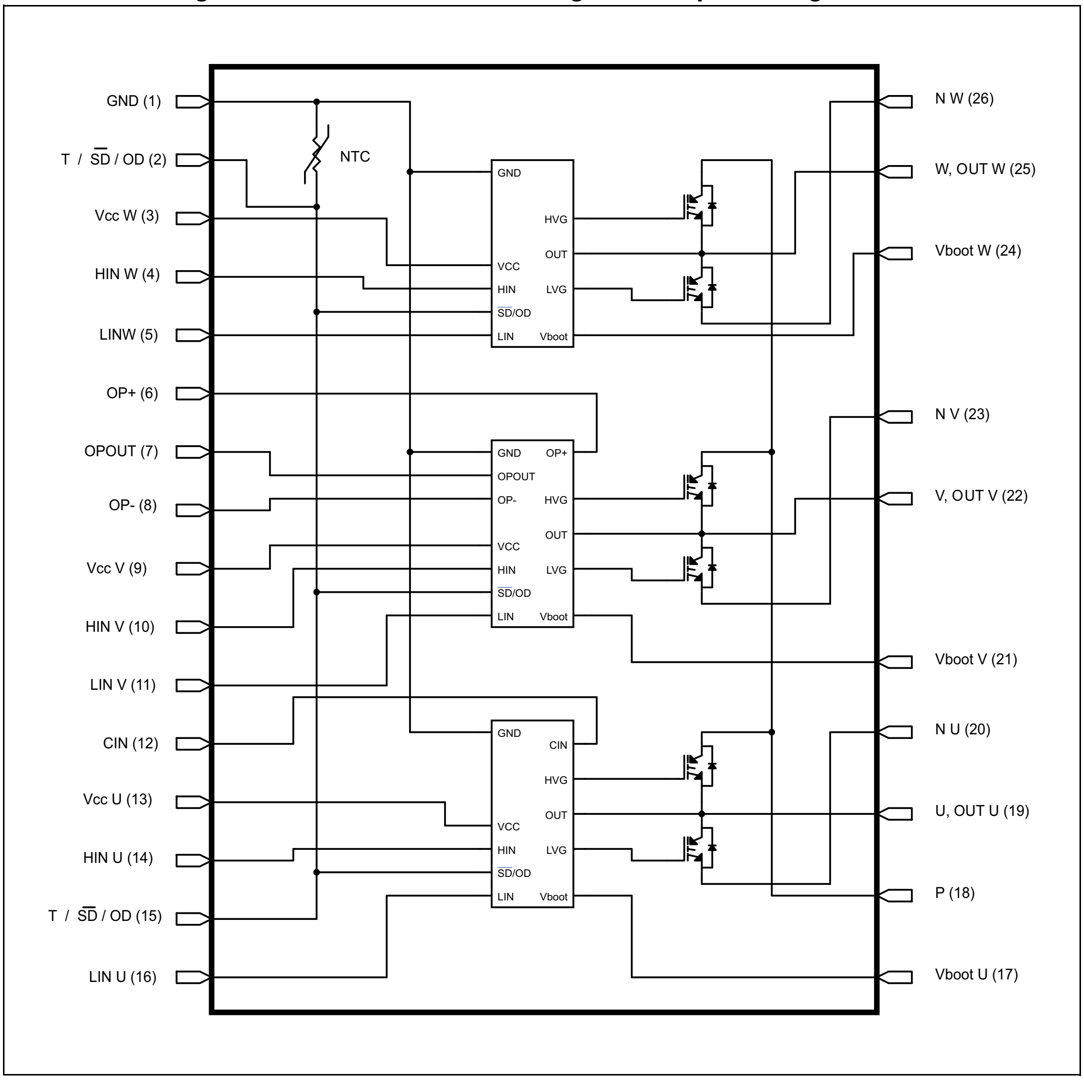


Table 2. Pin description

Pin	Symbol	Description
1	GND	Ground
2	T/$\overline{SD}$/OD	NTC thermistor terminal / shutdown logic input (active low) / open-drain (comparator output)
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	LIN W	Low-side logic input for W phase
6	OP+	Op-amp non inverting input
7	OPout	Op-amp output
8	OP-	Op-amp inverting input
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	LIN V	Low-side logic input for V phase
12	CIN	Comparator input
13	V_{CC} U	Low voltage power supply V phase
14	HIN U	High-side logic input for V phase
15	T/$\overline{SD}$/OD	NTC thermistor terminal / shutdown logic input (active low) / open-drain (comparator output)
16	LIN U	Low-side logic input for U phase
17	V_{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U,OUT_U	U phase output
20	N_U	Negative DC input for U phase
21	V_{BOOT} V	Bootstrap voltage for V phase
22	V,OUT_V	V phase output
23	N_V	Negative DC input for V phase
24	V_{BOOT} W	Bootstrap voltage for W phase
25	W,OUT_W	W phase output
26	N_W	Negative DC input for W phase

2 Absolute maximum ratings

(T_j= 25°C unless otherwise noted).

Table 3. Inverter parts

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage each IGBT (V_{IN}[(1)] = 0 V)	600	V
I_C	Continuous collector current each IGBT	8	A
I_{CP}[(2)]	Peak collector current each IGBT (less than 1ms)	16	A
P_{TOT}	Total dissipation at T_C=25 °C each IGBT	19.2	W
t_{scw}	Short-circuit withstand time (V_{CE} = 300 V, T_J = 125 °C, V_{CC} = V_{boot} = 15 V, V_{IN}[(1)]= 0 to 5 V)	5	µs

1. Applied between HINx, LINx and GND for x = U, V, W.
2. Pulsed width limited by max junction temperature.

Table 4. Control parts

Symbol	Parameter	Min	Max	Unit
V_{CC}	Low voltage power supply	-0.3	21	V
V_{BOOT}	Bootstrap voltage	-0.3	620	V
V_{OUT}	Output voltage between OUT_U, OUT_V, OUT_W and GND	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{CIN}	Comparator input voltage	-0.3	V_{CC} + 0.3	V
V_{op+}	Op-amp non-inverting input	-0.3	V_{CC} + 0.3	V
V_{op-}	Op-amp inverting input	-0.3	V_{CC} + 0.3	V
V_{IN}	Logic input voltage applied between HINx, LINx and GND	-0.3	15	V
$V_{T/\overline{SD}/OD}$	Open drain voltage	-0.3	15	V
$\Delta V_{OUT/dt}$	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60sec.)	1500	Vrms
T_J	Power chips operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

2.1 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single IGBT	6.5	°C/W
	Thermal resistance junction-case single diode	10	

3 Electrical characteristics

(T_j= 25°C unless otherwise noted).

3.1 Inverter part

Table 7. Static

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{CES}	Collector-cut off current (V_{IN}[(1)] = 0 logic state)	V_{CE} = 550 V, V_{CC} = V_{boot} = 15 V	-		250	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{Boot} = 15 V, V_{IN}[(1)]= 0 to 5 V, I_C = 8 A	-	2.0	2.4	V
V_F	Diode forward voltage	V_{IN}[(1)] = 0 logic state, I_C = 8 A	-	2.4		V

1. Applied between HINx, LINx and GND for x = U, V, W

Table 8. Inductive load switching time and energy

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{on}[(1)]	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}[(2)] = 0 to 5 V, I_C = 8 A (see *Figure 3*)	-	290	-	ns
t_{con}[(1)]	Cross-over time on		-	145	-	ns
t_{off}[(1)]	Turn-off time		-	515	-	ns
t_{coff}[(1)]	Cross-over time off		-	90	-	ns
t_{rr}	Reverse recovery time		-	110	-	ns
E_{ON}	Turn-on switching energy		-	200	-	µJ
E_{OFF}	Turn-off switching energy		-	95	-	µJ

1. t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.
2. Applied between HINx, LINx and GND for x = U, V, W

Figure 2. Switching time test circuit

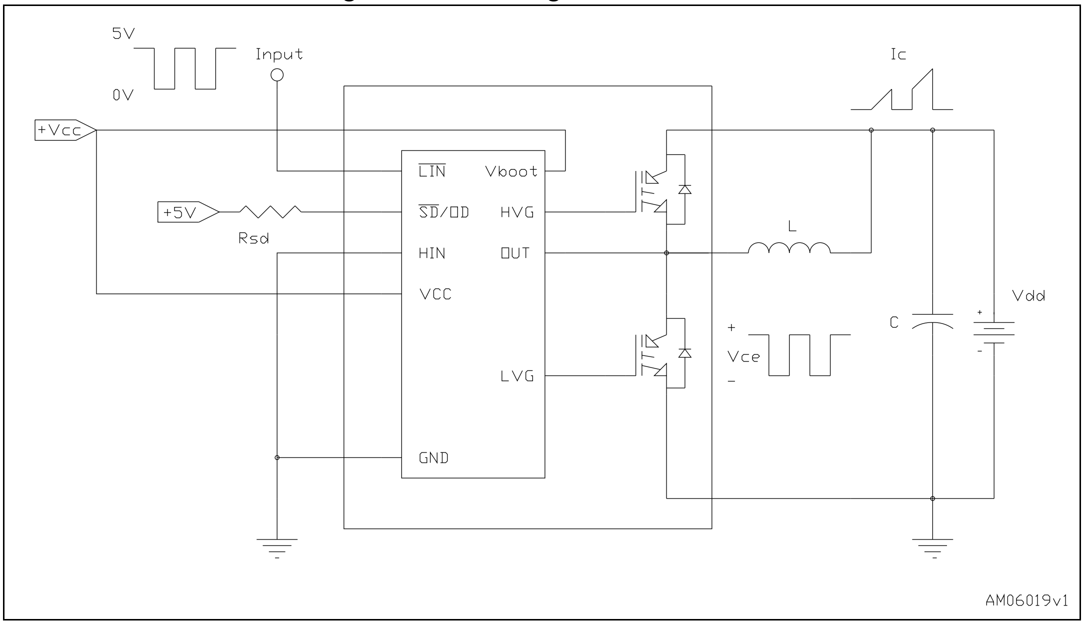
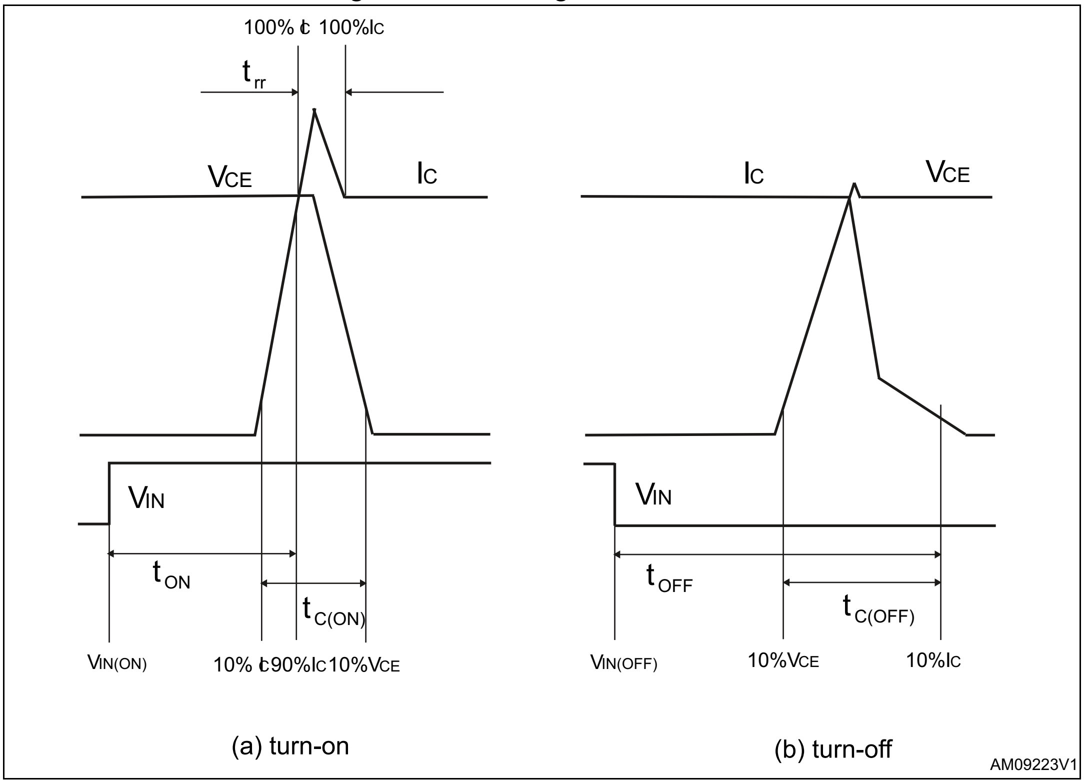


Figure 3. Switching time definition



3.2 Control part

(V_{CC}=15 V unless otherwise specified)

Table 9. Low voltage power supply

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
$V_{CCH\_th(on)}$	V_{CCH} UV turn-on threshold		11.5	12	12.5	V
$V_{CCH\_th(off)}$	V_{CCH} UV turn-off threshold		10	10.5	11	V
I_{qccu}	Under voltage quiescent supply current	V_{CC}=10V; $V_{T/\overline{SD}/OD}$=5V; L_{IN}=H_{IN}=C_{IN}=0			150	µA
I_{qcc}	Quiescent current	V_{CC}=10 V; $V_{T/\overline{SD}/OD}$=5V; L_{IN}=H_{IN}=C_{IN}=0			1	mA
V_{REF}	Internal comparator (C_{IN}) reference voltage		0.51	0.54	0.56	V

Table 10. Bootstrapped voltage

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
$V_{BS\_th(on)}$	V_{BS} UV turn-on threshold		11.1	11.5	12.1	V
$V_{BS\_th(off)}$	V_{BS} UV turn-off threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} <9V $V_{T/\overline{SD}/OD}$=5V; L_{IN}=0V;H_{IN}=5V;C_{IN}=0F;		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} =15V $V_{T/\overline{SD}/OD}$=5V; L_{IN}=0V;H_{IN}=5V;C_{IN}=0F;		150	210	µA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 11. Logic inputs

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.25			V
I_{HINh}	HIN logic “1” input bias	HIN=15V	20	40	100	µA
I_{HINl}	HIN logic “0” input bias current	HIN=0V			1	µA
I_{LINh}	LIN logic “1” input bias current	LIN=15V	20	40	100	µA
I_{LINl}	LIN logic “0” input bias current	LIN=0V			1	µA
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ =15V	220	295	370	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ =0V			3	µA
Dt	Dead time	See *Figure 8*		180		ns

Table 12. Op-amp characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{io}	Input offset voltage	V_{ic}=0V, V_o=7.5V			6	mV
I_{io}	Input offset current	V_{ic}=0V, V_o=7.5V		4	40	nA
I_{ib}	Input bias current(1)	V_{ic}=0V, V_o=7.5V		100	200	nA
V_{OL}	Low level output voltage range	R_L=10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage range	R_L=10 kΩ to GND	14	14.7		V
I_o	Output short-circuit current	Source V_{id}=+1V, V_o=0V	16	30		mA
		Sink V_{id}=-1V, V_o= V_{CC}	50	80		mA
SR	Slew rate	V_i=1-4V; C_L=100pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o=7.5V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L=2 kΩ	70	85		dB

Table 12. Op-amp characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
SVR	Supply voltage rejection ratio	vs. V_{cc}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of the input current is out of the IC.

Table 13. Sense comparator characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{ib}	Input bias current	V_{Cin}=1V	-		3	µA
V_{od}	Open drain low level output voltage	I_{od}=3mA	-		0.5	V
R_{ON_OD}	Open drain low level output resistance	I_{od}=3mA	-	166		Ω
R_{PD_SD}	$\overline{SD}$ pull down resistor(1)			125		kΩ
t_{d_comp}	Comparator delay	$V_{T/\overline{SD}/OD}$ pulled to 5V through 100 kΩ resistor	-	90	130	ns
SR	Slew rate	C_L=180pF; R_{pu}=5 kΩ	-	60		V/µs
t_{sd}	Shutdown to high/low side driver propagation delay	V_{OUT} =0V, V_{boot} = V_{CC}, V_{IN}=0 to 3.3V	50	125	200	ns
t_{isd}	Comparator triggering to high/low side driver turn-off propagation delay	Measured applying a voltage step from 0V to 3.3V to pin of C_{IN}	50	200	250	ns

1. Equivalent value as a result of the resistances of three drivers in parallel

Table 14. Truth table

Condition	Logic input (V_I)			Output	
	T/$\overline{SD}$/OD	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X(1)	X(1)	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 “logic state” half-bridge tri-state	H	L	L	L	L
1 “logic state” Low side direct driving	H	H	L	H	L
1 “logic state” high side direct driving	H	L	H	L	H

1. X = don’t care

3.2.1 NTC thermistor

Figure 4. Internal structure of $\overline{SD}$ and NTC[a]

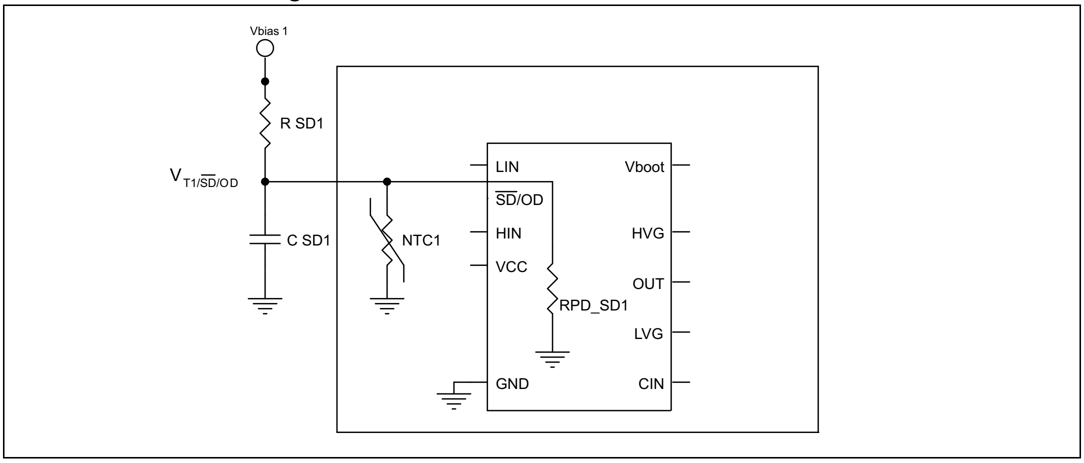
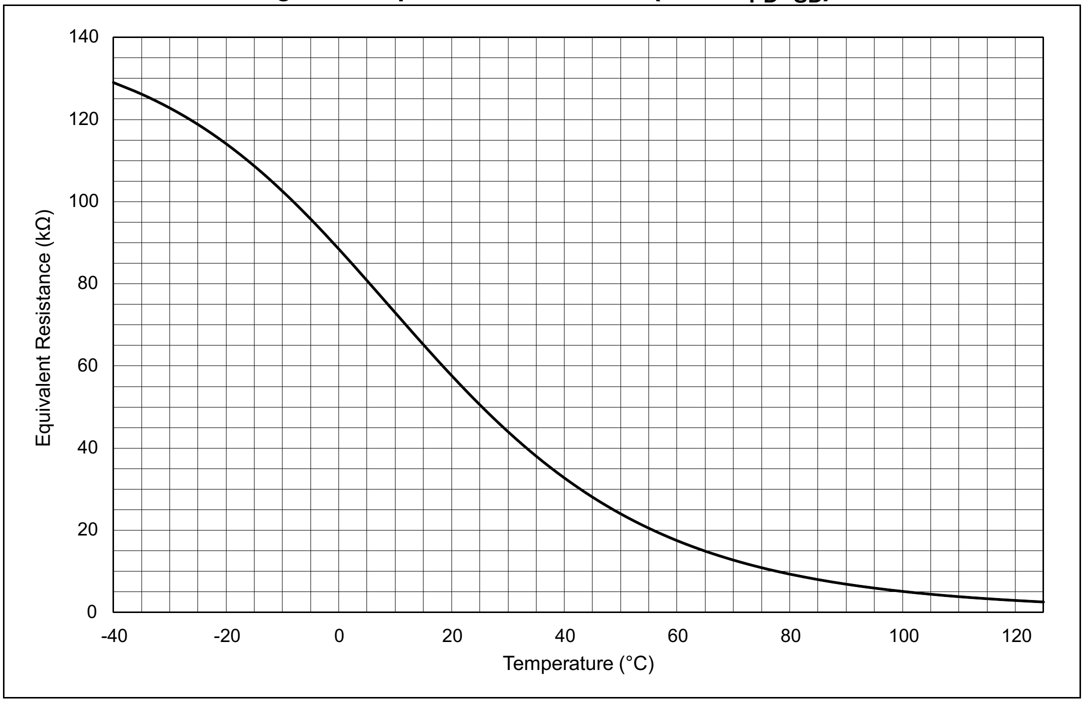


Figure 5. Equivalent resistance (NTC//R_{PD_SD})



a. RPD_SD: equivalent value as result of resistances of three drivers in parallel.

Figure 6. Equivalent resistance (NTC//R_{PD_SD}) zoom

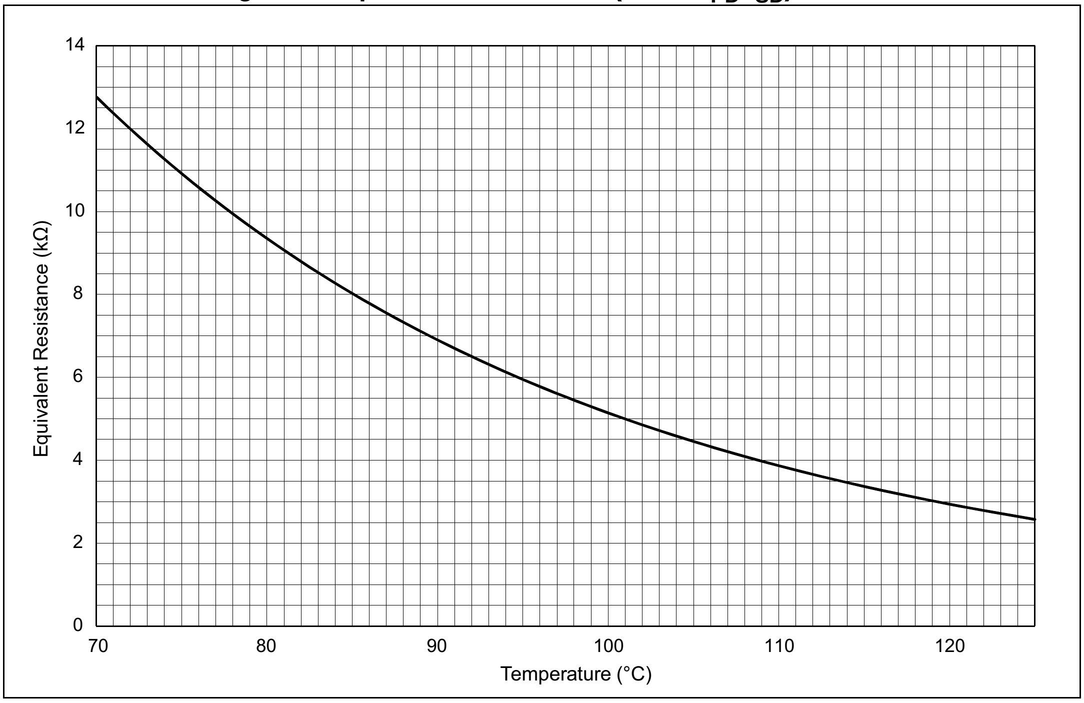
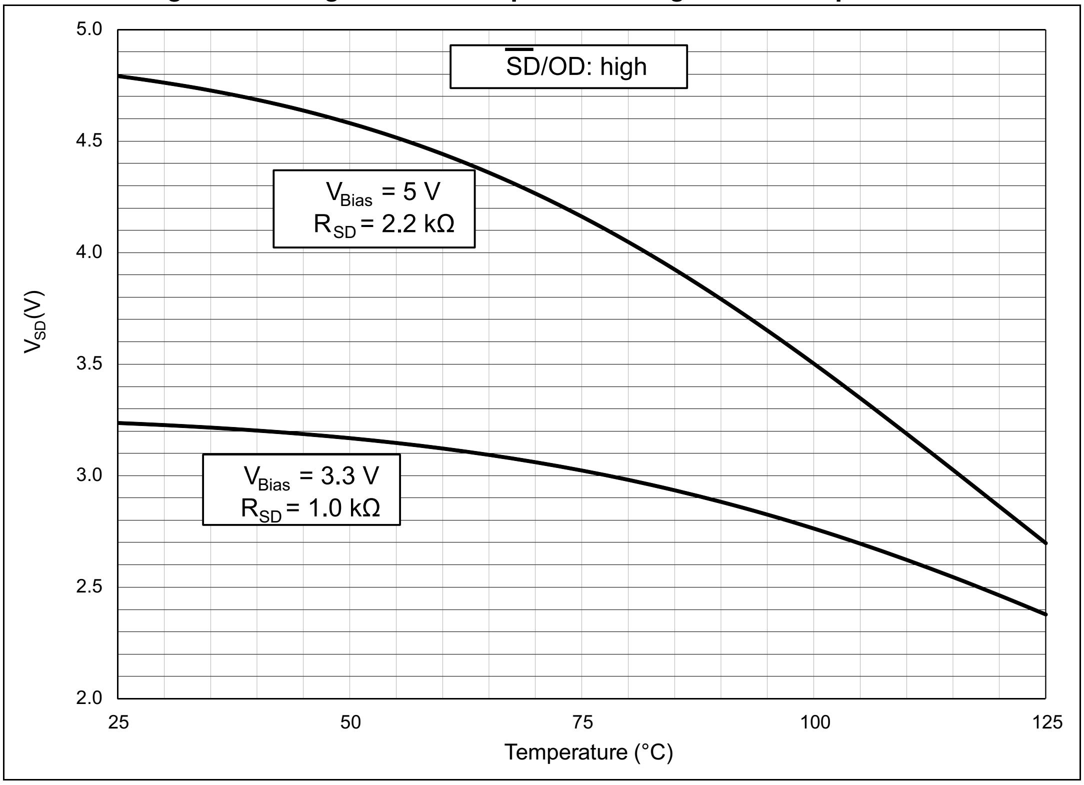
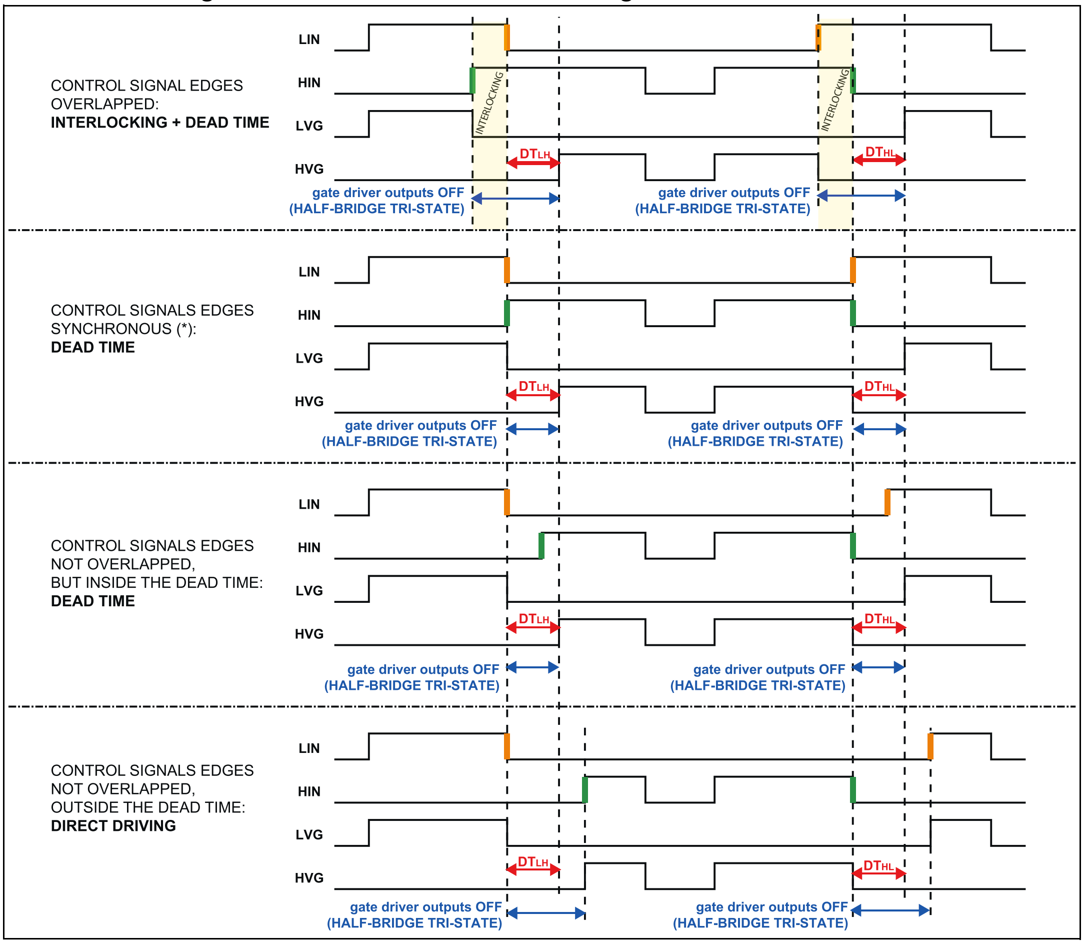


Figure 7. Voltage of T/$\overline{SD}$/OD pin according to NTC temperature



3.3 Waveform definitions

Figure 8. Dead time and interlocking waveform definitions



4 Smart shutdown function

The device integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference V_{REF} connected to the inverting input, while the non-inverting input on pin (CIN) can be connected to an external shunt resistor for simple overcurrent protection.

When the comparator triggers, the device is set to the Shutdown state and both its outputs are switched to the low-level setting, causing the half bridge to enter a tri-state.

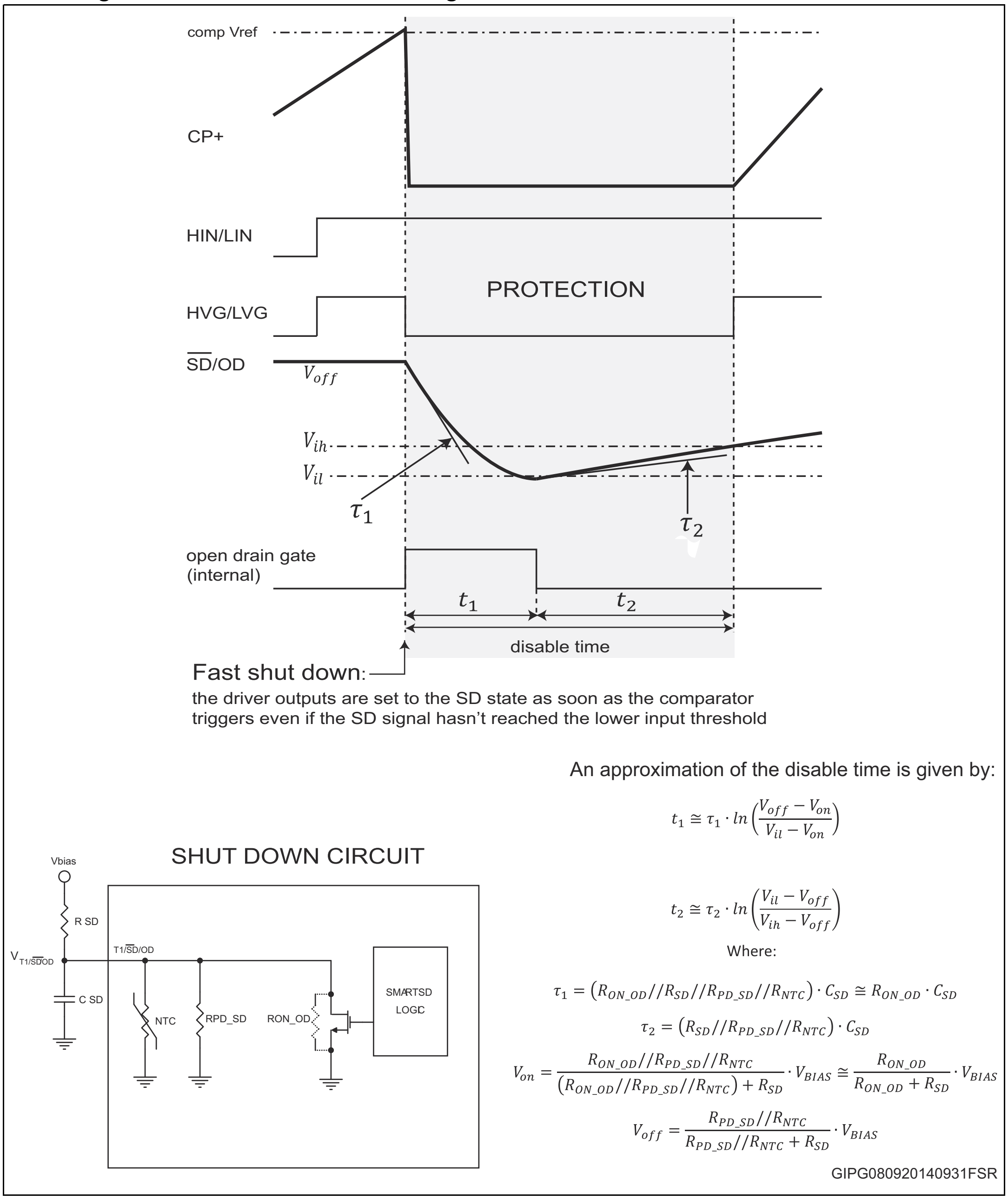
In common overcurrent protection architectures, the comparator output is usually connected to the Shutdown input through an RC network that provides a mono-stable circuit which implements a protection time following a fault condition.

Our smart shutdown architecture immediately turns off the output gate driver in case of overcurrent along a preferential path for the fault signal which directly switches off the outputs. The time delay between the fault and output shutdown no longer depends on the RC values of the external network connected to the shutdown pin. At the same time, the DMOS connected to the open-drain output (pin T/$\overline{SD}$/OD) is turned on by the internal logic, which holds it on until the shutdown voltage is lower than the logic input lower threshold (Vil).

Also, the smart shutdown function allows increasing the real disable time without increasing the constant time of the external RC network.

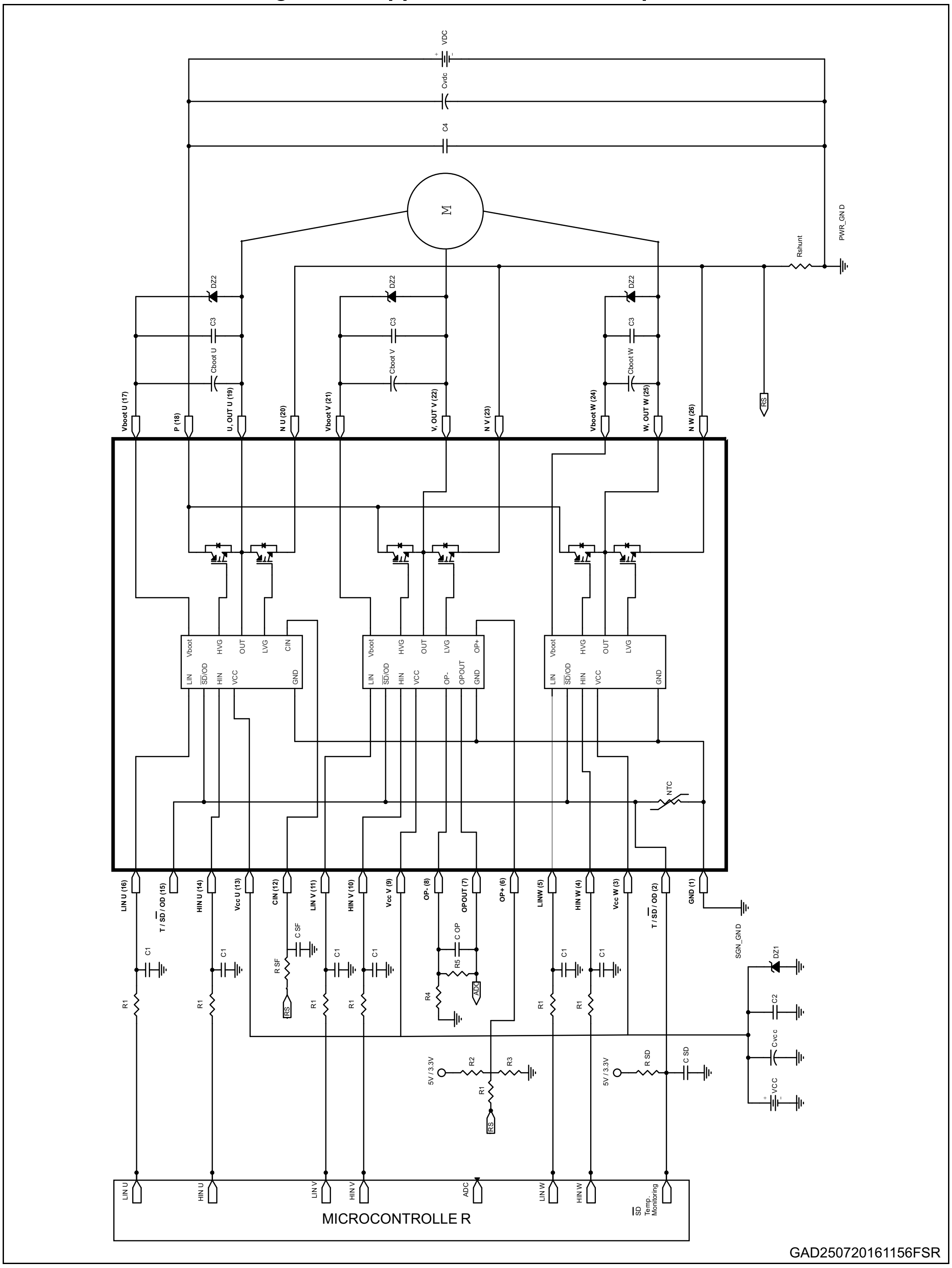
An NTC thermistor for temperature monitoring is internally connected in parallel to the $\overline{SD}$ pin. To avoid undesired shutdown, keep the voltage $V_{T/\overline{SD}/OD}$ higher than the high-level logic threshold by setting the pull-up resistor $R_{\overline{SD}}$ to 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU power supplies, respectively.

Figure 9. Smart shutdown timing waveforms in case of overcurrent event



5 Application circuit example

Figure 10. Application circuit example[b]



b. Application designers are free to use a different scheme according with the specifications of the device.

6 Guidelines

- Input signals HIN, LIN are active-high logic. A 375 kΩ (typ.) pull-down resistor is built-in for each input. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is suggested. The filters should be done with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
- The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can help to reduce the transient circuit demand on the power supply. Also, to reduce high frequency switching noise distributed on the power lines, placing a decoupling capacitor C2 (100 to 220 nF, with low ESR and low ESL) as close as possible to Vcc pin and in parallel whit the bypass capacitor is suggested.
- The use of RC filter (RSF, CSF) for preventing protection circuit malfunction is recommended. The time constant (RSF x CSF) should be set to 1 µs and the filter must be placed as close as possible to the CIN pin.
- The $\overline{SD}$ is an input/output pin (open drain type if used as output). A built-in thermistor NTC is internally connected between the $\overline{SD}$ pin and GND. The voltage V_{SD}-GND decreases as the temperature increases, due to the pull-up resistor R_{SD}. In order to keep the voltage always higher than the high level logic threshold, the pull-up resistor is suggested to be set at 1 kΩ or 2.2 kΩ for 3.3 V or 5 V MCU power supply, respectively. The C_{SD} capacitor of the filter on $\overline{SD}$ should be fixed no higher than 3.3 nF in order to assure a $\overline{SD}$ activation time $\tau 1 <= 500$ ns, in addition the filter should be placed as close as possible to the $\overline{SD}$ pin.
- The decoupling capacitor C_3 (from 100 to 220 nF, ceramic with low ESR and low ESL), in parallel with each C_{boot}, is useful to filter high frequency disturbance. Both C_{boot} and C3 (if present) should be placed as close as possible to the U, V, W and V_{boot} pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.
- To prevent the overvoltage on Vcc pin, a Zener diode (Dz1) can be used. Similarly on the V_{boot} pin, a Zener diode (Dz2) can be placed in parallel with each C_{boot}.
- The use of the decoupling capacitor C4 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{vdc} is useful to prevent surge destruction. Both capacitors C4 and C_{vdc} should be placed as close as possible to the IPM (C4 has priority over C_{vdc}).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Use low inductance shunt resistors for phase leg current sensing.
- In order to avoid malfunctions, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
- The connection of SGN_GND to PWR_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

Note: These guidelines are useful for application design to ensure the specifications of the device. For further details, please refer to the relevant application note.

Table 15. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied between P-N_u,N_v,N_w		300	500	V
V_{CC}	Control supply voltage	Applied between V_{cc}-GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{bootx}-OUT for x=U,V,W	13		18	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1			µs
f_{PWM}	PWM input signal	-40°C<T_c<100°C -40°C<T_j<125°C			25	kHz
T_c	Case operation temperature				100	°C

7 Electrical characteristics (curves)

Figure 11. Output characteristics (T_J = 25 °C)

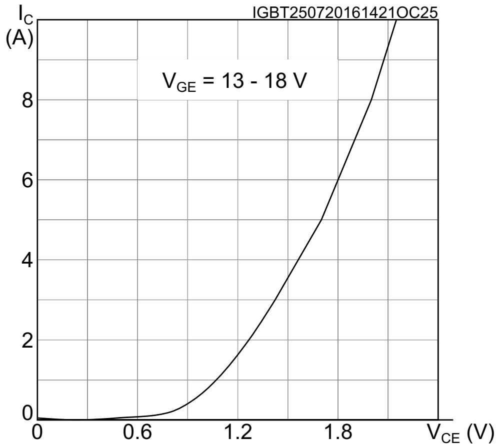


Figure 12. $V_{CE(sat)}$ vs. collector current

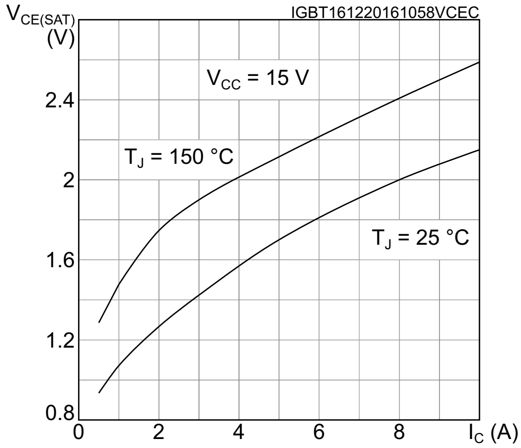


Figure 13. Diode VF vs forward current

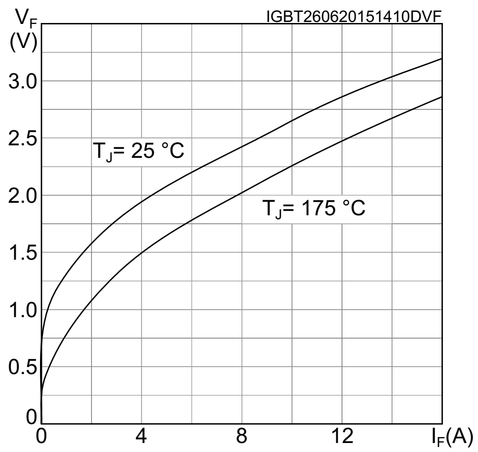


Figure 14. Eon switching energy vs collector current

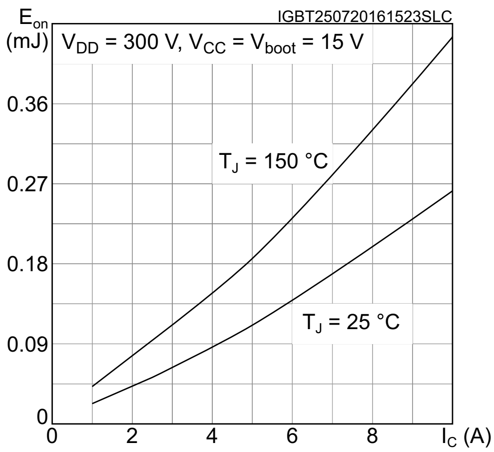


Figure 15. Eoff switching energy vs collector current

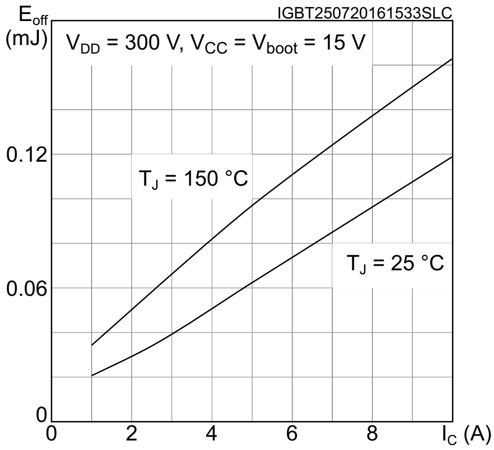
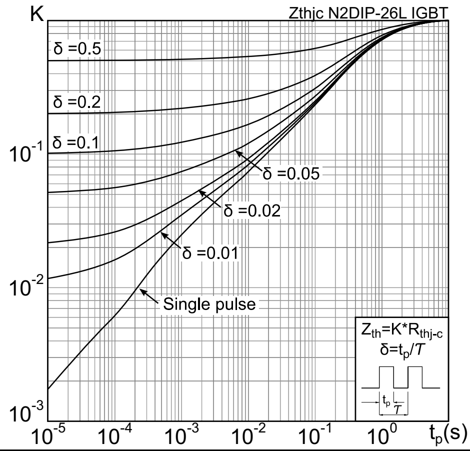


Figure 16. Thermal impedance



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 N2DIP-26L type Z package information

Figure 17. N2DIP-26L type Z package mechanical outline

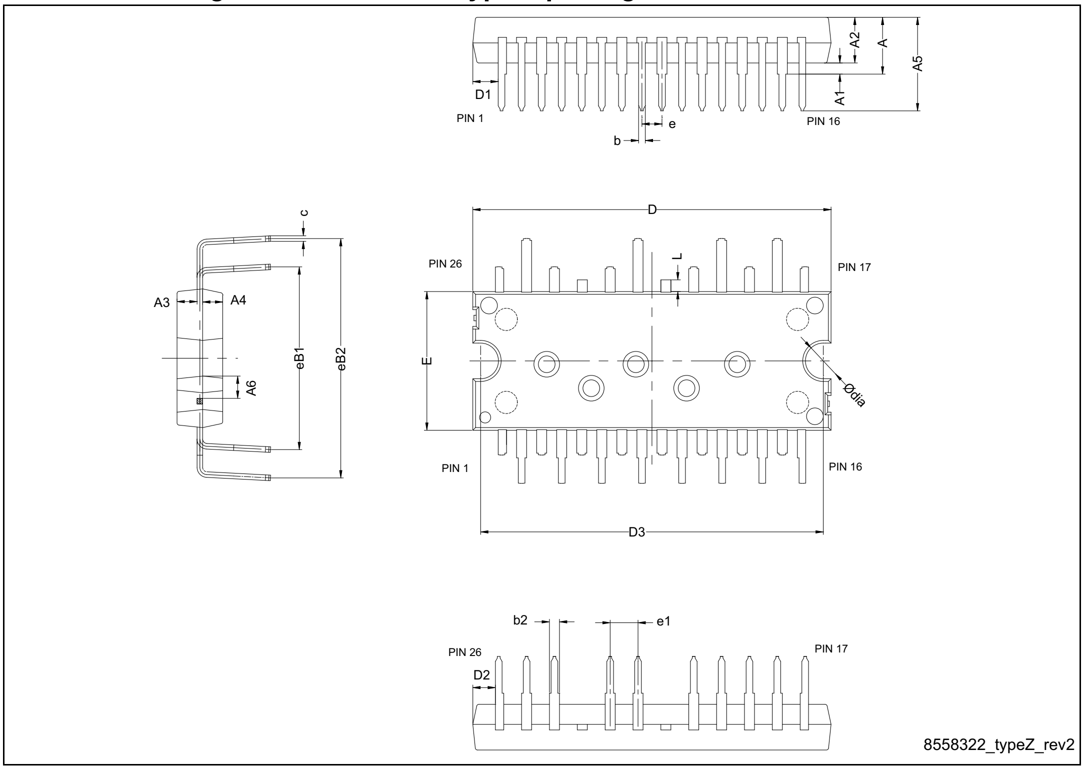


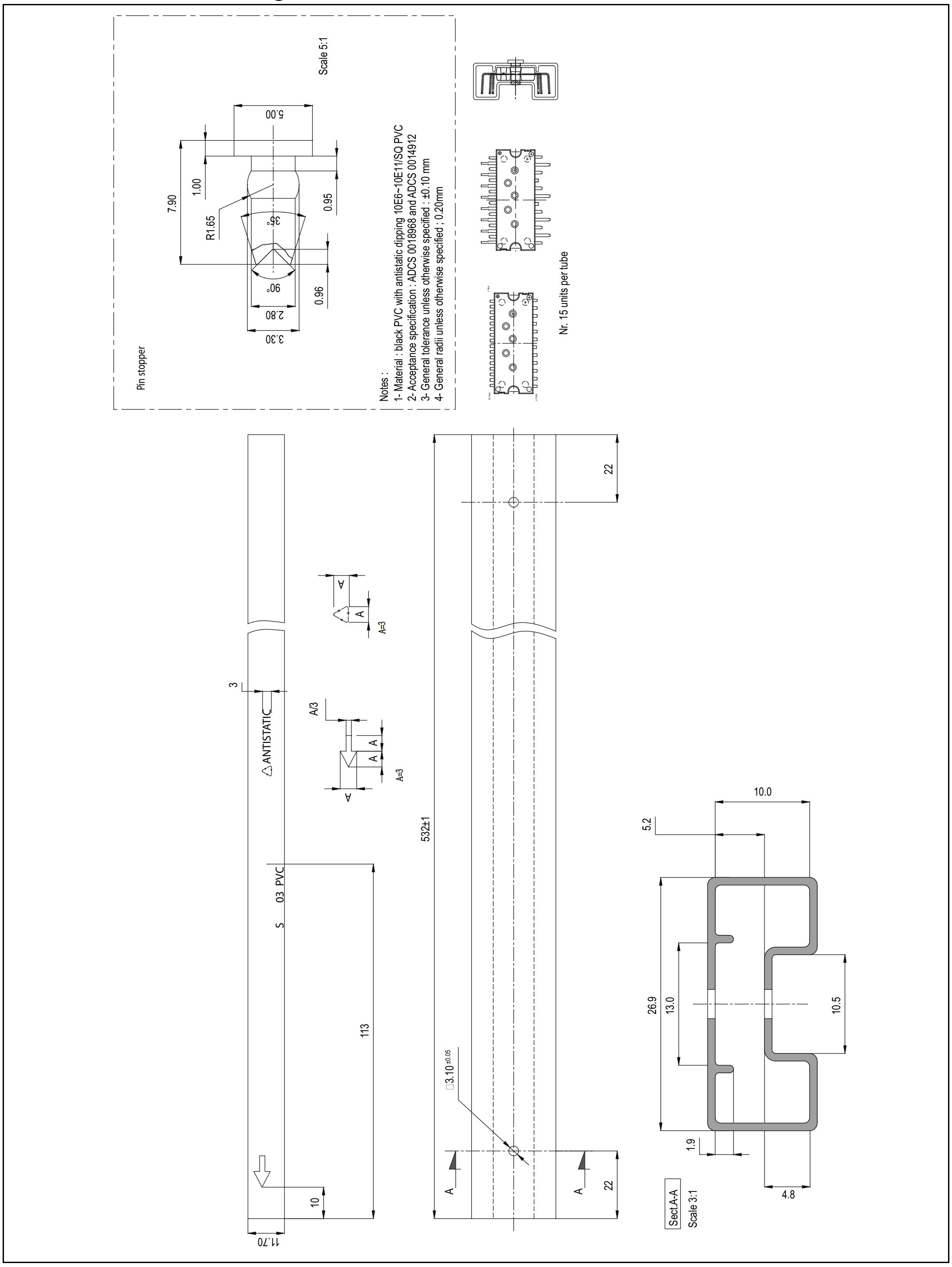
Table 16. N2DIP-26L type Z mechanical dimensions(1)

Ref.	Dimensions			Ref.	Dimensions			Ref.	Dimensions		
	Min.	Typ.	Max.		Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.80	5.10	5.40	b	0.53		0.72	E	12.35	12.45	12.55
A1	0.80	1.00	1.20	b2	0.83		1.02	e	1.70	1.80	1.90
A2	4.00	4.10	4.20	c	0.46		0.59	e1	2.40	2.50	2.60
A3	1.70	1.80	1.90	D	32.05	32.15	32.25	eB1	16.10	16.40	16.70
A4	1.70	1.80	1.90	D1	2.10			eB2	21.18	21.48	21.78
A5	8.10	8.40	8.70	D2	1.85			L	0.85	1.05	1.25
A6	1.75			D3	30.65	30.75	30.85	dia	3.10	3.20	3.30

1. All dimensions are expressed in millimeters.

9 Packaging mechanical data

Figure 18. N2DIP-26L tube dimensions[c]



c. All dimensions are expressed in millimeters.

10 Revision history

Table 17. Document revision history

Date	Revision	Changes
22-Jan-2016	1	Initial release.
26-Jul-2016	2	Document status promoted from target to preliminary data. Updated features in cover page, *Section 3: Electrical characteristics*, *Section 3.2: Control part*, *Section 5: Application circuit example* and *Section 6: Guidelines*. Added *Section 7: Electrical characteristics (curves)*.
16-Dec-2016	3	Document status promoted from preliminary to production data. Updated *Figure 12: $V_{CE(sat)}$ vs. collector current*.