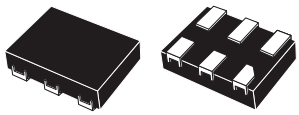
# STG5123

## Low voltage 1 Ω single SPDT switch with break-before-make feature

## Features

- High speed:
  - $t_{PD}$ = 130 ps (typ.) at $V_{CC}$ = 3.0 V
  - $t_{PD}$ = 140 ps (typ.) at $V_{CC}$ = 2.3 V
- Ultra low power dissipation:
  - $I_{CC}$ = 0.2 µA (max.) at $T_A$ = 85 °C
- Low ON resistance:
  - $R_{ON}$ = 1.0 Ω (Typ.) at $V_{CC}$ = 4.5 V
  - $R_{ON}$ = 1.2 Ω (Typ.) at $V_{CC}$ = 3.0 V
  - $R_{ON}$ = 2.0 Ω (Typ.) at $V_{CC}$ = 1.8 V
- Wide operating voltage range:
  - $V_{CC}$ (opr) = 1.65 to 4.5 V single supply
- 5 V tolerant and 1.8 V compatible threshold on digital control input at $V_{CC}$ = 1.65 to 4.5 V
- Latch-up performance exceeds 200 mA per JESD 78, Class II
- ESD performance tested per JESD22
  - 2000 V human-body model (A114-B, Class II)
  - 200 V machine model (A115-A)
  - 1000 V charged-device model (C101)



**DFN6L**

## Description

The STG5123 is a high-speed CMOS low voltage single analog SPDT (single-pole dual-throw) switch or 2:1 multiplexer/demultiplexer switch fabricated using silicon gate $C^2MOS$ technology. Designed to operate from 1.65 to 4.5 V, this device is ideal for portable applications.

The device offers very low ON resistance (1 Ω) at $V_{CC}$ = 4.5 V. The switch S1 is ON (connected to common ports Dn) when the SEL input is held high and OFF (state of high impedance state exists between the two ports) when SEL is held low. The switch S2 is ON (connected to common port D) when the SEL input is held low and OFF (state of high impedance state exists between the two ports) when SEL is held high.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD and transient excess voltage immunity.

**Table 1. Device summary**

| Order code | Package | Packaging |
|---|---|---|
| STG5123DTR | DFN6L (1.2 x 1 mm) | Tape and reel |

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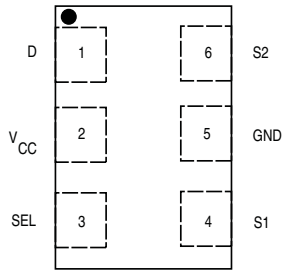
# 1 Pin connections and functions

**Figure 1. Pin connections** (top through view)




**DFN6L**

**Table 2. Pin descriptions**

| Pin number | Symbol | Name and function |
|---|---|---|
| 4 | S1 | Independent channel |
| 6 | S2 | Independent channel |
| 1 | D | Common channels |
| 3 | SEL | Control |
| 2 | $V_{CC}$ | Positive supply voltage |
| 5 | GND | Ground (0V) |

**Figure 2. Input equivalent circuit**

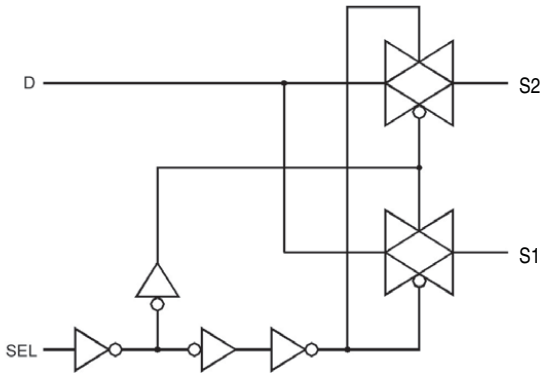



**Table 2. Truth table**

| Sel | Switch S1 | Switch S2 |
|---|---|---|
| H | ON | OFF (1) |
| L | OFF (1) | ON |

1. High impedance

# 2 Electrical ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.5 to 5.5 | V |
| $V_I$ | DC input voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $V_{IC}$ | DC control input voltage | –0.5 to 5.5 | V |
| $V_O$ | DC output voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{IKC}$ | DC input diode current on control pin ($V_{SEL}$ < 0 V) | –50 | mA |
| $I_{IK}$ | DC input diode current ($V_{IN}$ < 0 V) | ±50 | mA |
| $I_{OK}$ | DC output diode current | ±20 | mA |
| $I_O$ | DC output current | ±200 | mA |
| $I_{OP}$ | DC output current peak (pulse at 1 ms, 10% duty cycle) | ±400 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or ground current | ±100 | mA |
| $P_D$ | Power dissipation at $T_A$ = 70ºC (1) | 1120 | mW |
| $T_{STG}$ | Storage temperature | –65 to 150 | °C |
| $T_L$ | Lead temperature (10 sec) | 300 | °C |

1. Derate above 70ºC by 18.5mW/C

**Table 4. Recommended operating conditions**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 to 4.5 | V |
| $V_I$ | Input voltage | | 0 to $V_{CC}$ | V |
| $V_{IC}$ | Control input voltage | | 0 to 4.5 | V |
| $V_O$ | Output voltage | | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating temperature | | –40 to 85 | °C |
| dt/dv | Input rise and fall time control input | $V_{CC}$ = 1.65 to 2.7 V | 0 to 20 | ns/V |
| | | $V_{CC}$ = 3.0 to 4.5 V | 0 to 10 | |

# 3 Electrical characteristics

## 3.1 DC electrical characteristics

**Table 5. DC specifications**

| Symbol | Parameter | $V_{CC}$ (V) | Test condition | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | High level input voltage | 1.65 – 1.95 | | 0.65 $V_{CC}$ | | | 0.65 $V_{CC}$ | | V |
| | | 2.3 – 2.5 | | 1.2 | | | 1.2 | | |
| | | 2.7 – 3.0 | | 1.3 | | | 1.3 | | |
| | | 3.3 – 3.6 | | 1.4 | | | 1.4 | | |
| | | 4.5 | | 1.6 | | | 1.6 | | |
| $V_{IL}$ | Low level input voltage | 1.65 – 1.95 | | | | 0.40 | | 0.40 | V |
| | | 2.3 – 2.5 | | | | 0.60 | | 0.60 | |
| | | 2.7 – 3.0 | | | | 0.60 | | 0.60 | |
| | | 3.3 – 3.6 | | | | 0.60 | | 0.60 | |
| | | 4.5 | | | | 0.80 | | 0.80 | |
| $R_{ON}$ | Switch ON resistance | 1.8 | $V_S$ = 0 V to $V_{CC}$ $I_S$ = 100 mA | | 2.0 | 3.0 | | 3.5 | Ω |
| | | 2.7 | | | 1.3 | 1.6 | | 1.8 | |
| | | 3.0 | | | 1.2 | 1.5 | | 1.7 | |
| | | 4.5 | | | 1.0 | 1.2 | | 1.4 | |
| $\Delta R_{ON}$ | ON resistance match between channels (1) | 1.8 | $V_S$ at $R_{ON}$ max $I_S$ = 100 mA | | 0.06 | | | | Ω |
| | | 2.7 | | | 0.05 | | | | |
| | | 3.0 | | | 0.05 | | | | |
| | | 4.5 | | | 0.05 | | | | |
| $R_{FLAT}$ | ON resistance flatness (2) | 1.8 | $V_S$ = 0 V to $V_{CC}$ $I_S$ = 100 mA | | 1.0 | 1.5 | | 1.5 | Ω |
| | | 2.7 | | | 0.45 | 0.60 | | 0.70 | |
| | | 3.0 | | | 0.43 | 0.50 | | 0.60 | |
| | | 4.5 | | | 0.39 | 0.50 | | 0.60 | |
| $I_{OFF}$ | OFF state leakage current (SN), (D) | 4.3 | $V_S$ = 0.3 or 4 V | | | ±20 | | ±100 | nA |
| $I_{IN}$ | Input leakage current | 0 – 5.0 | $V_{SEL}$ = 0 to 4.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | Quiescent supply current | 1.65 – 5.0 | $V_{SEL}$ = $V_{CC}$ or GND | | | ±0.05 | | ±0.2 | µA |

**Table 5. DC specifications (continued)**

| Symbol | Parameter | $V_{CC}$ (V) | Test conditions | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $I_{CCLV}$ | Quiescent supply current low voltage driving | 4.3 | $V_{SEL}$ = 1.65 V | | ±17 | ±35 | | ±70 | µA |
| | | 4.3 | $V_{SEL}$ = 1.80 V | | ±15 | ±30 | | ±60 | |
| | | 4.3 | $V_{SEL}$ = 2.60 V | | ±5 | ±10 | | ±20 | |

1. $\Delta R_{ON} = R_{ON(Max)} - R_{ON(Min)}$
2. Flatness is defined as the difference between the maximum and minimum value of ON resistance as measured over the specified analog signal ranges.

## 3.2 AC electrical characteristics

**Table 6. AC electrical characteristics** ($C_L$ = 35 pF, $R_L$ = 50 Ω, $t_r = t_f \leq$5 ns)

| Symbol | Parameter | $V_{CC}$ (V) | Test conditions | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | | | – 40 to 85 °C | | |
| | | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | 1.65 – 1.95 | | | 0.15 | | | | ns |
| | | 2.3 – 2.7 | | | 0.14 | | | | |
| | | 3.0 – 3.3 | | | 0.13 | | | | |
| | | 3.6 – 5.0 | | | 0.13 | | | | |
| $t_{ON}$ | Turn-ON time | 1.65 – 1.95 | $V_S$ = 0.8 V | | 36 | | | | ns |
| | | 2.3 – 2.7 | $V_S$ = 1.5 V | | 31 | 40 | | 45 | |
| | | 3.0 – 3.3 | | | 24 | 31 | | 40 | |
| | | 3.6 – 5.0 | | | 21 | 28 | | 32 | |
| $t_{OFF}$ | Turn-OFF time | 1.65 – 1.95 | $V_S$ = 0.8 | | 29 | | | | ns |
| | | 2.3 – 2.7 | $V_S$ = 1.5 V | | 17 | 27 | | 37 | |
| | | 3.0 – 3.3 | | | 12 | 23 | | 33 | |
| | | 3.6 – 5.0 | | | 11 | 21 | | 31 | |
| $t_D$ | Break-before-make time delay | 1.65 – 1.95 | $C_L$ = 35 pF<br>$R_L$ = 50 Ω<br>$V_S$ = 1.5 V | | 15 | | | | ns |
| | | 2.3 – 2.7 | | | 10 | | | | |
| | | 3.0 – 3.3 | | | 8 | | | | |
| | | 3.6 – 5.0 | | | 6 | | | | |
| Q | Charge injection | 1.65 | $C_L$ = 100pF<br>$V_{GEN}$ = 0 V<br>$R_{GEN}$ = 0 Ω | | 16 | | | | pC |
| | | 2.3 | | | 22 | | | | |
| | | 3 | | | 26 | | | | |
| | | 5.0 | | | 33 | | | | |

## 3.3 Analog switch characteristics

**Table 7. Analog switch characteristics** ($C_L$ = 5 pF, $R_L$ = 50 Ω, $T_A$ = 25 °C)

| Symbol | Parameter | $V_{CC}$ (V) | Test conditions | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | Min | Typ | Max | Min | Max | |
| OIRR | Off isolation (1) | 1.65 – 5.0 | $V_S$ = 1 $V_{RMS}$<br>f = 100 kHz | | – 75 | | | | dB |
| Xtalk | Crosstalk | 1.6 – 5.0 | $V_S$ = 1 $V_{RMS}$<br>f = 100 kHz | | – 80 | | | | dB |
| THD | Total harmonic distortion | 2.3 – 5.0 | $R_L$ = 600 Ω<br>$V_S$ = 2 $V_{PP}$<br>f = 20 Hz to 20 kHz | | 0.03 | | | | % |
| BW | -3dB bandwidth | 1.65 – 5.0 | $R_L$ = 50 Ω | | 150 | | | | MHz |
| $C_{IN}$ | Control pin input capacitance | | | | 6 | | | | pF |
| $C_{ON}$ | Sn port capacitance when switch is enabled | 3.3 | f = 1 MHz | | 52 | | | | |
| $C_{OFF}$ | Sn port capacitance when switch is disabled | 3.3 | f = 1 MHz | | 25 | | | | |
| $C_D$ | D port capacitance when switch is enabled | 3.3 | f = 1 MHz | | 50 | | | | |

1. OFF isolation = $20Log_{10}$ ($V_D/V_S$), $V_D$ = output. $V_S$ = input to OFF switch.

# 4 Test circuits

**Figure 3. ON resistance**

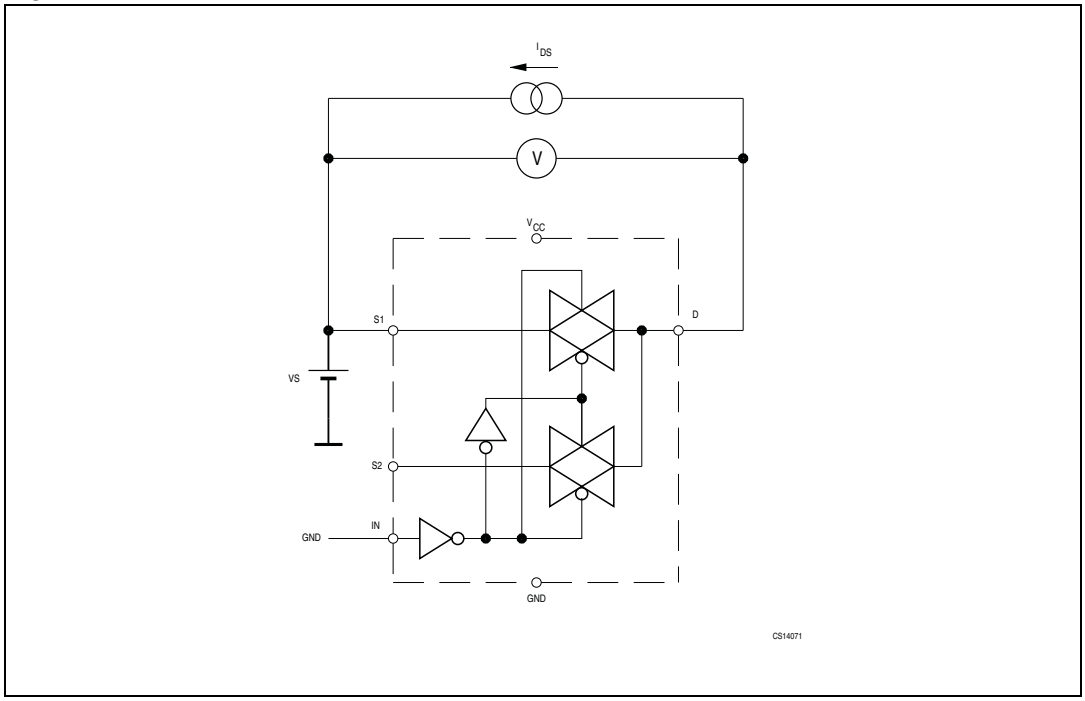



**Figure 4. Bandwidth**

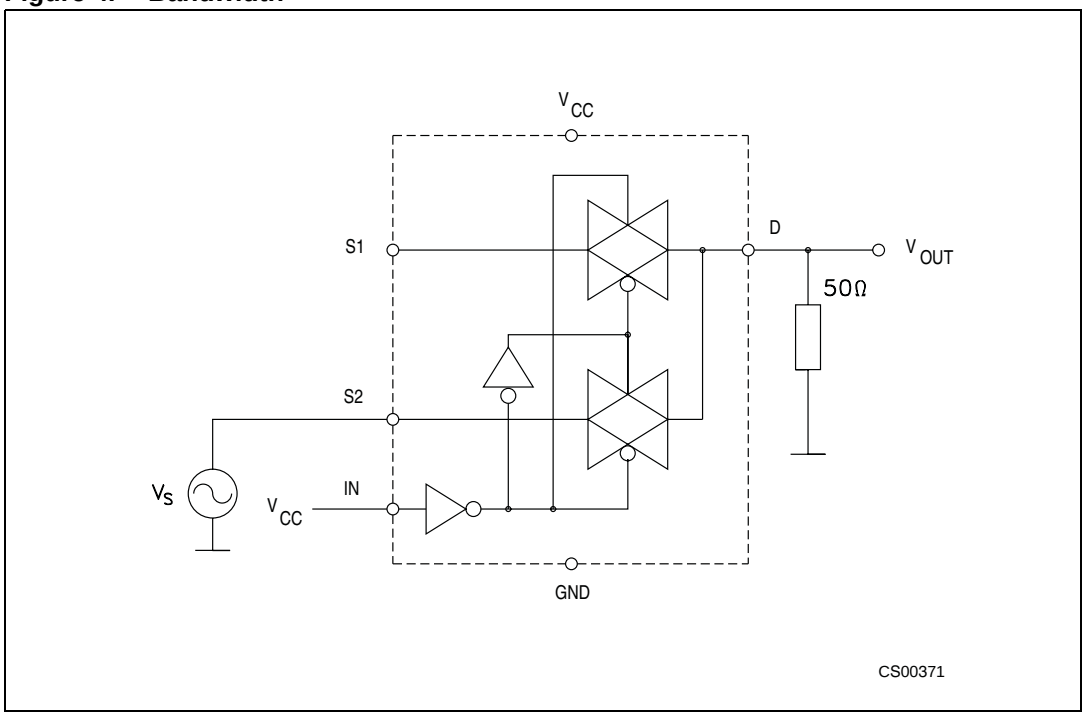


**Figure 5. OFF leakage**

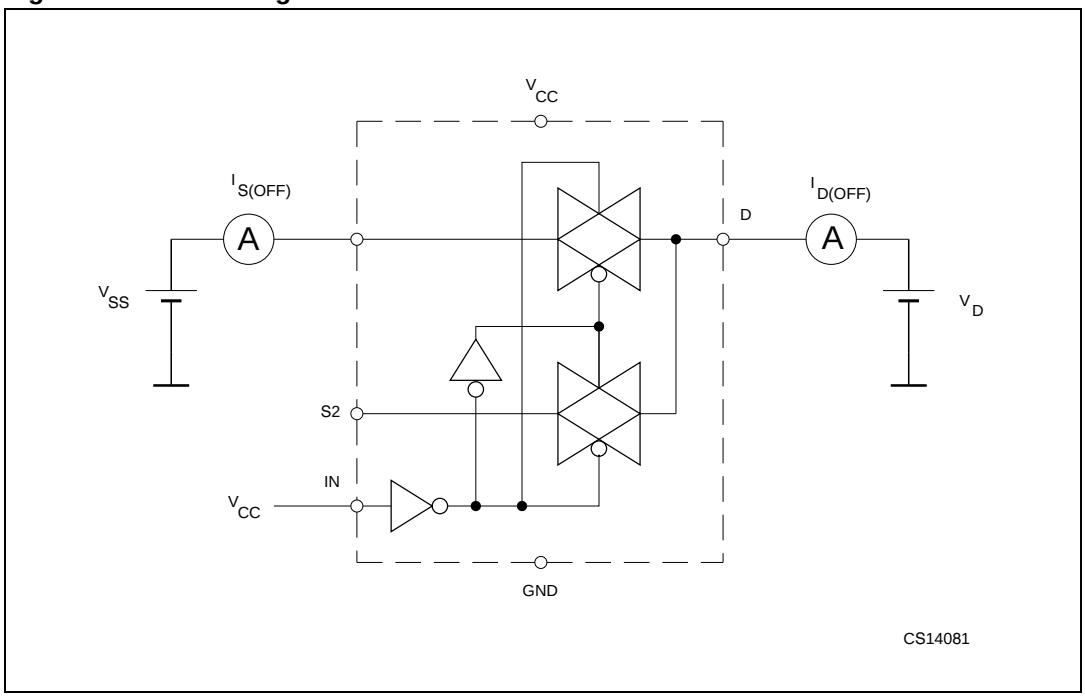



**Figure 6. Channel-to-channel crosstalk**

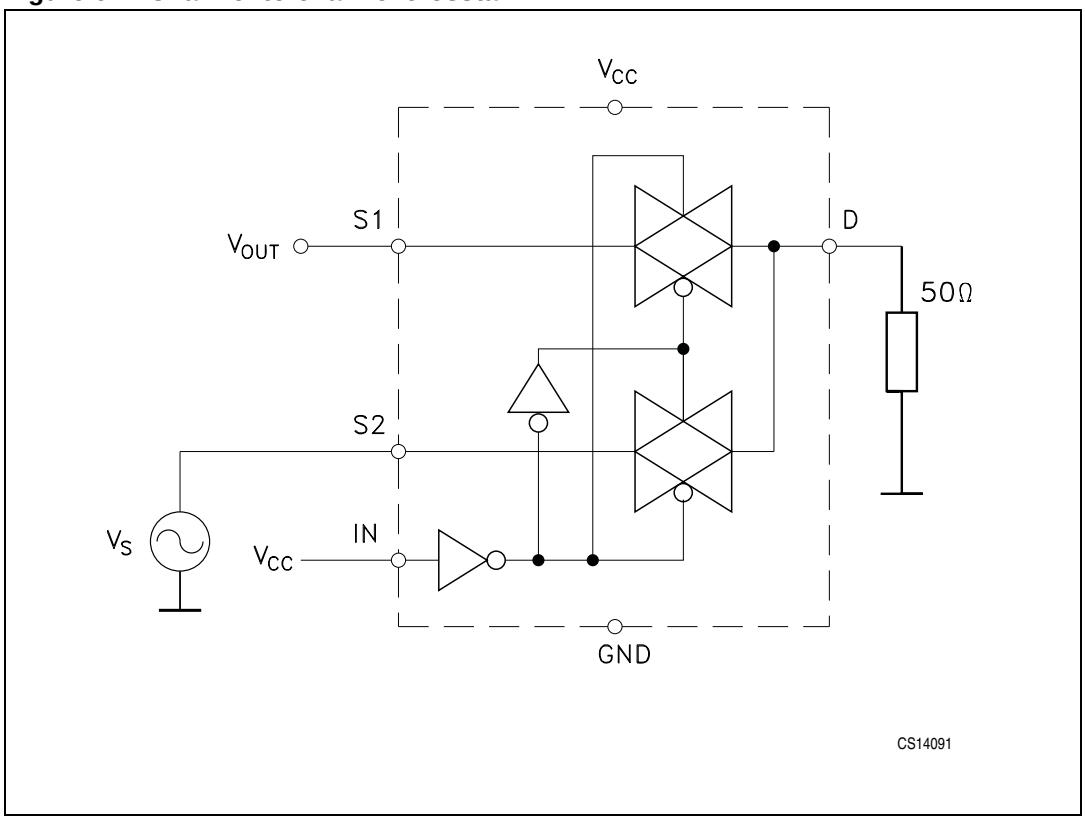


**Figure 7. OFF isolation**

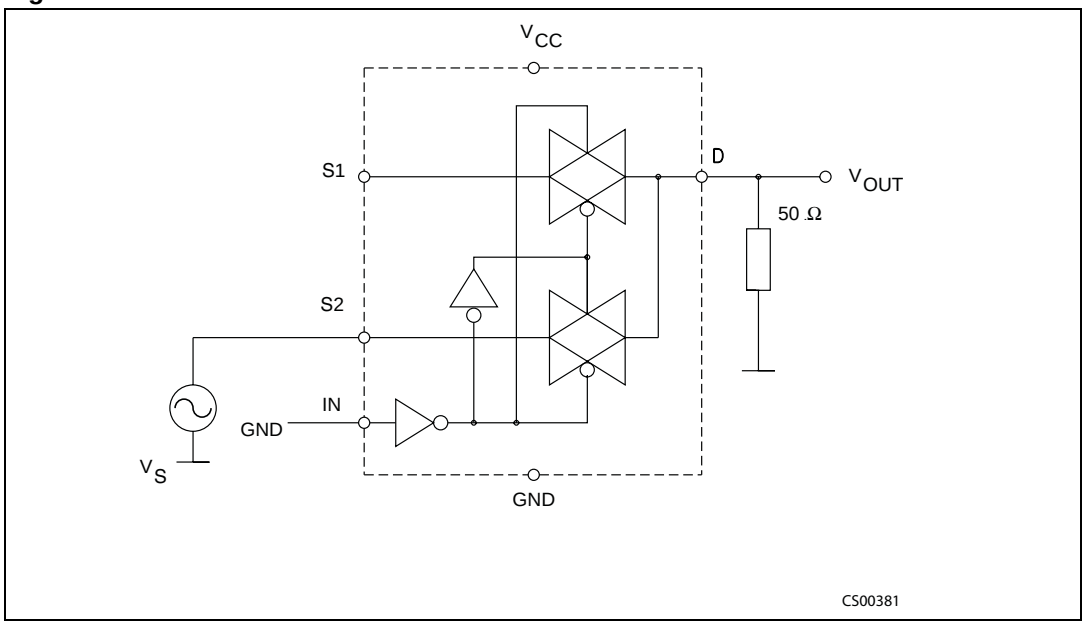
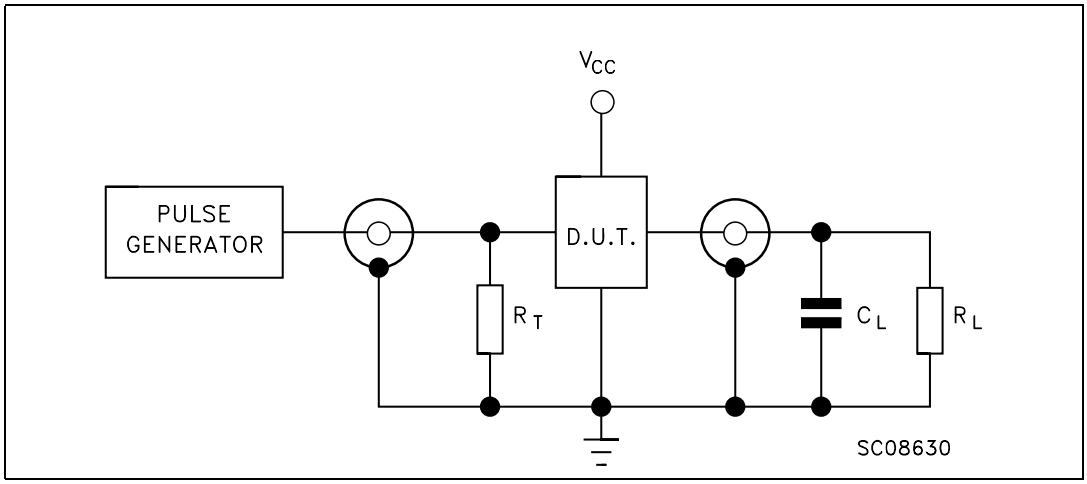



**Figure 8. Test circuit**




1. $C_L$ = 5/35 pF or equivalent: (includes jig capacitance)
2. $R_L$ = 50 Ω or equivalent
3. $R_T$ = $Z_{OUT}$ of pulse generator (typically 50 Ω)

**Figure 9. Break-before-make time delay**

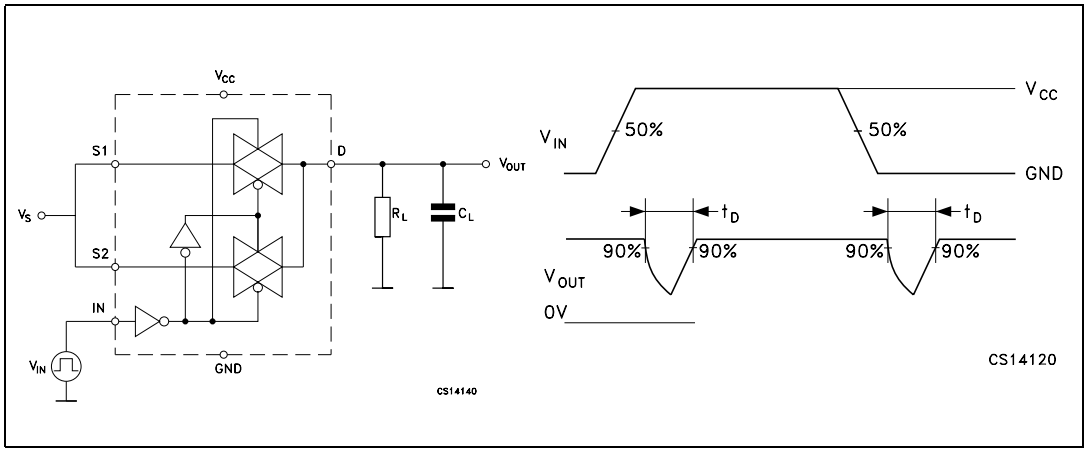



**Figure 10. Switching time and charge injection**
($V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω, $R_L$ = 1 MΩ, $C_L$ = 100 pF)

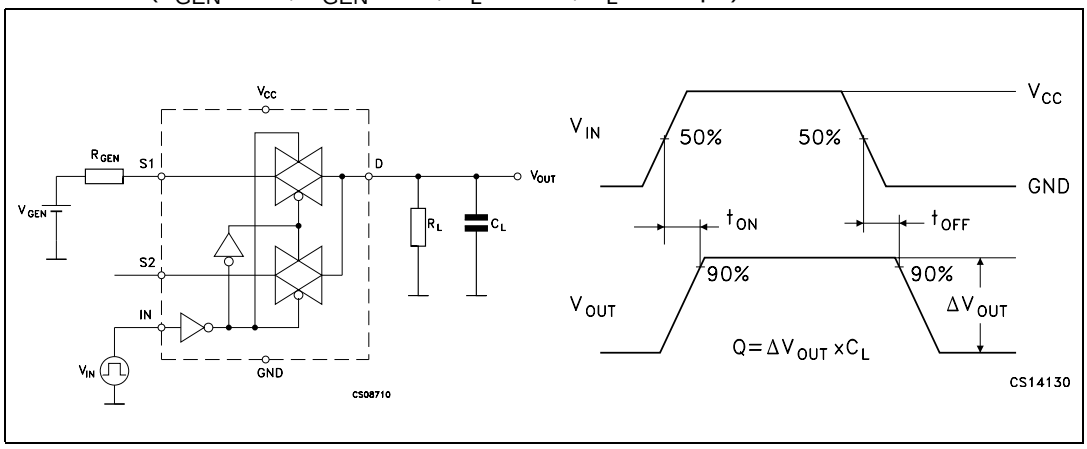
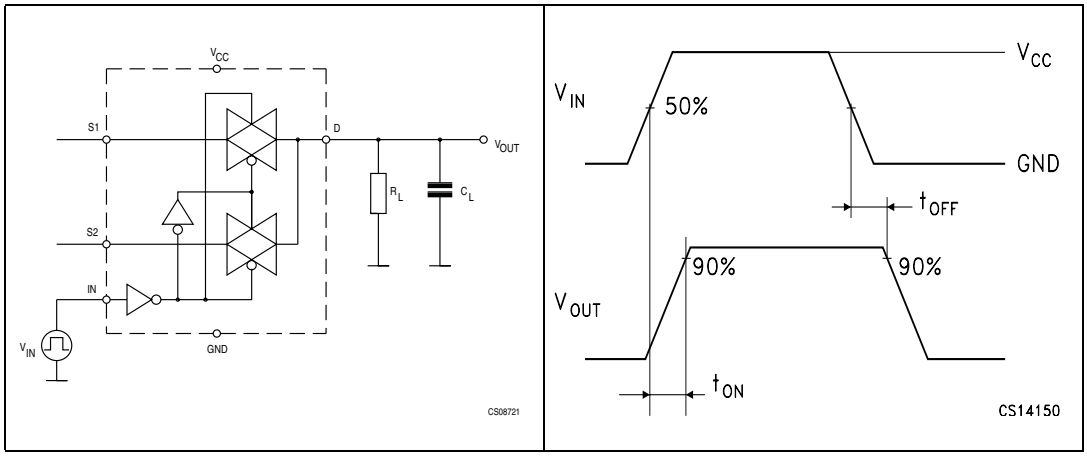


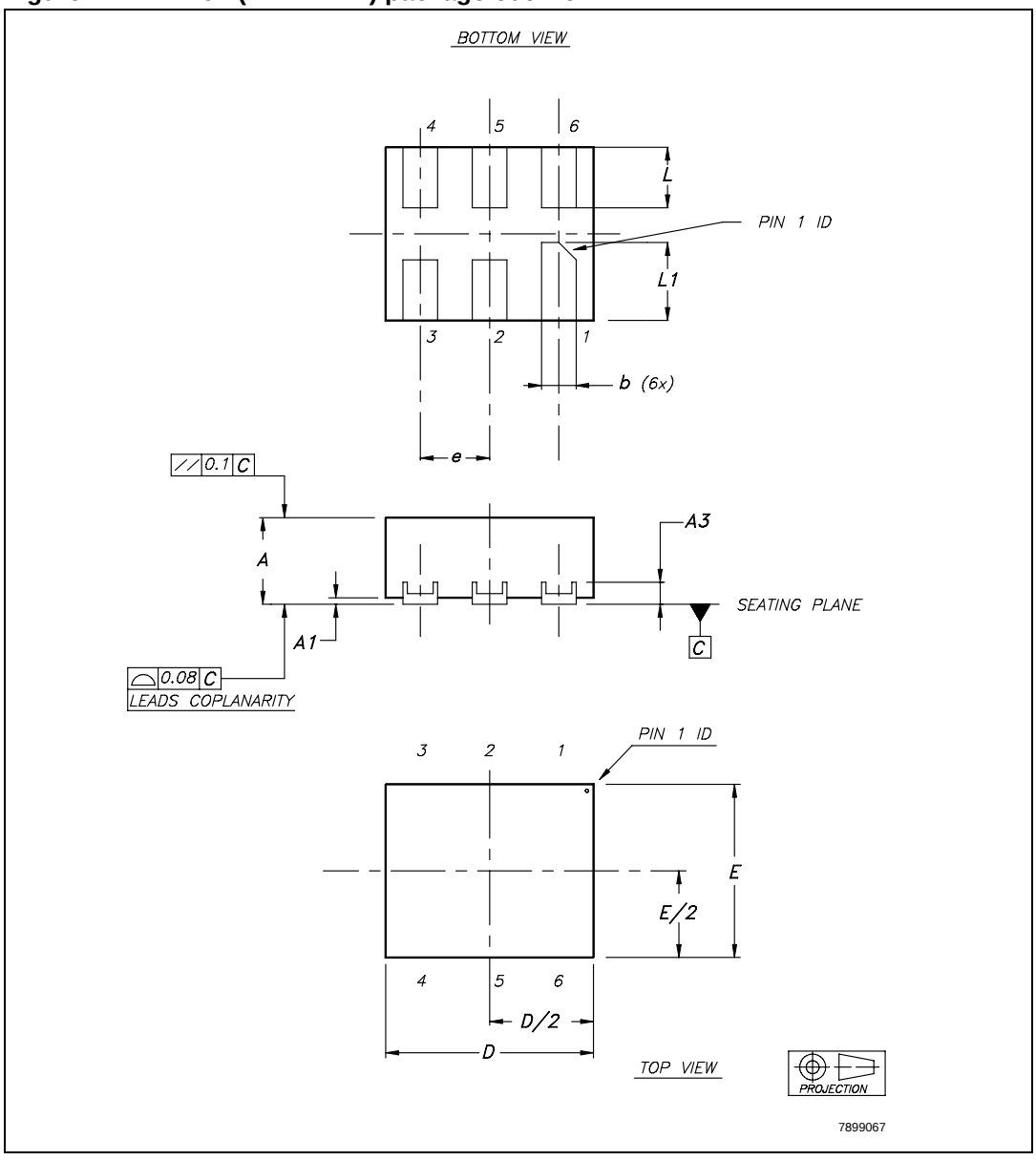

**Figure 11. Turn on, turn off delay time**



# 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 12. DFN6L (1.2 x 1mm) package outline**




1. Drawing not to scale.

**Table 8. DFN6L (1.2 x 1 mm) mechanical data**

| Symbol | millimeters | | |
|---|---|---|---|
| | Typ | Min | Max |
| A | 0.50 | 0.45 | 0.55 |
| A1 | 0.02 | 0 | 0.05 |
| A3 | 0.127 | | |
| b | 0.20 | 0.15 | 0.25 |
| D | 1.20 | 1.15 | 1.25 |
| E | 1 | 0.95 | 1.05 |
| e | 0.40 | | |
| L | 0.35 | 0.30 | 0.40 |
| L1 | 0.45 | 0.40 | 0.50 |

**Figure 13. DFN6L (1.2 x 1 mm) foot print recommendation**

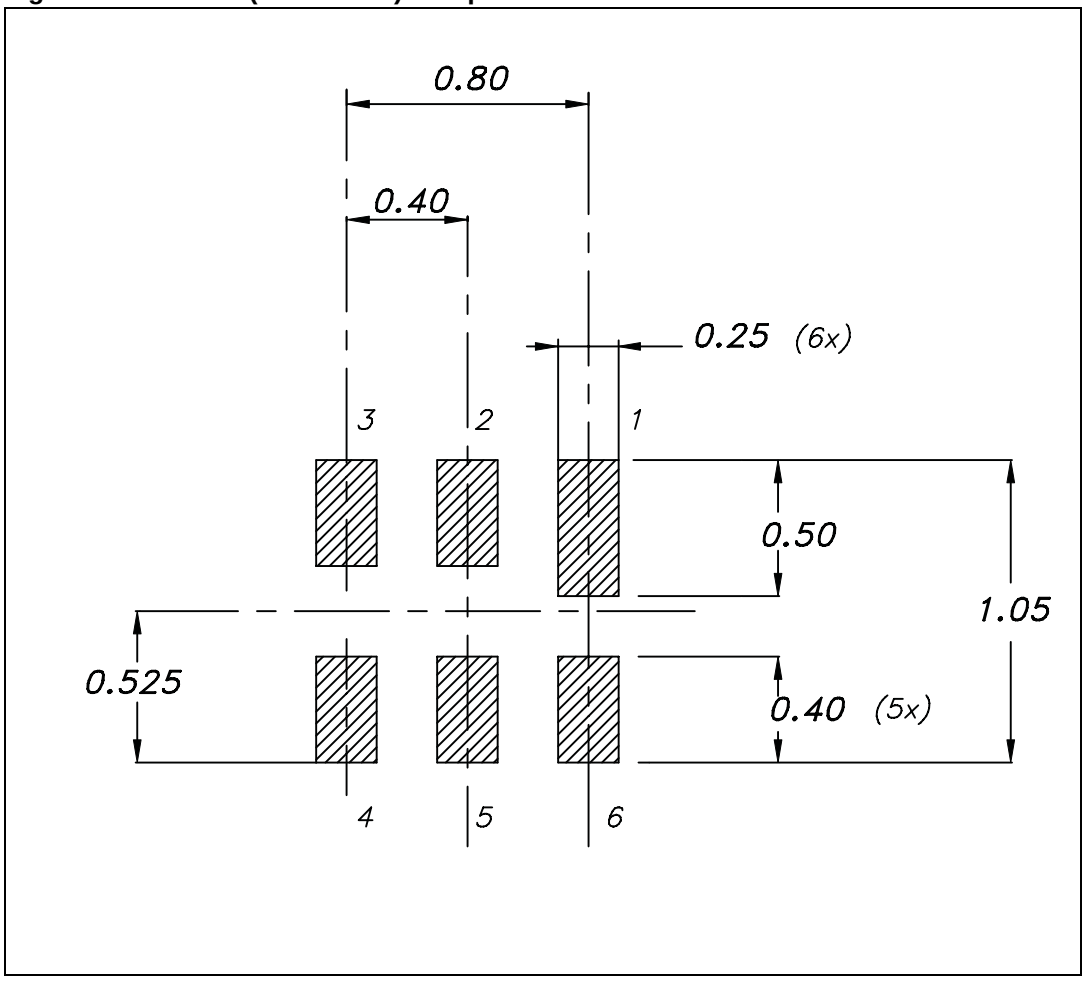
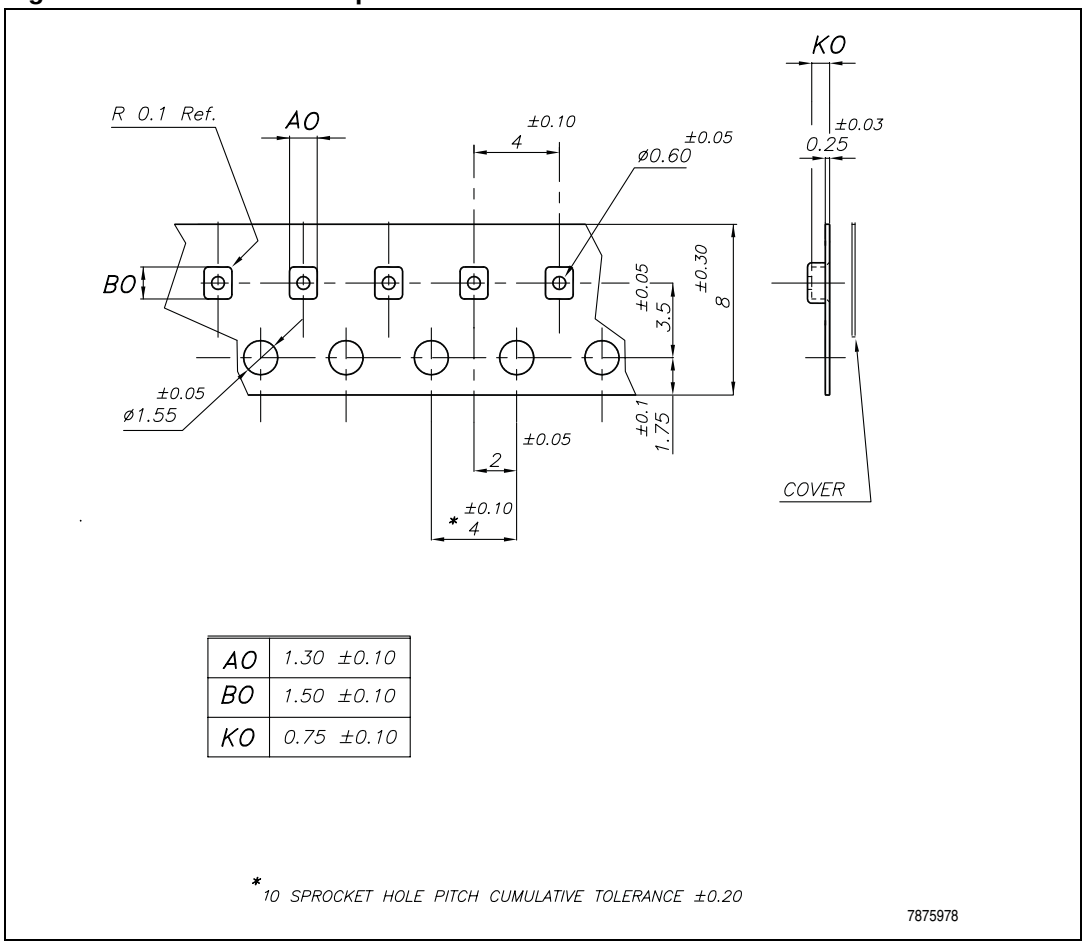
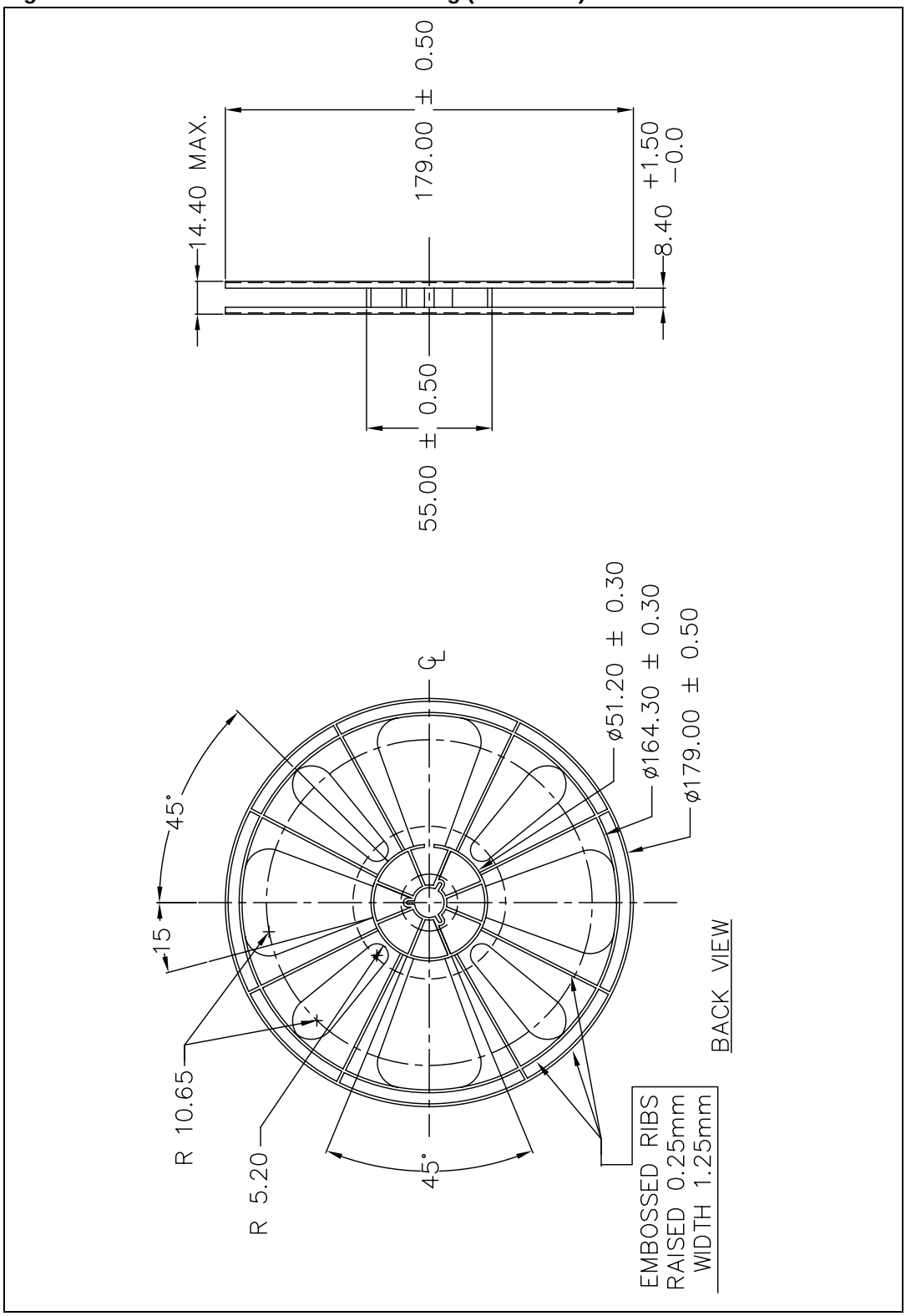


**Figure 14. DFN6L carrier tape information**



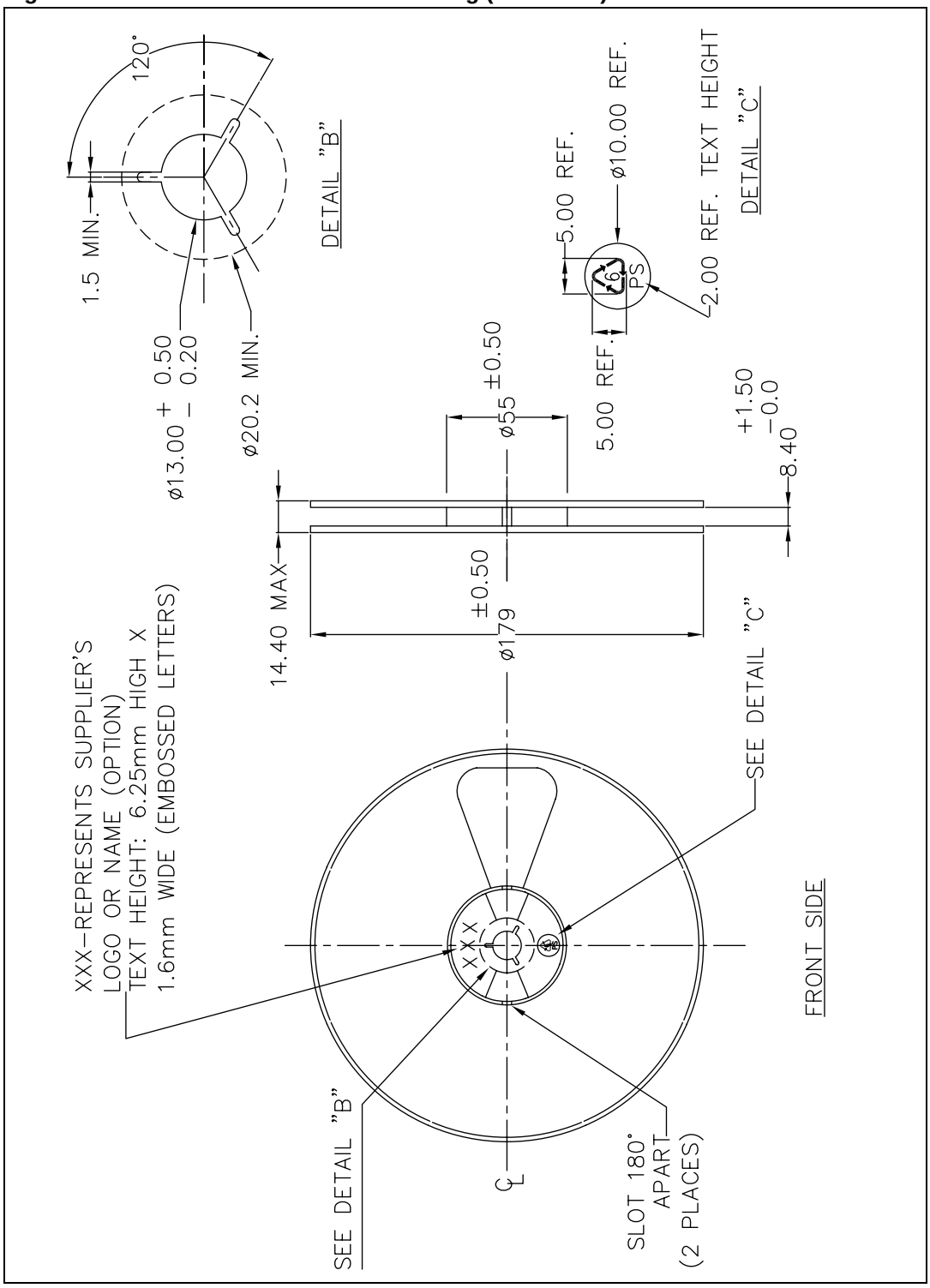

1. Drawing not to scale.
2. Dimensions are in millimeters.

**Figure 15. DFN6L reel information drawing (back view)**




1. Drawing not to scale.
2. Dimensions are in millimeters.

**Figure 16. DFN6L reel information drawing (front view)**




1. Drawing not to scale.
2. Dimensions are in millimeters.

# 6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 30-Oct-2007 | 1 | Initial release |

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