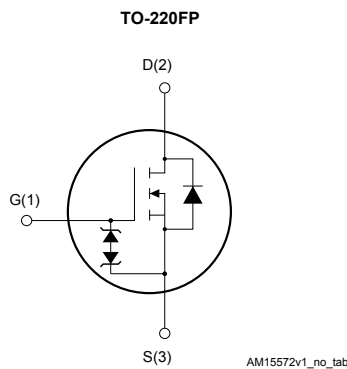
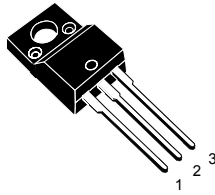


## N-channel 525 V, 1.25 $\Omega$ typ., 4.4 A, UltraFASTmesh™ Power MOSFET in a TO-220FP package



### Product status link

[STF5N52U](#)

### Product summary

<b>Order code</b>	STF5N52U
<b>Marking</b>	5N52U
<b>Package</b>	TO-220FP
<b>Packing</b>	Tube

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STF5N52U	525 V	1.50 $\Omega$	4.4 A	25 W

- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low  $R_{DS(on)}$
- Extremely low  $t_{rr}$

### Applications

- Switching applications

### Description

This device is N-channel Power MOSFET developed using UltraFASTmesh™ technology, which combines the advantages of reduced on resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4.4	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.8	
$I_{DM}^{(1)}$	Drain current (pulsed)	17.6	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	20	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}$ ; $T_C=25\text{ }^\circ\text{C}$ )	2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	2.8	kV

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 4.4\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{jmax}$ )	4.4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	170	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	525			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 525\text{ V}$			10	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 525\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}^{(1)}$			500	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2.2\text{ A}$		1.25	1.50	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance		-	529	-	pF
$C_{oss}$	Output capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	71	-	pF
$C_{rss}$	Reverse transfer capacitance		-	13.4	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 420\text{ V}$ , $V_{GS} = 0\text{ V}$	-	11	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 416\text{ V}$ , $I_D = 4.4\text{ A}$ , $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	16.9	-	nC
$Q_{gs}$	Gate-source charge		-	4.2	-	nC
$Q_{gd}$	Gate-drain charge		-	8.4	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260\text{ V}$ , $I_D = 2.2\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	11.4	-	ns
$t_r$	Rise time		-	13.6	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	23.1	-	
$t_f$	Fall time		-	15	-	

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		4.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		17.6	A
$V_{SD}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 4.4\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$	-	55		ns
$Q_{rr}$	Reverse recovery charge		-	95		nC
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	3.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	120		ns
$Q_{rr}$	Reverse recovery charge		-	266		nC
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4.5		A

1. Pulse width is limited by safe operating area
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ V}$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

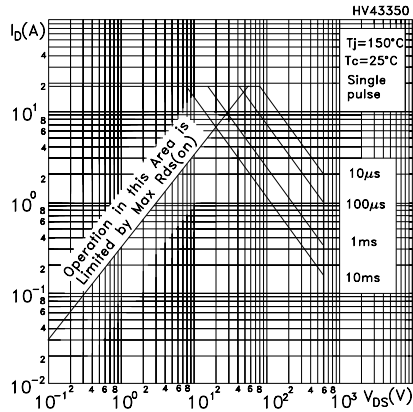


Figure 2. Thermal impedance

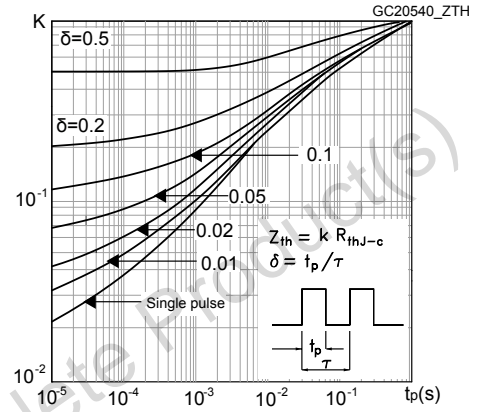


Figure 3. Output characteristics

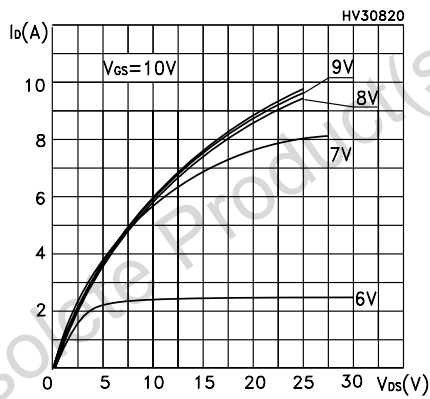


Figure 4. Transfer characteristics

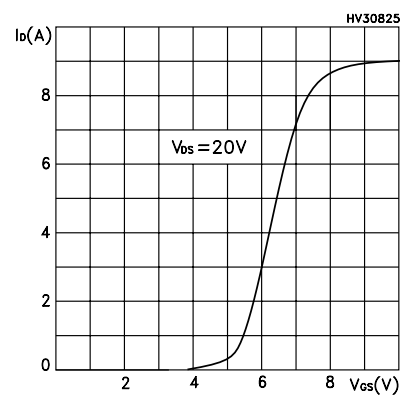


Figure 5. Normalized  $V_{(BR)DSS}$  vs temperature

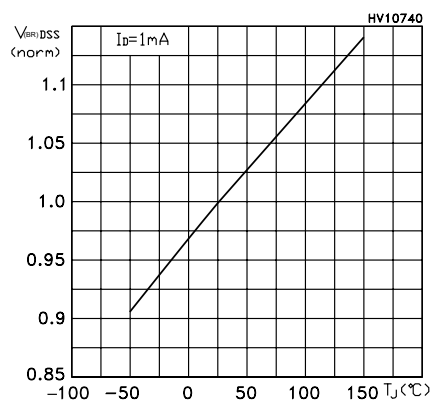
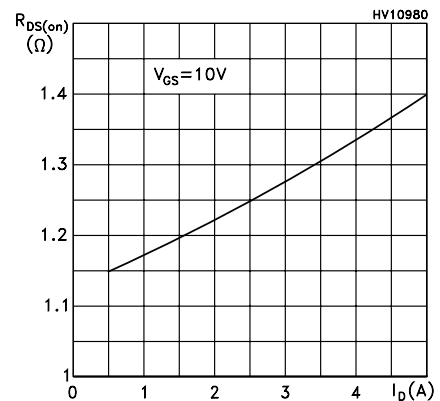
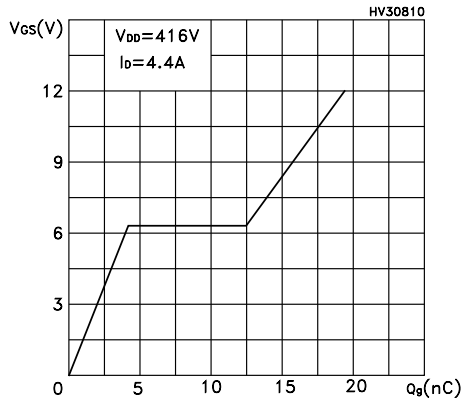
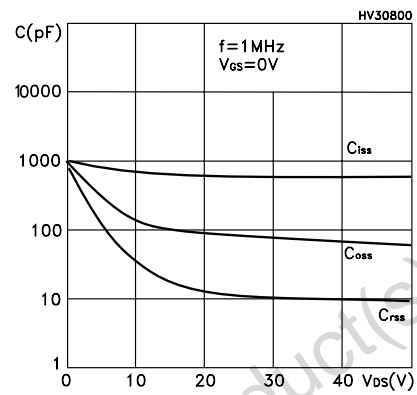
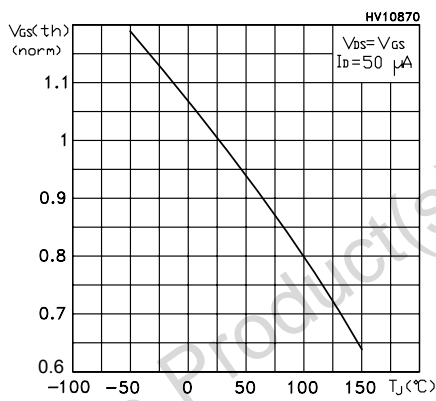
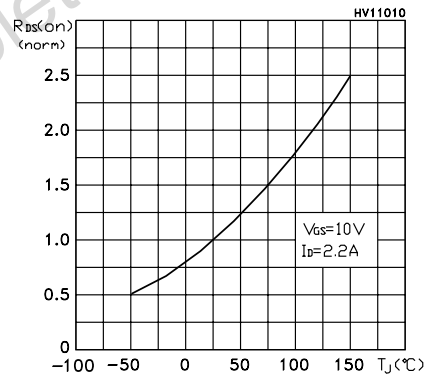
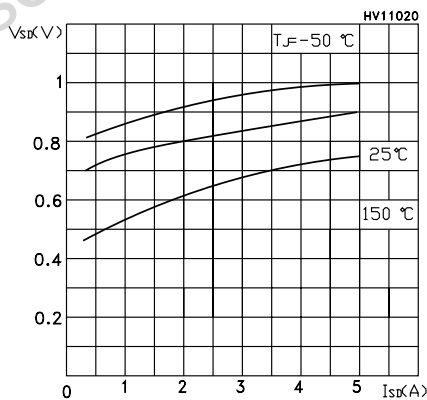
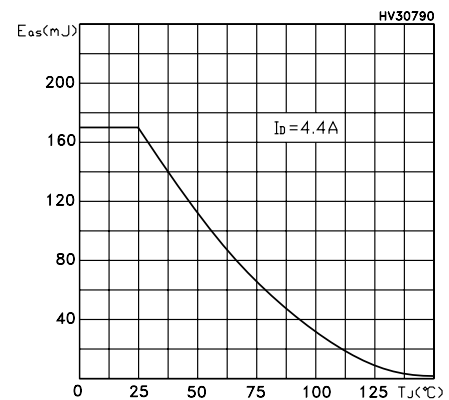


Figure 6. Static drain-source on-resistance

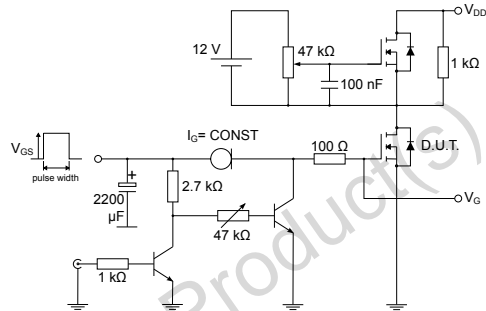


**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Capacitance variations**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Source-drain diode forward characteristics**

**Figure 12. Maximum avalanche energy vs temperature**


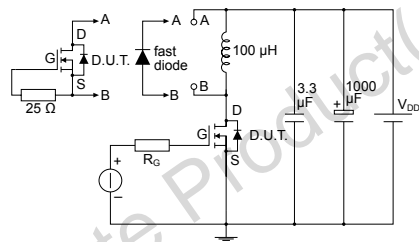
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

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## 4 Package information

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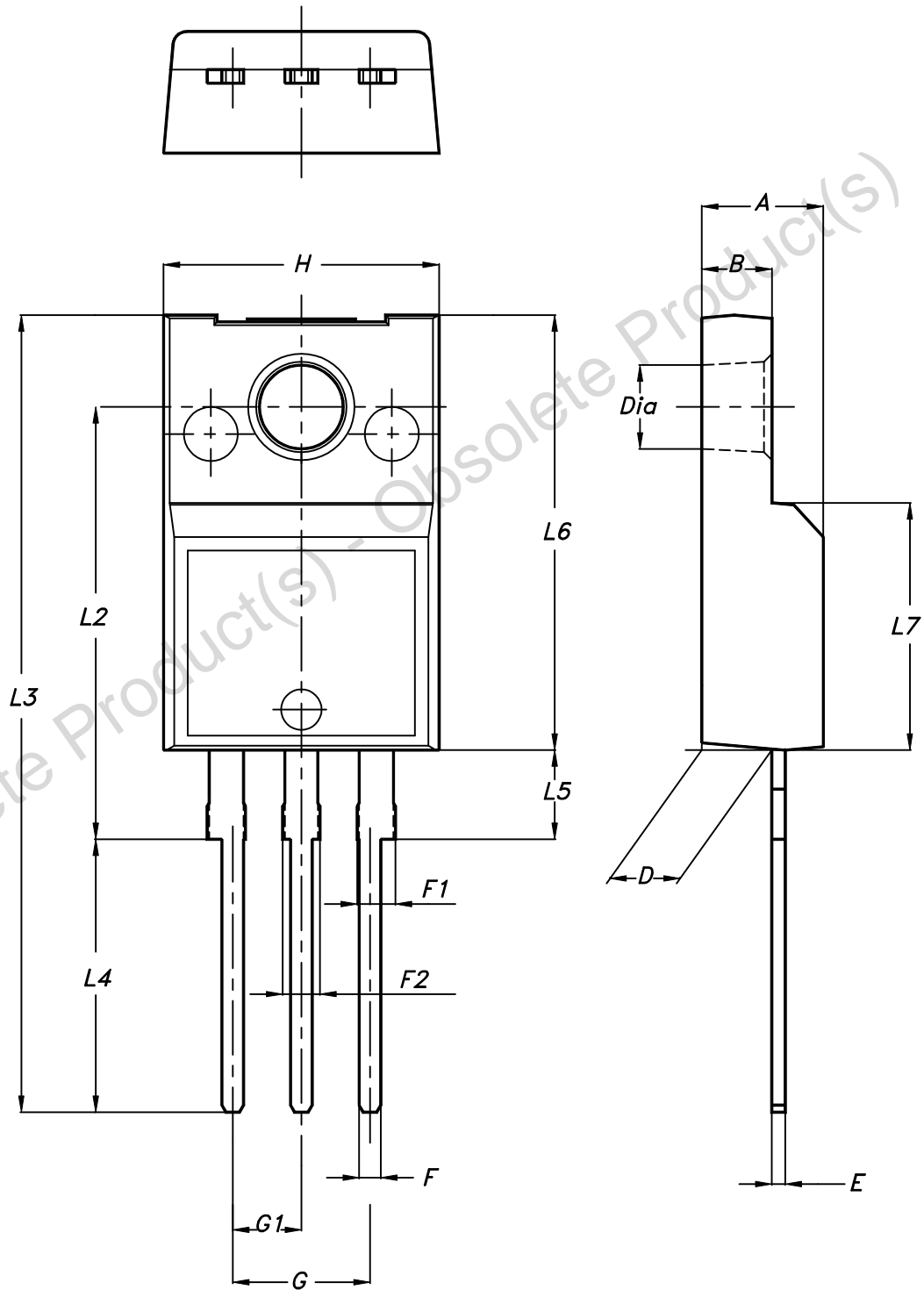
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### 4.1 TO-220FP package information

Figure 19. TO-220FP package outline



7012510\_Rev\_12\_B

Table 9. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
05-Mar-2019	1	First release. Part number previously included in datasheet DocID15684.

Obsolete Product(s) - Obsolete Product(s)

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