STB13N80K5, STF13N80K5, STP13N80K5, STW13N80K5

N-channel 800 V, 0.37 Ω typ., 12 A MDmesh™ K5 Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247

Datasheet - production data

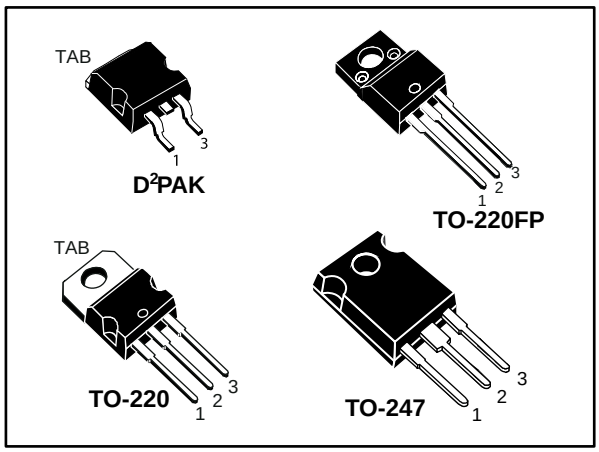
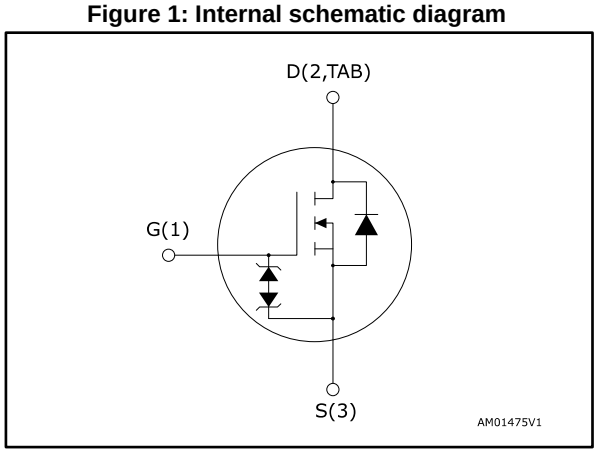


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB13N80K5	800 V	0.45 Ω	12 A	190 W
STF13N80K5				35 W
STP13N80K5				190 W
STW13N80K5				

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STB13N80K5	13N80K5	D²PAK	Tape and reel
STF13N80K5		TO-220FP	Tube
STP13N80K5		TO-220	
STW13N80K5		TO-247	

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D²PAK, TO-220, TO-247	TO-220FP	
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	12	12 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	7.6	7.6 (1)	A
I_{DM}(2)	Drain current (pulsed)	48	48 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	35	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat-sink (t = 1 s, T_C = 25 °C)		2500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50		
T_j	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

Notes:

(1)Limited by package.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 12 A, di/dt =100 A/µs; V_{DS} peak < $V_{(BR)DSS}$.

(4)V_{DS} ≤ 640 V.

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		D²PAK	TO-220	TO-220FP	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.66		3.57	0.66	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5		50	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	30				°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	148	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 ° C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DD} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.37	0.45	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	870	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	110	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	43	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D= 0 A	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 2.5 A V_{GS}= 0 to 10 V (see *Figure 22: "Test circuit for gate charge behavior"*)	-	29	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

Notes:

(1)$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 400 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 21: "Test circuit for resistive load switching times"* and *Figure 26: "Switching time waveform"*)	-	16	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	16	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
I_{SDM}(1)	Source-drain current (pulsed)		-		56	A
V_{SD}(2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 23: "Test circuit for inductive load switching and diode recovery times"*)	-	406		ns
Q_{rr}	Reverse recovery charge		-	5.7		µC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD}= 60 V, T_j= 150 °C (see *Figure 23: "Test circuit for inductive load switching and diode recovery times"*)	-	600		ns
Q_{rr}	Reverse recovery charge		-	7.9		µC
I_{RRM}	Reverse recovery current		-	26		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ±1 mA, I_D= 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for D²PAK

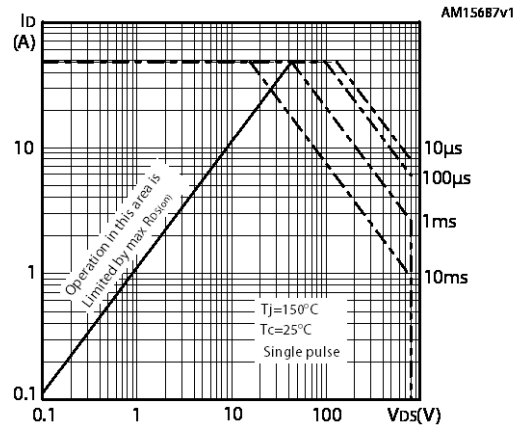


Figure 3: Thermal impedance for D²PAK

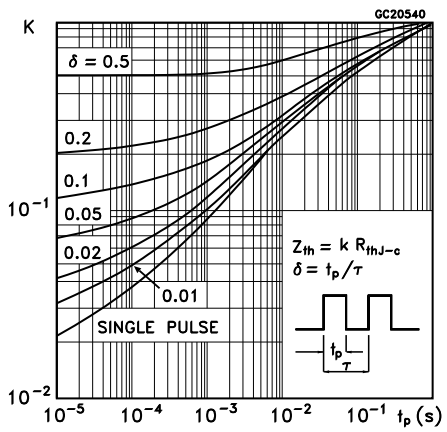


Figure 4: Safe operating area for TO-220FP

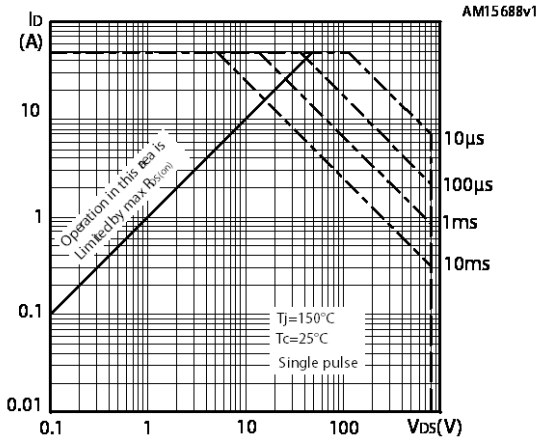


Figure 5: Thermal impedance for TO-220FP

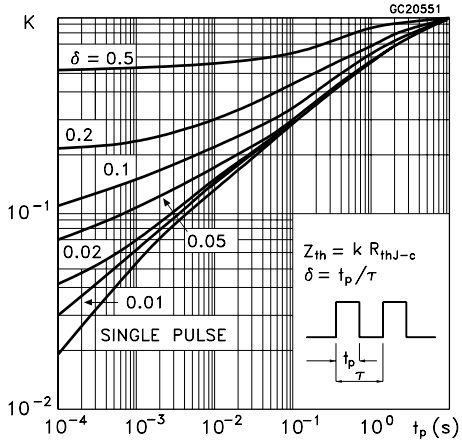


Figure 6: Safe operating area for TO-220

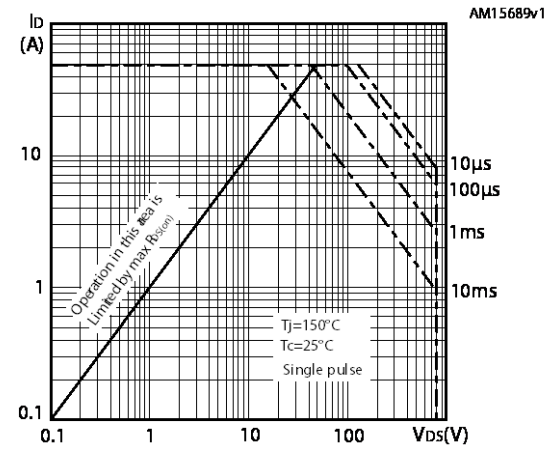


Figure 7: Thermal impedance for TO-220

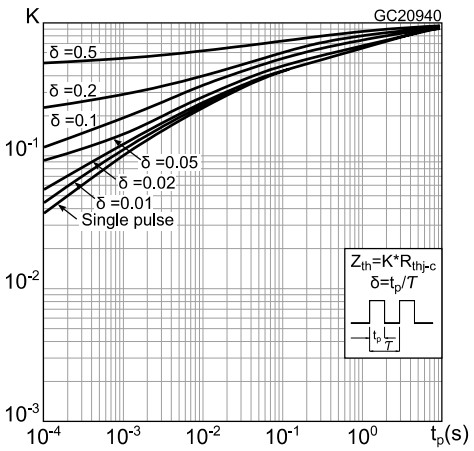


Figure 8: Safe operating area for TO-247

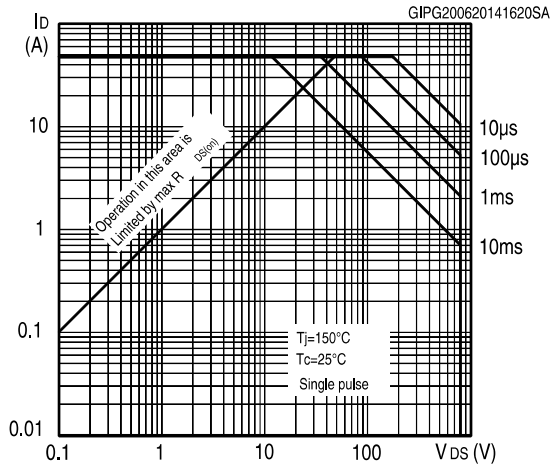


Figure 9: Thermal impedance for TO-247

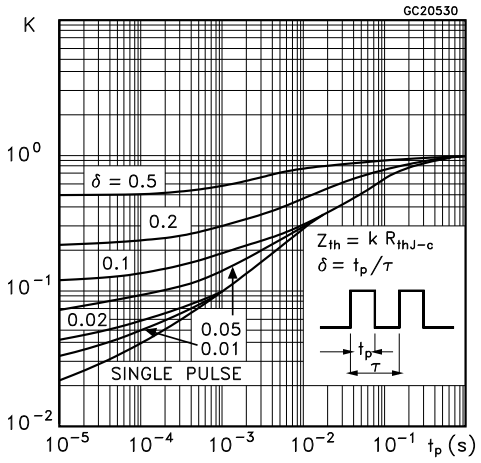


Figure 10: Output characteristics

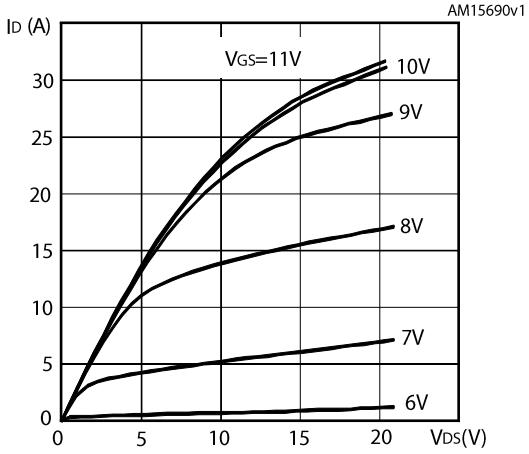


Figure 11: Transfer characteristics

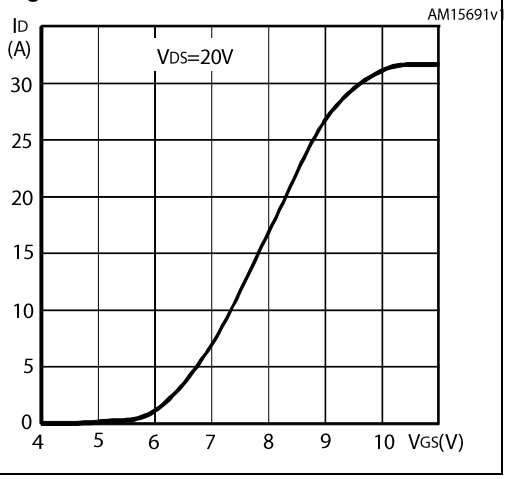


Figure 12: Gate charge vs gate-source voltage

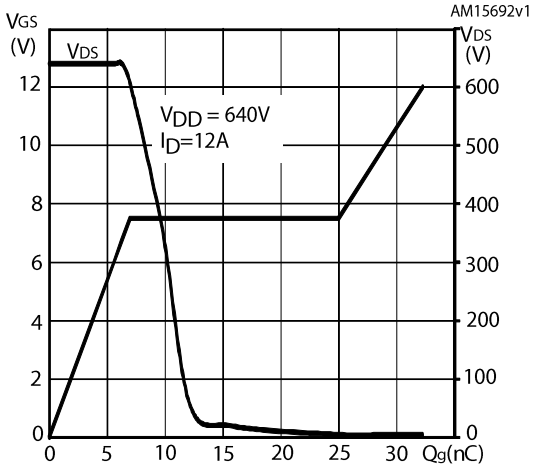


Figure 13: Static drain-source on-resistance

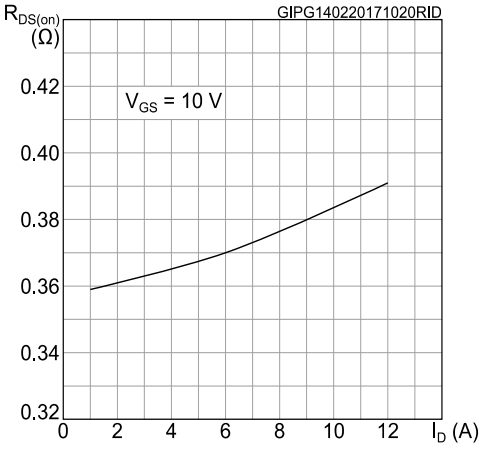


Figure 14: Capacitance variations

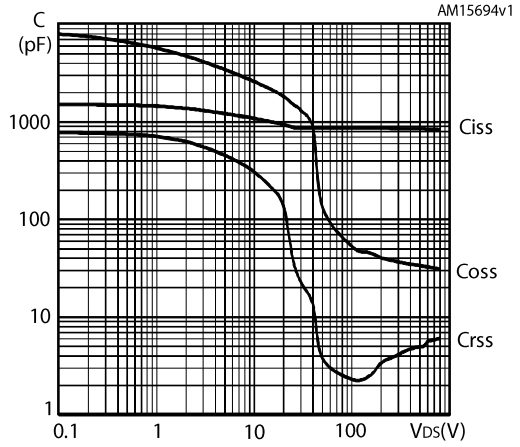


Figure 15: Output capacitance stored energy

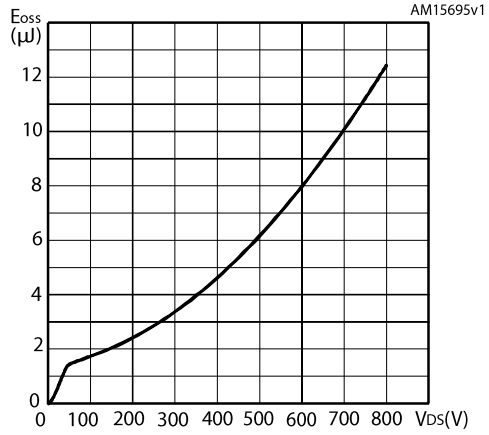


Figure 16: Normalized gate threshold voltage vs temperature

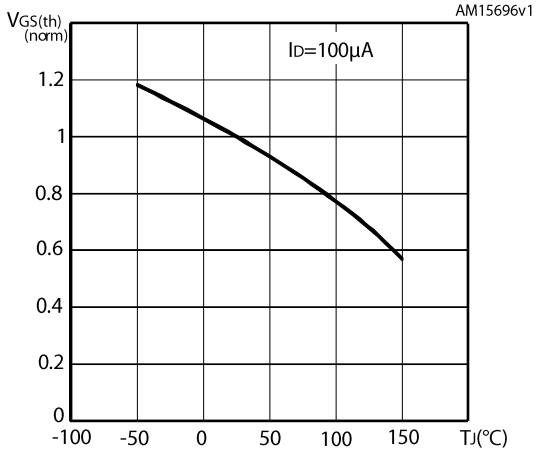


Figure 17: Normalized on-resistance vs temperature

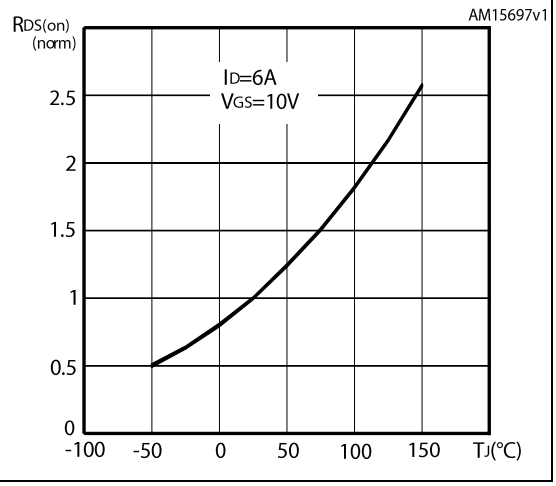


Figure 18: Normalized $V_{(BR)DSS}$ vs temperature

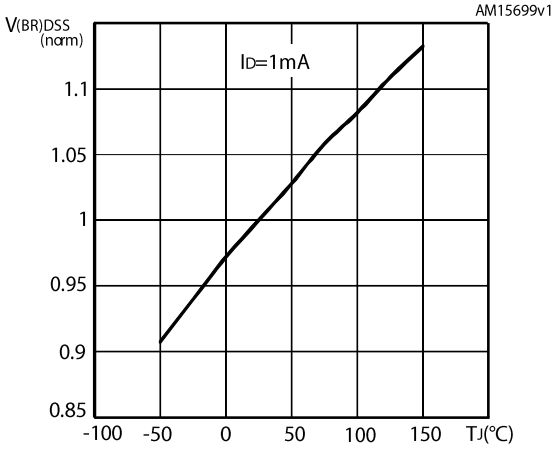


Figure 19: Source-drain diode forward characteristics

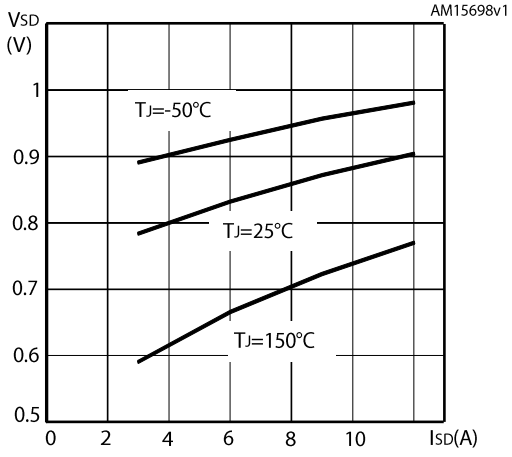
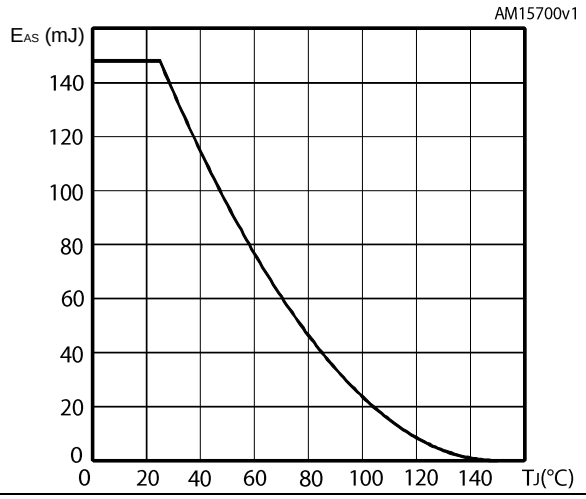


Figure 20: Maximum avalanche energy vs. starting T_j



3 Test circuits

Figure 21: Test circuit for resistive load switching times

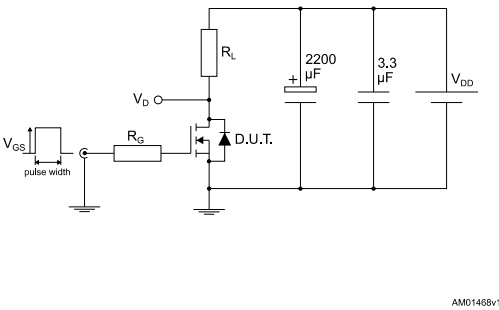


Figure 22: Test circuit for gate charge behavior

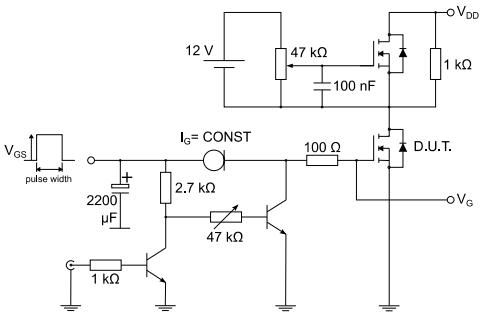


Figure 23: Test circuit for inductive load switching and diode recovery times

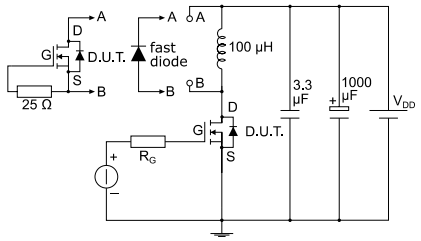


Figure 24: Unclamped inductive load test circuit

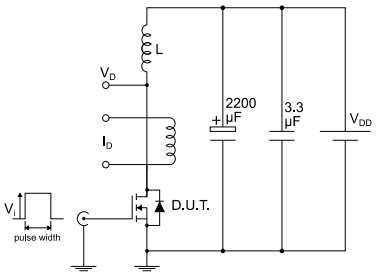


Figure 25: Unclamped inductive waveform

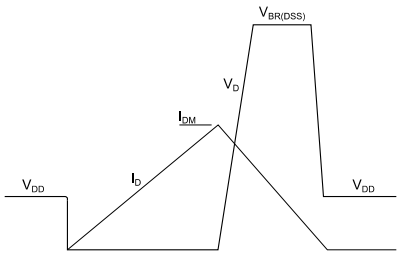
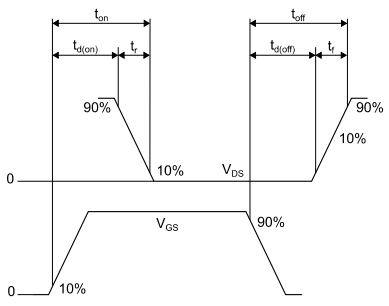


Figure 26: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 27: D²PAK (TO-263) type A package outline

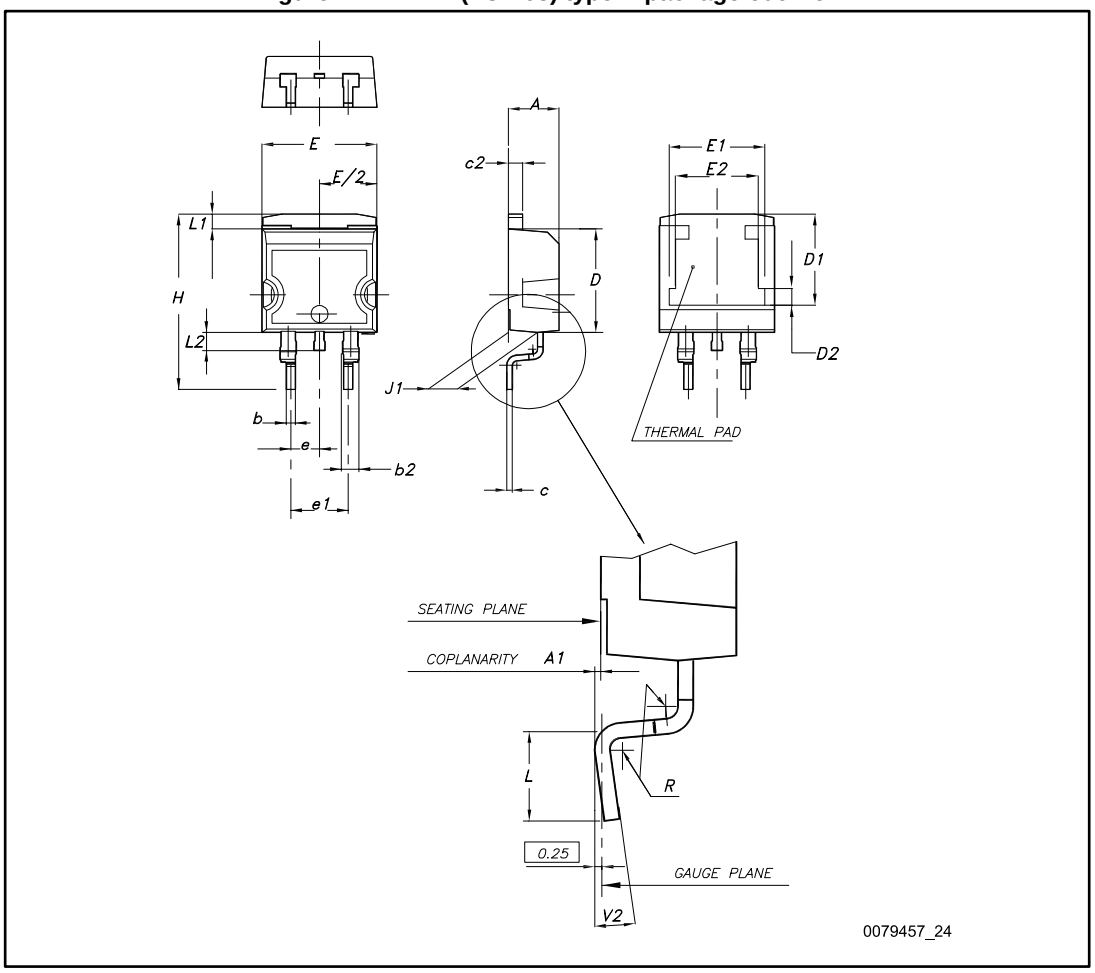
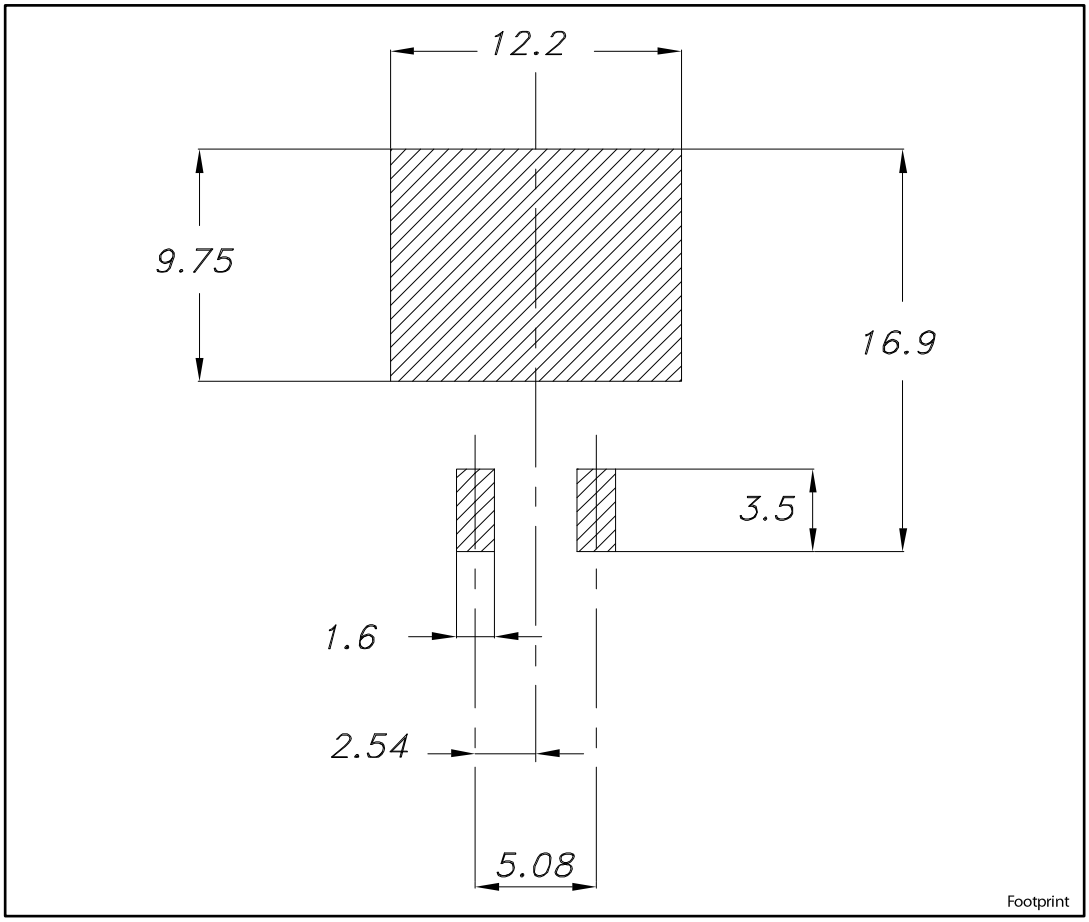


Table 10: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 28: D²PAK (TO-263) type A recommended footprint (dimensions are in mm)



4.2 TO-220FP package information

Figure 29: TO-220FP package outline

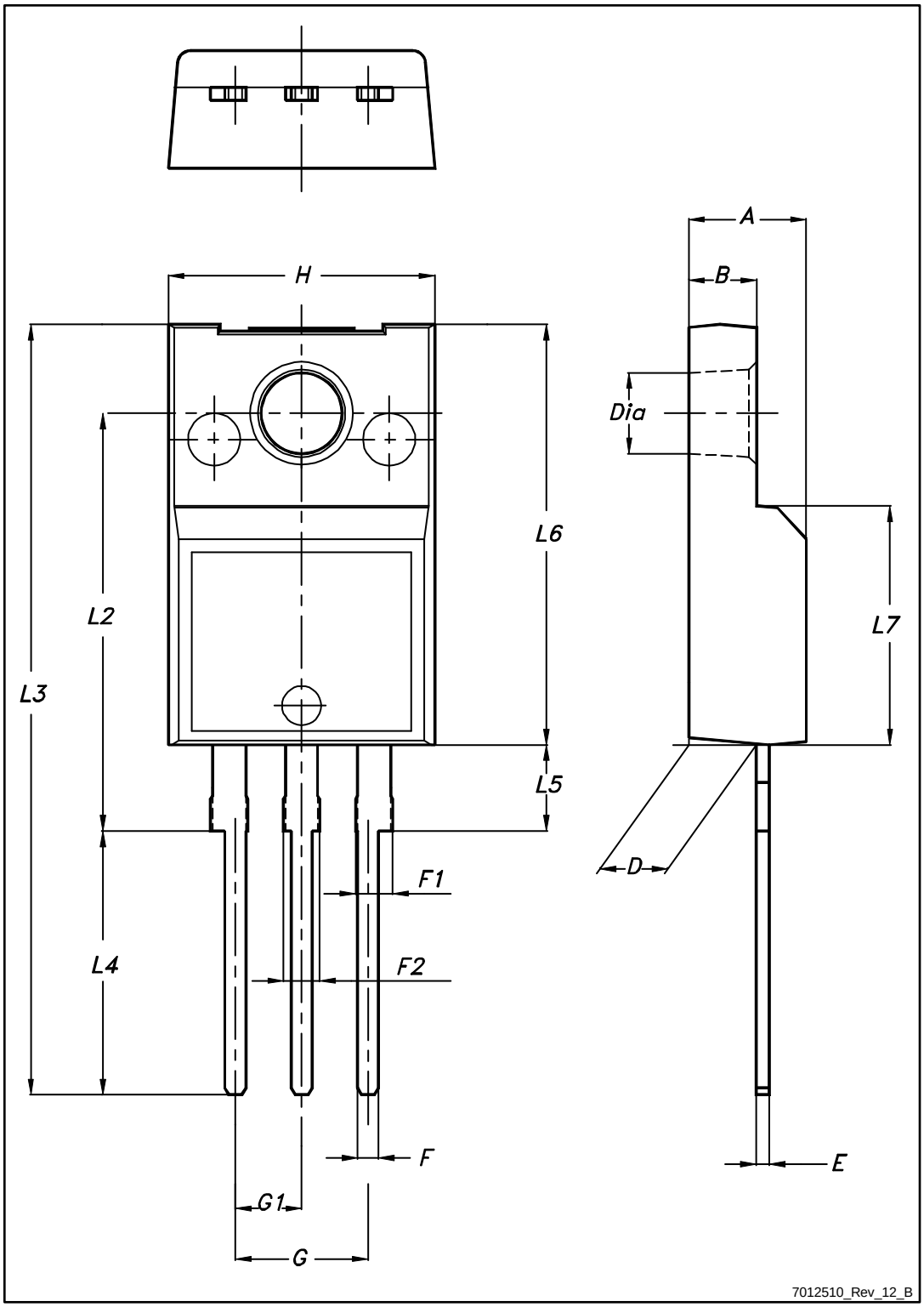


Table 11: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.3 TO-220 type A packing information

Figure 30: TO-220 type A package outline

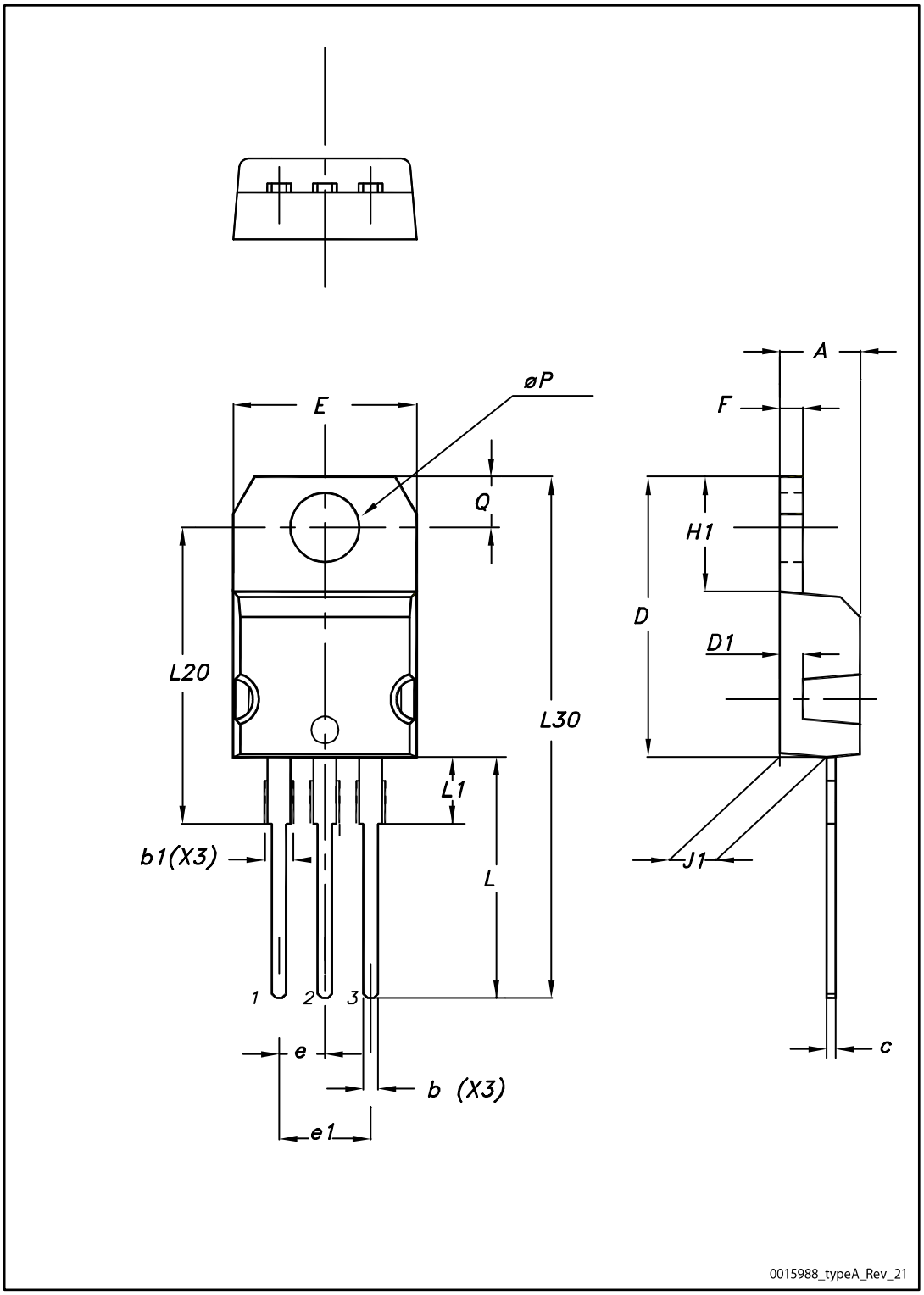


Table 12: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 TO-247 package information

Figure 31: TO-247 package outline

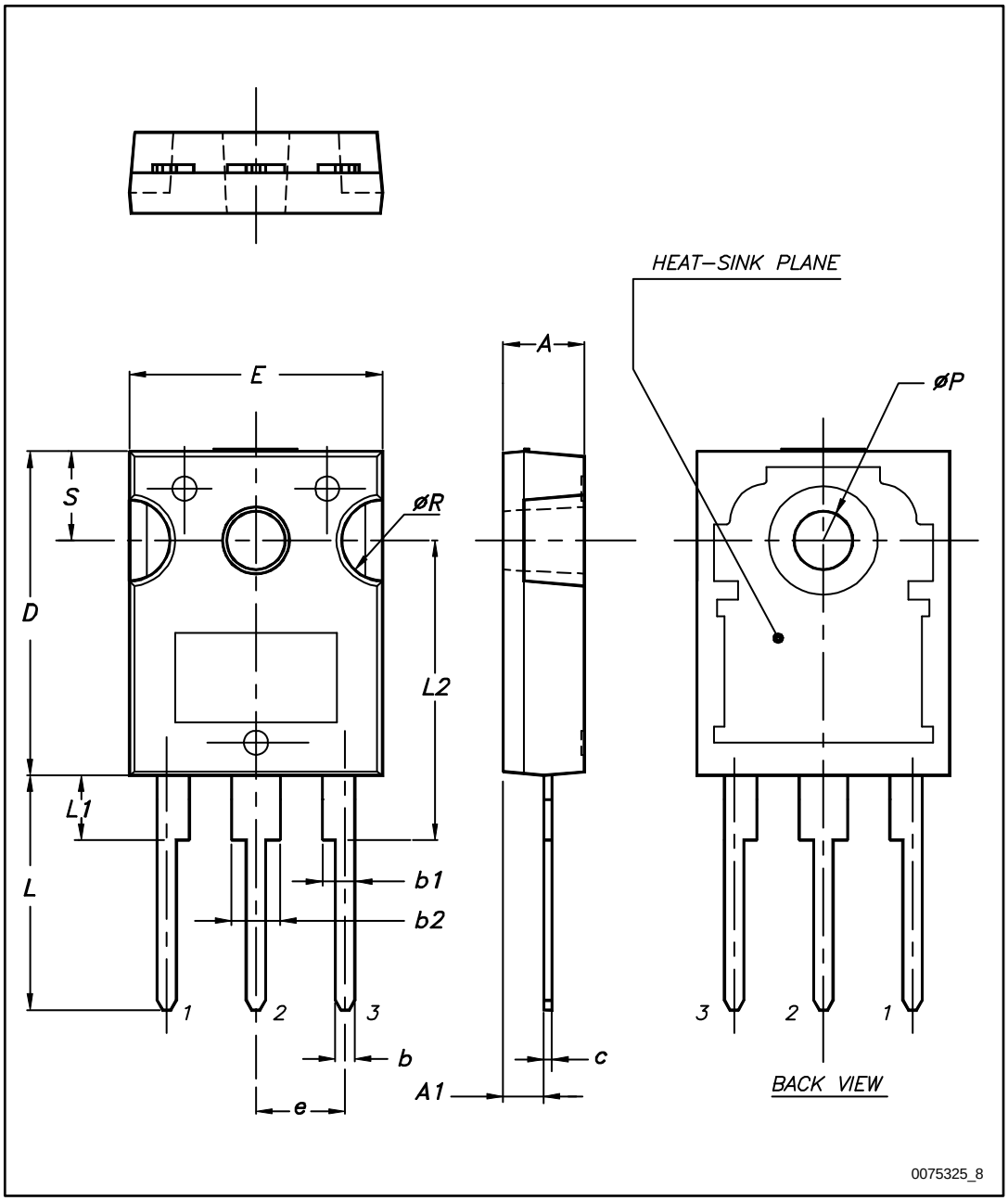


Table 13: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.5 D²PAK type A packing information

Figure 32: D²PAK type A tape outline

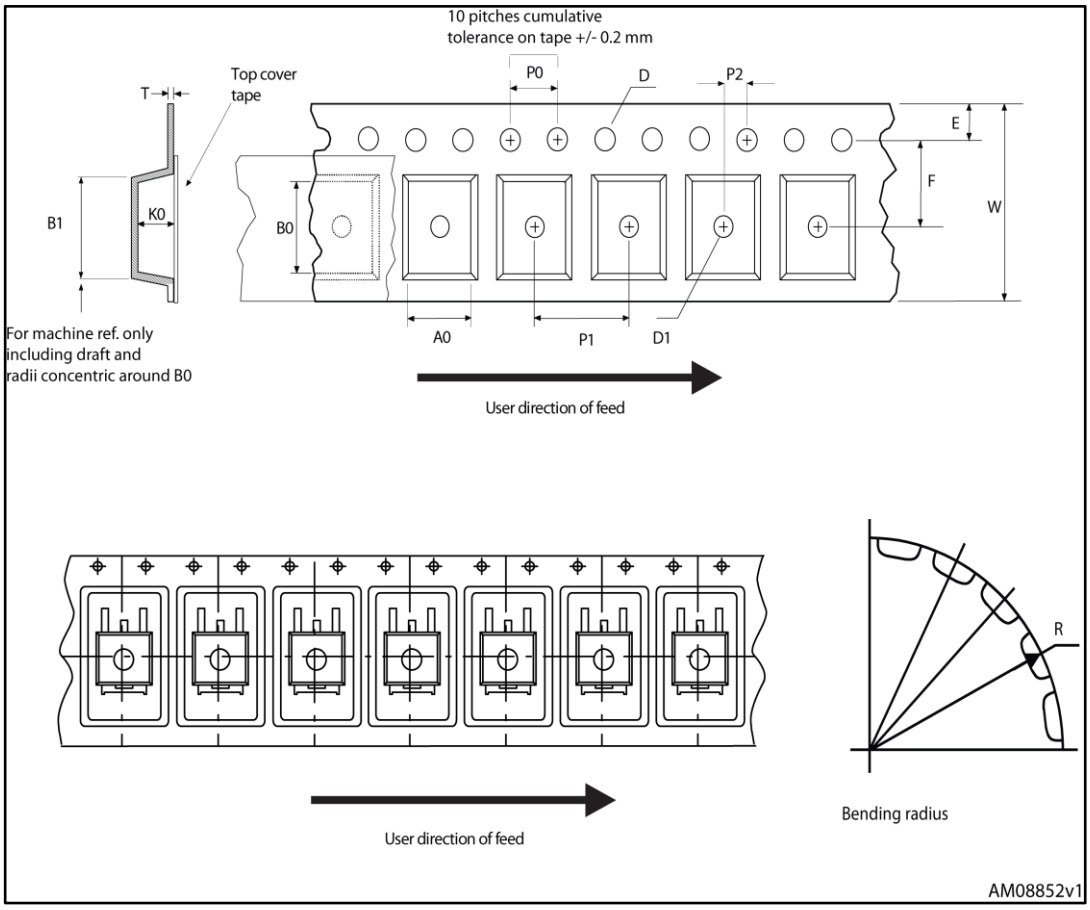


Figure 33: D²PAK type A reel outline

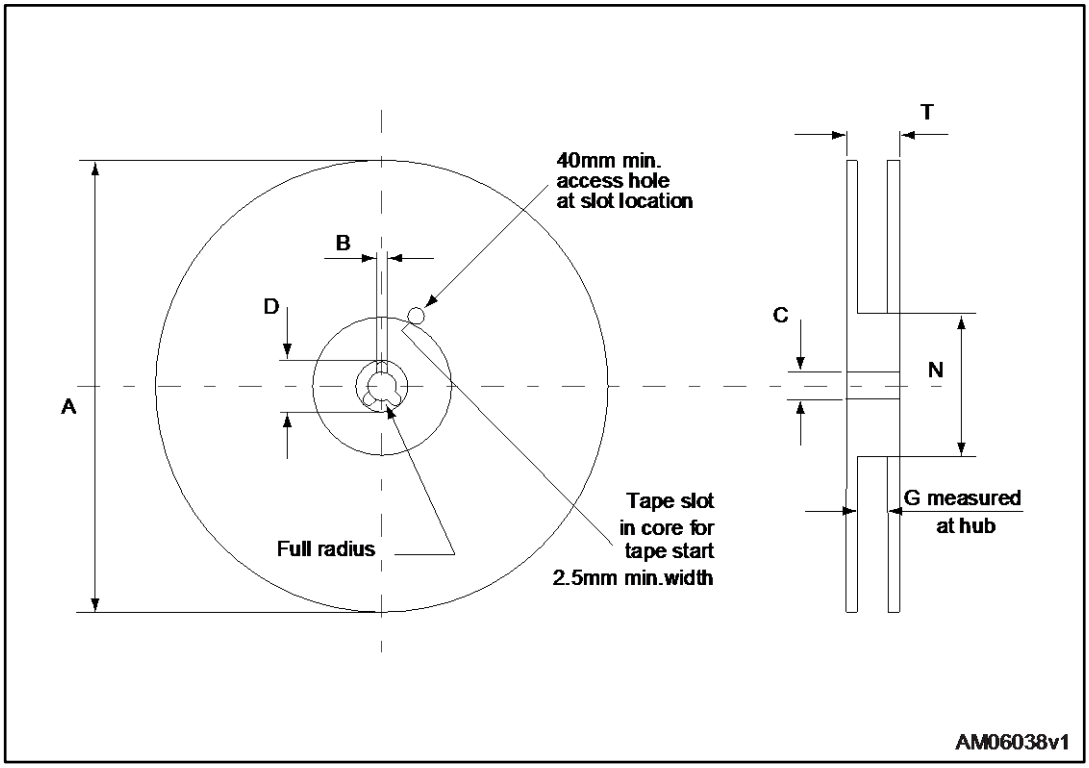


Table 14: D²PAK type A tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 15: Document revision history

Date	Revision	Changes
07-Mar-2013	1	First release.
27-Mar-2013	2	Updated Figure 1: Internal schematic diagram. Minor text changes. Document status promoted from preliminary data to production data.
15-Apr-2013	3	– Modified: E_{AS} value, the entire typical values on *Table 5, 6* and *7* – Inserted: *Section 2.1: Electrical characteristics (curves)* – Minor text changes
25-Sep-2017	4	Added: TO-247 package. Updated title, features and description. Updated *Figure 13: "Static drain-source on-resistance"*. Updated *Table 2: "Absolute maximum ratings"*, *Table 5: "On/off-state"*, *Table 6: "Dynamic"* and *Table 8: "Source-drain diode"*. Added *Figure 8: "Safe operating area for TO-247"* and *Figure 9: "Thermal impedance for TO-247"*. Updated *Section 4.4: "TO-247 package information".* Minor text changes.

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