

## N-channel 400 V, 0.59 $\Omega$ typ., 6 A MDmesh II Plus™ low $Q_g$ Power MOSFET in a DPAK package

Datasheet - preliminary data

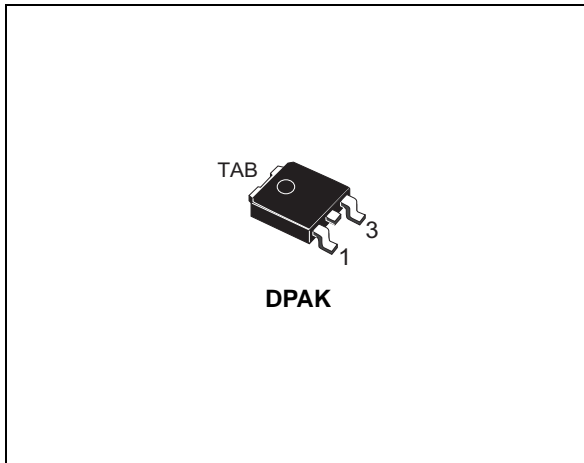
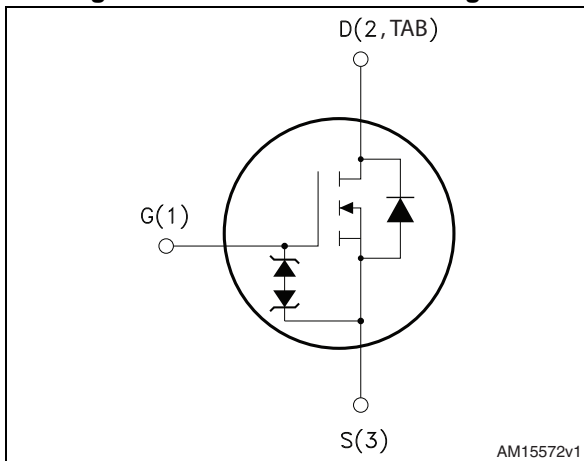


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STD9N40M2	450 V	0.8 $\Omega$	6 A

- Extremely low gate charge
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD9N40M2	9N40M2	DPAK	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	400	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$dv/dt^{(1)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(2)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

- $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD}=320\text{ V}$
- $V_{DS} \leq 320\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max <sup>(1)</sup>	50	$^\circ\text{C}/\text{W}$

- When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50$ )	148	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	400			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 400\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 400\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		0.59	0.8	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	270	-	pF
$C_{oss}$	Output capacitance		-	22	-	pF
$C_{riss}$	Reverse transfer capacitance		-	0.7	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }320\text{ V}$	-	94	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	7.1	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 320\text{ V}, I_D = 6\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	8.8	-	nC
$Q_{gs}$	Gate-source charge		-	1.7	-	nC
$Q_{gd}$	Gate-drain charge		-	4.8	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}, I_D = 3\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> and <a href="#">19</a> )	-	10.5	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	7.5	-	ns
$t_f$	Fall time		-	21	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0, I_{SD} = 6 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 16</a> )	-	208		ns
$Q_{rr}$	Reverse recovery charge		-	1.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	11.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	264		ns
$Q_{rr}$	Reverse recovery charge		-	1.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	12.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

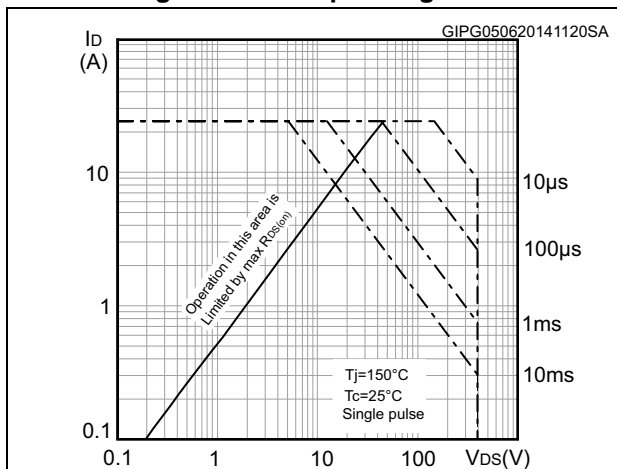


Figure 3. Thermal impedance

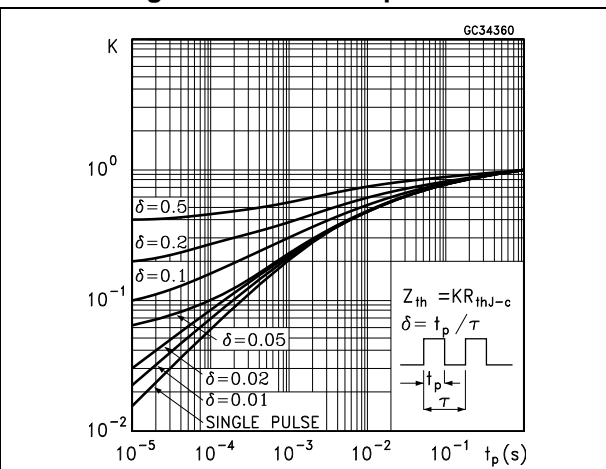


Figure 4. Output characteristics

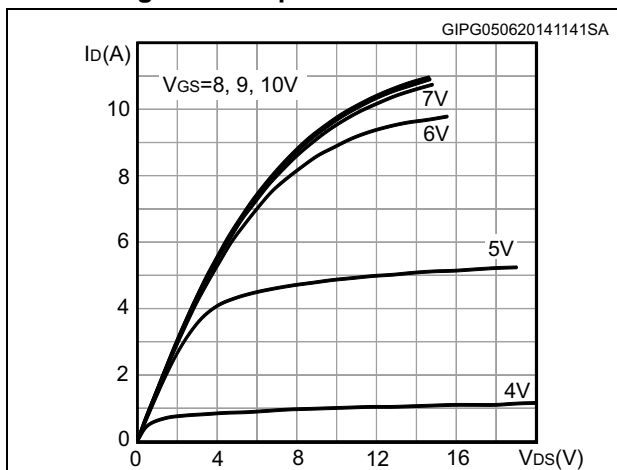


Figure 5. Transfer characteristics

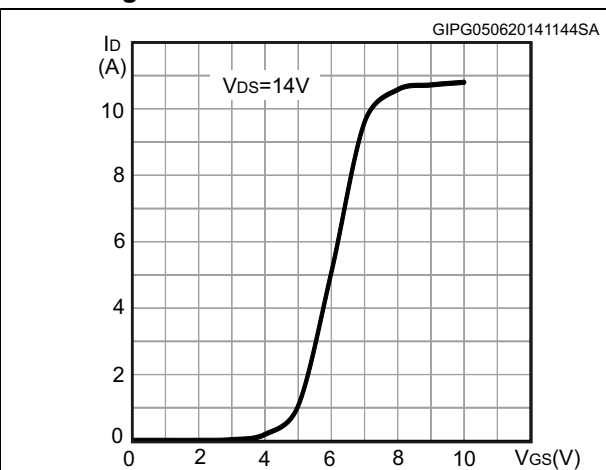


Figure 6. Gate charge vs gate-source voltage

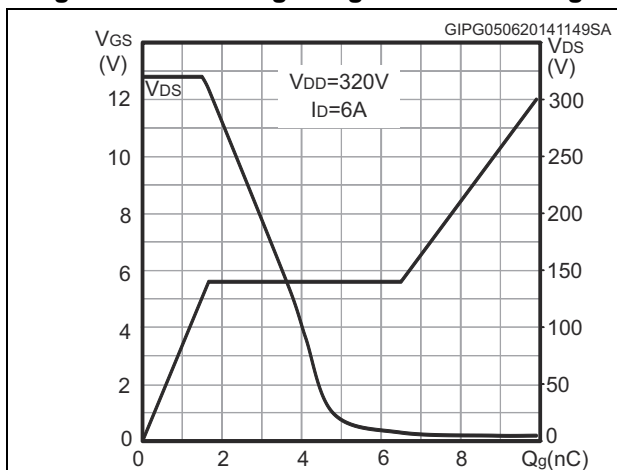


Figure 7. Static drain-source on-resistance

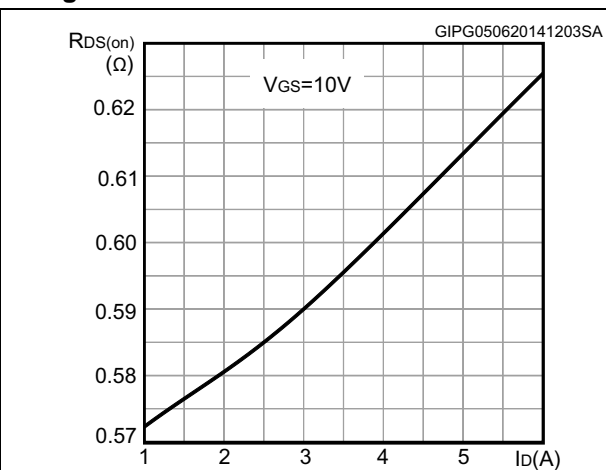


Figure 8. Capacitance variations

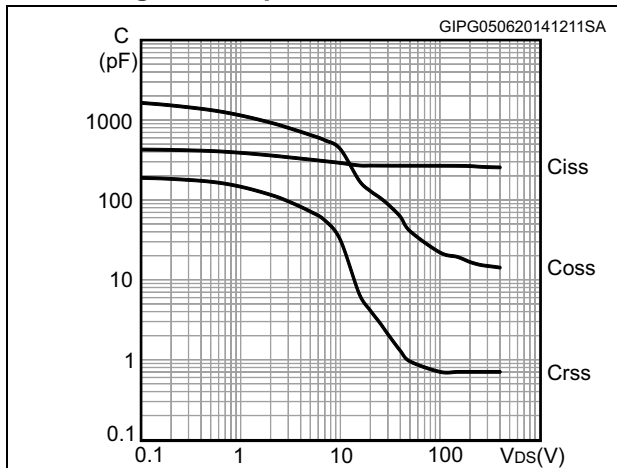


Figure 9. Output capacitance stored energy

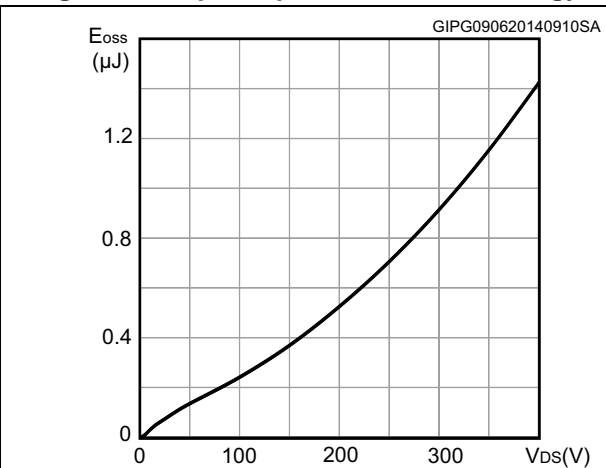


Figure 10. Normalized gate threshold voltage vs temperature

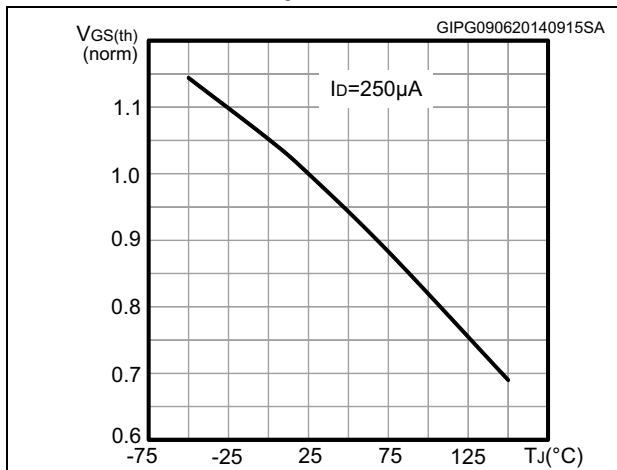


Figure 11. Normalized on-resistance vs temperature

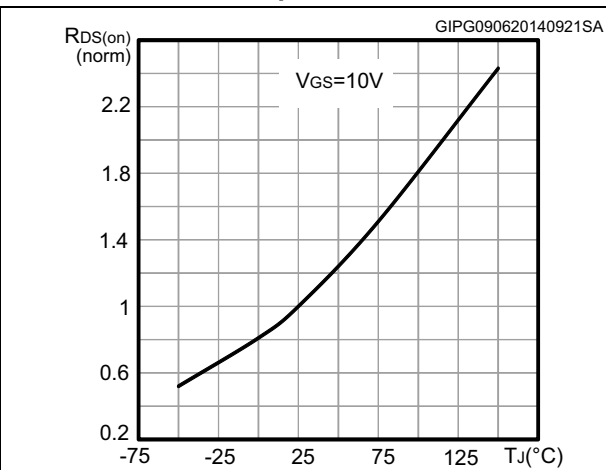


Figure 12. Normalized V(BR)DSS vs temperature

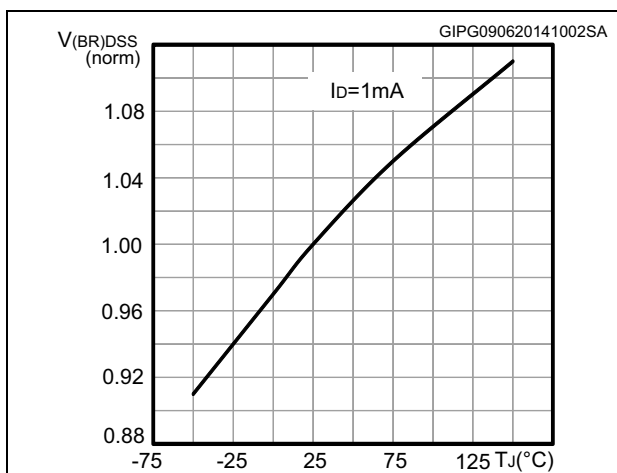
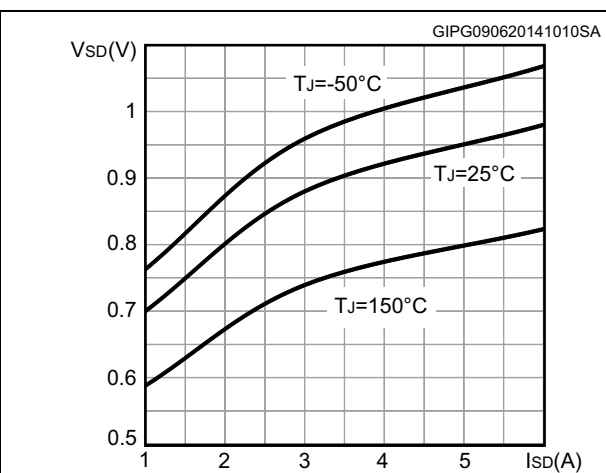


Figure 13. Source-drain diode forward characteristics



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit



Figure 16. Test circuit for inductive load switching and diode recovery times



Figure 17. Unclamped inductive load test circuit



Figure 18. Unclamped inductive waveform

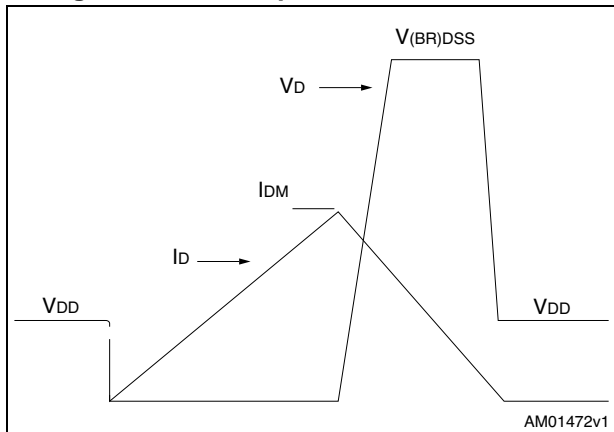


Figure 19. Switching time waveform

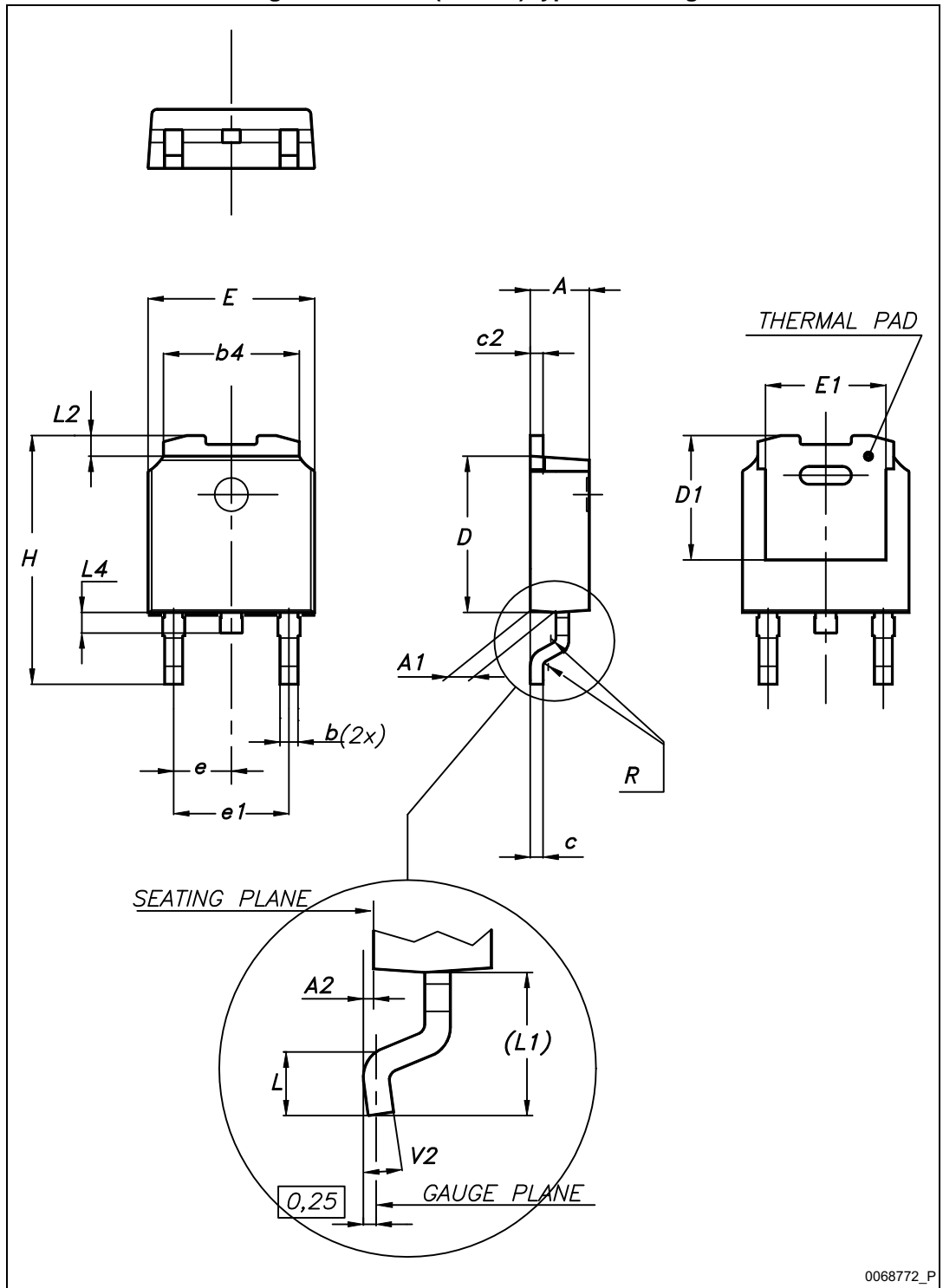




## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 20. DPAK (TO-252) type A drawing

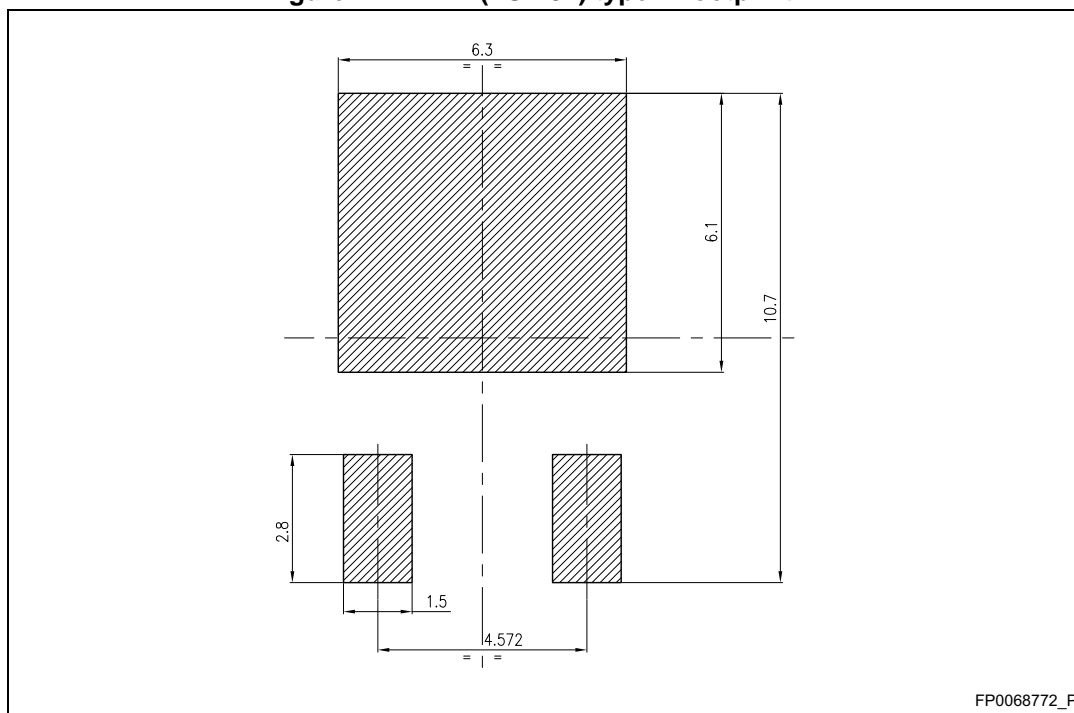


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Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) type A footprint (a)



a. All dimensions are in millimeters

# 5 Packaging mechanical data

Figure 22. Tape for DPAK (TO-252)

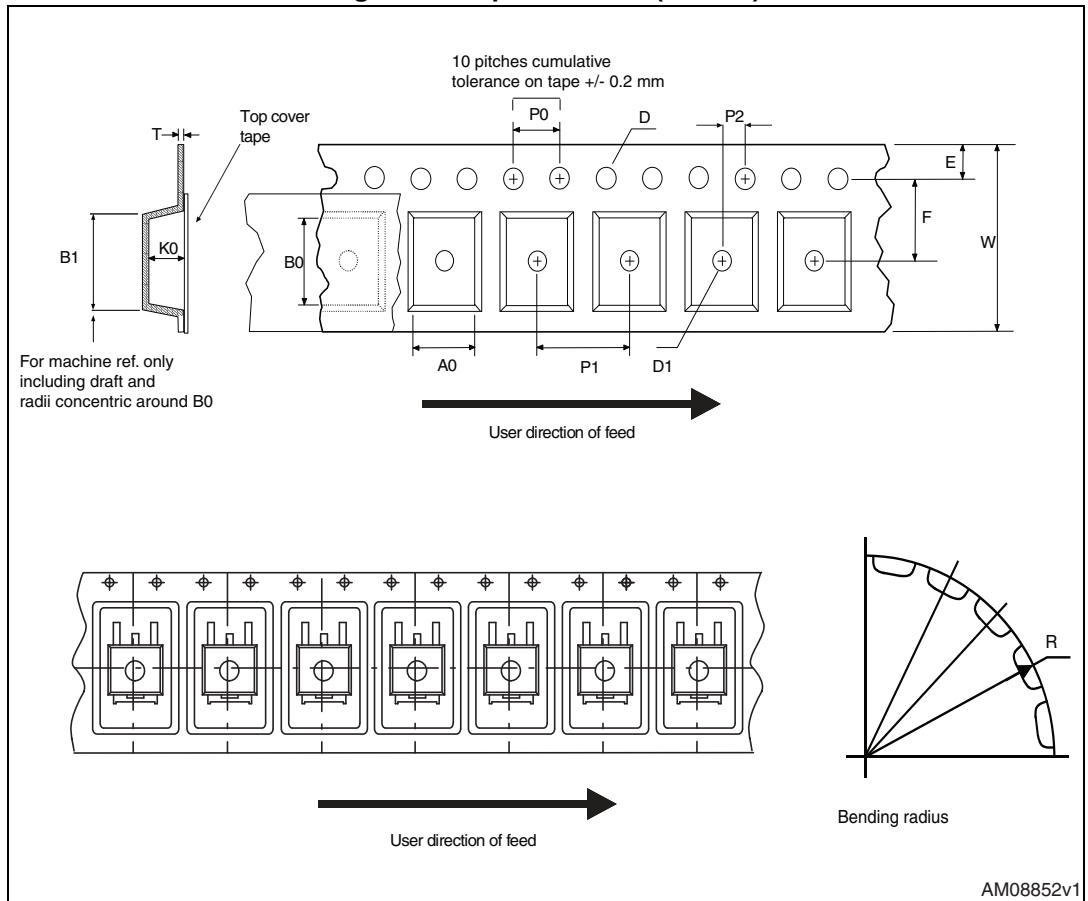


Figure 23. Reel for DPAK (TO-252)

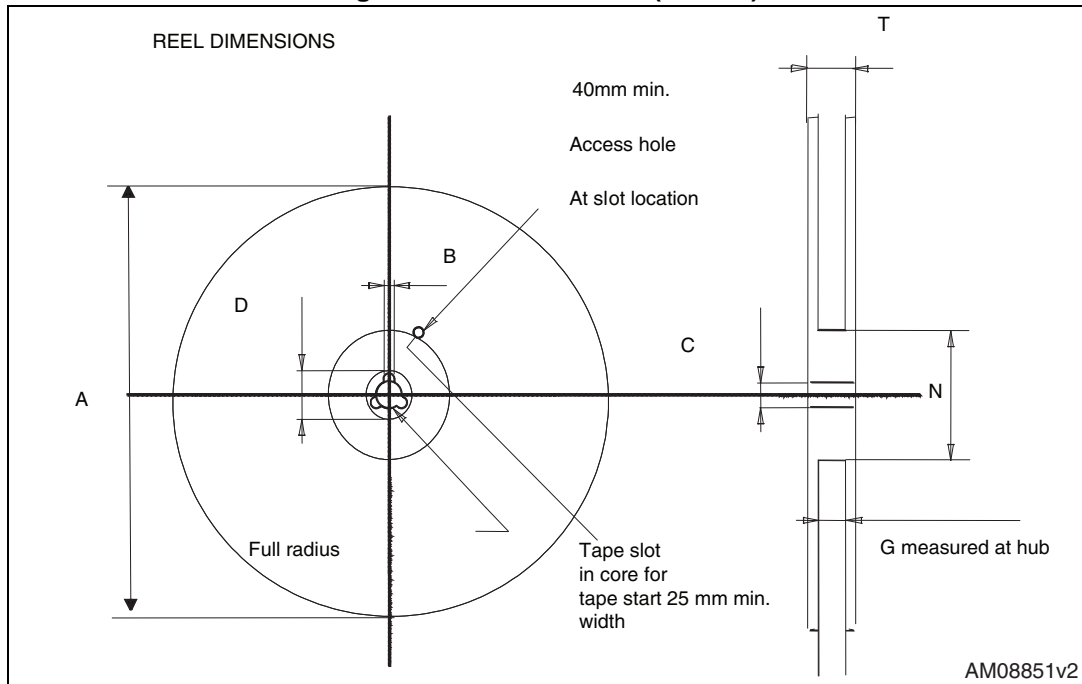


Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
09-Jan-2014	1	First release.
18-Jun-2014	2	<ul style="list-style-type: none"><li>– Modified: title</li><li>– Modified: values in <a href="#">Table 4</a></li><li>– Modified: <math>R_{DS(on)}</math> and <math>I_{DSS}</math> (test conditions) in <a href="#">Table 5</a></li><li>– Modified: the entire typical values in <a href="#">Table 6</a>, <a href="#">7</a> and <a href="#">8</a></li><li>– Added: <a href="#">Table 8</a></li><li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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