



# STD16NF25 STF16NF25 - STP16NF25

N-channel 250V - 0.195Ω - 13A - DPAK/TO-220/TO-220FP  
Low gate charge STripFET™ II Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> Max	I <sub>D</sub>	P <sub>w</sub>
STD16NF25	250V	<0.235Ω	13A	90W
STF16NF25	250V	<0.235Ω	13A <sup>(1)</sup>	25W
STP16NF25	250V	<0.235Ω	13A	90W

1. Limited only by maximum temperature allowed

- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

## Application

- Switching applications

## Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

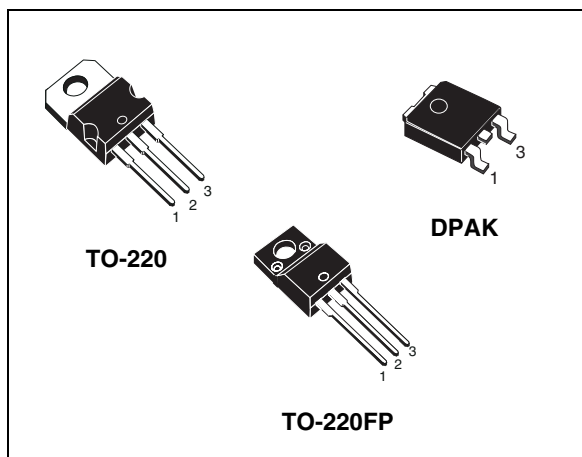


Figure 1. Internal schematic diagram

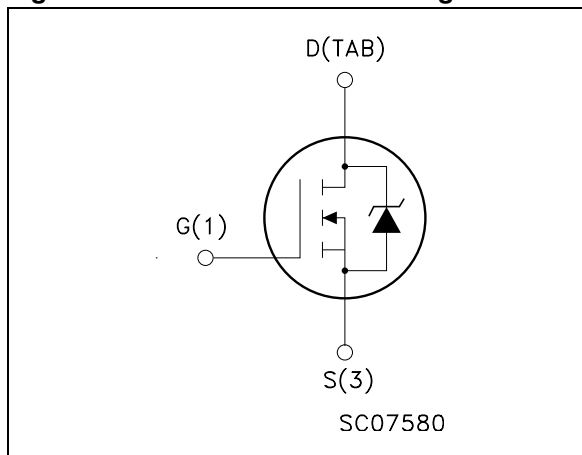


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD16NF25	16NF25	DPAK	Tape & reel
STF16NF25	16NF25	TO-220FP	Tube
STP16NF25	16NF25	TO-220	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		DPAK TO-220	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	250		V
V <sub>GS</sub>	Gate- source voltage	± 20		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	13	13 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100°C	8.19	8.19 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	52	52 <sup>(1)</sup>	A
P <sub>tot</sub>	Total dissipation at T <sub>C</sub> = 25°C	90	25	W
	Derating Factor	0.72	0.2	W/°C
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;Tc=25°C)	--	2500	V
T <sub>stg</sub>	Storage temperature	-55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature			

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area.
3. I<sub>SD</sub> ≤ 13A, di/dt ≤ 300A/μs, V<sub>DD</sub> ≤ 80% V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220	DPAK	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.39		5	°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction to pcb max	--	50	--	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max	62.5	100	62.5	°C/W
T <sub>J</sub>	Maximum lead temperature for soldering purpose	300			°C

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>J</sub> Max)	13	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> =25°C, I <sub>d</sub> = 13A, V <sub>dd</sub> =50V)	100	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	250			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max ratings}$ $V_{DS} = \text{max ratings},$ $T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 6.5A$		0.195	0.235	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 6.5A$		10		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		680 125 20		pF pF pF
$C_{oss\ eq.}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0V \text{ to } 200V,$ $V_{GS} = 0$		48		pF
$R_G$	Intrinsic gate resistance	$f=1MHz, \text{ open drain}$		2.1		$\Omega$
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 125V, I_D = 6.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see <a href="#">Figure 18</a> )		9 17 35 17		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 200V, I_D = 6.5A,$ $V_{GS} = 10V$ (see <a href="#">Figure 19</a> )		18 3 8		nC nC nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%.
2.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				13 52	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 13A, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 13A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 60V$ (see <a href="#">Figure 20</a> )		133 651 10		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 13A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 60V, T_j = 150^\circ C$ (see <a href="#">Figure 20</a> )		157 895 11		ns $\mu C$ A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

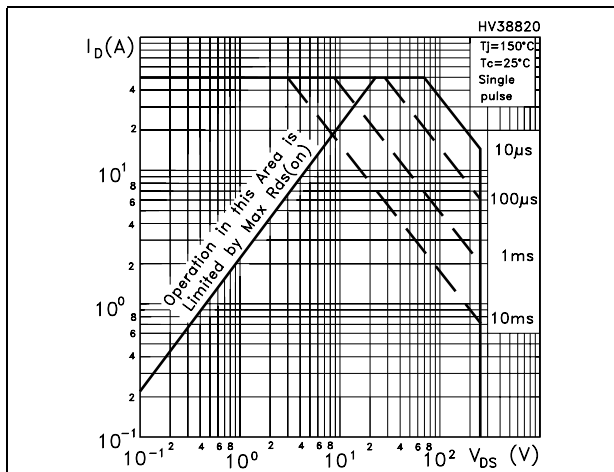


Figure 3. Thermal impedance for TO-220

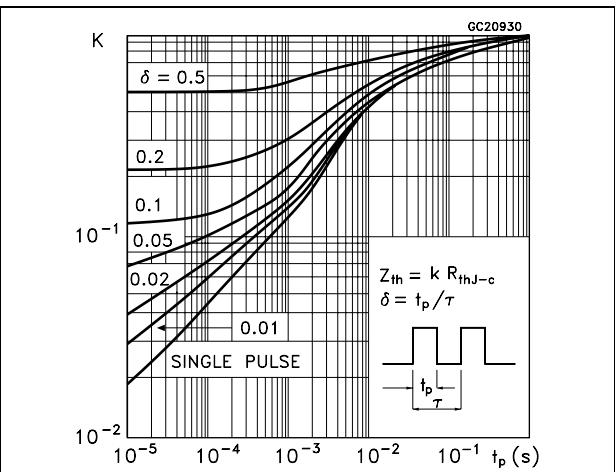


Figure 4. Safe operating area for TO-220FP

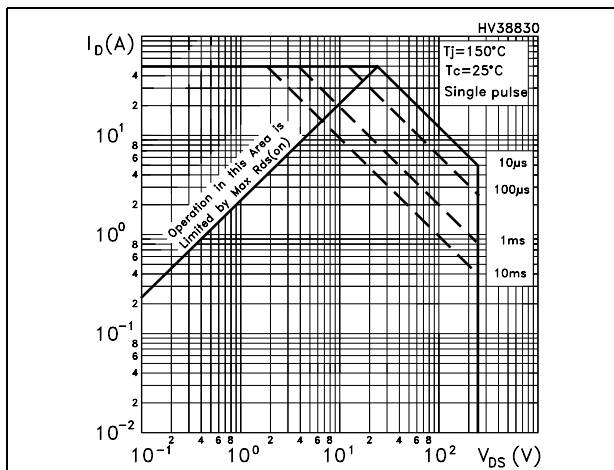


Figure 5. Thermal impedance for TO-220FP

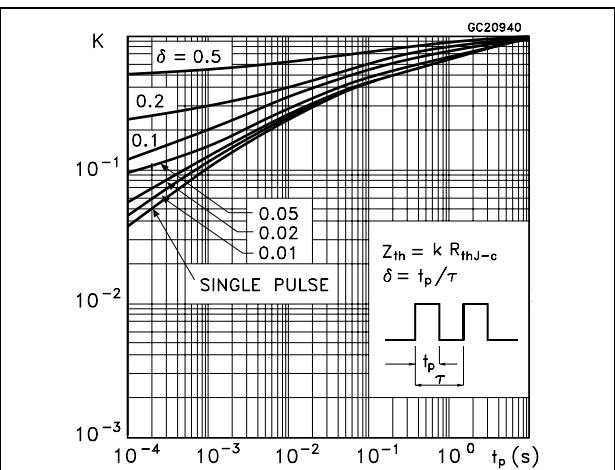


Figure 6. Safe operating area for DPAK

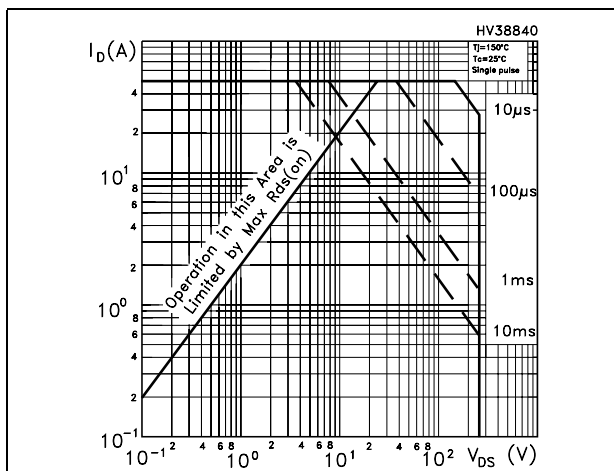


Figure 7. Thermal impedance for DPAK

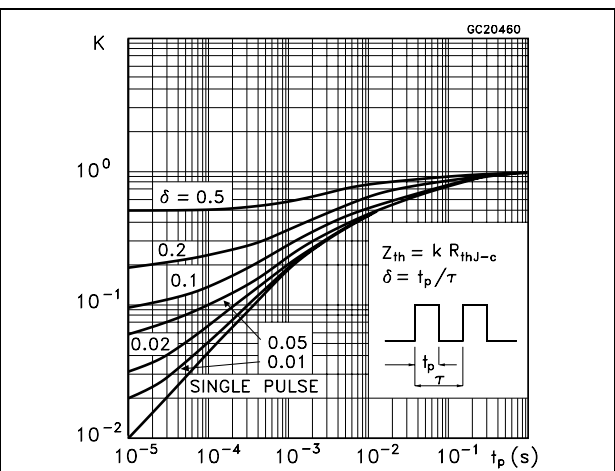


Figure 8. Output characteristics

Figure 9. Transfer characteristics

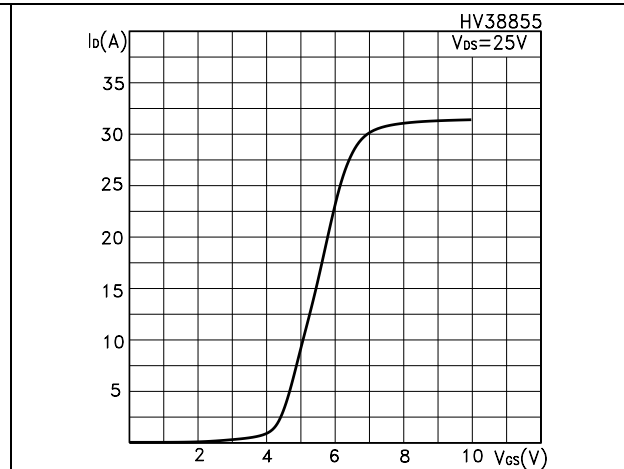
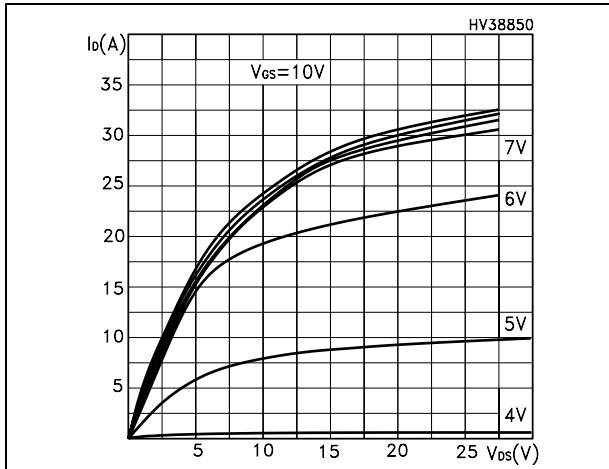


Figure 10. Normalized  $BV_{DSS}$  vs temperature

Figure 11. Static-drain source on resistance

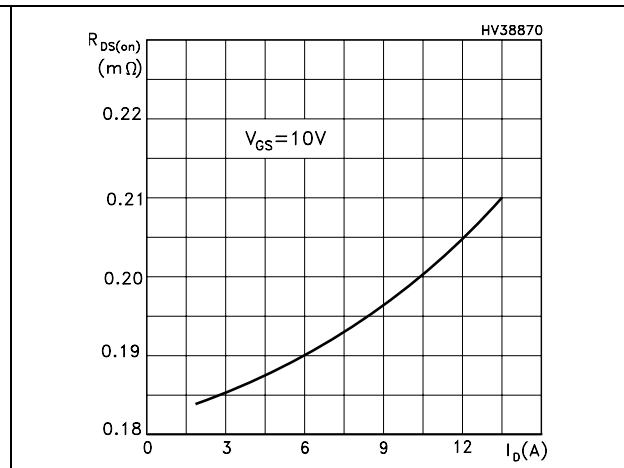
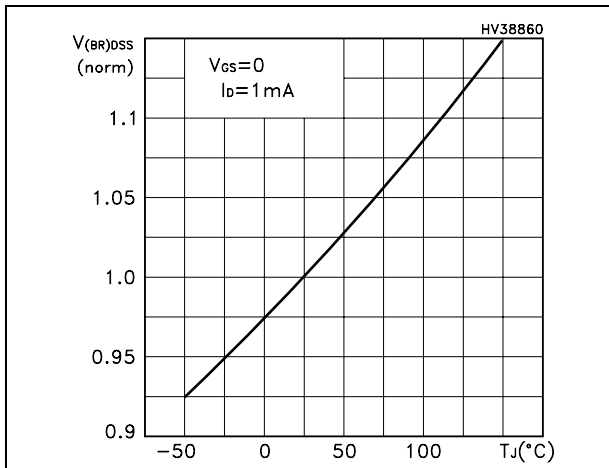


Figure 12. Gate charge vs gate-source voltage

Figure 13. Capacitance variations

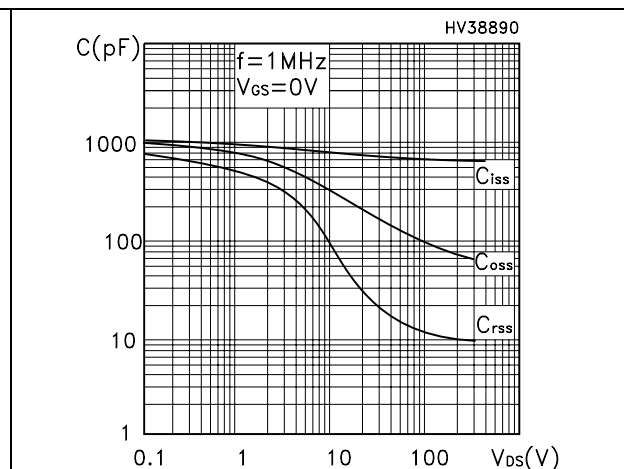
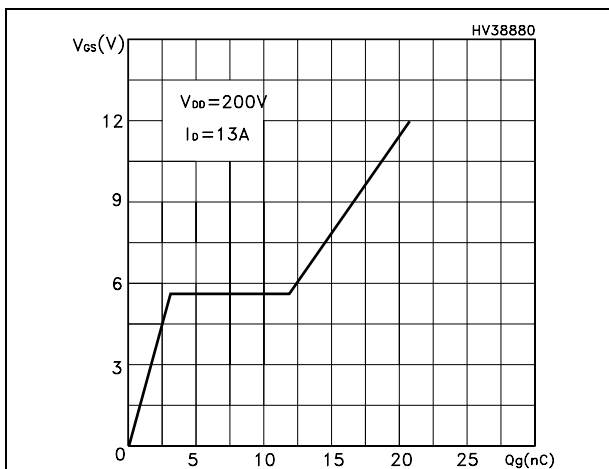


Figure 14. Normalized gate threshold voltage vs temperature

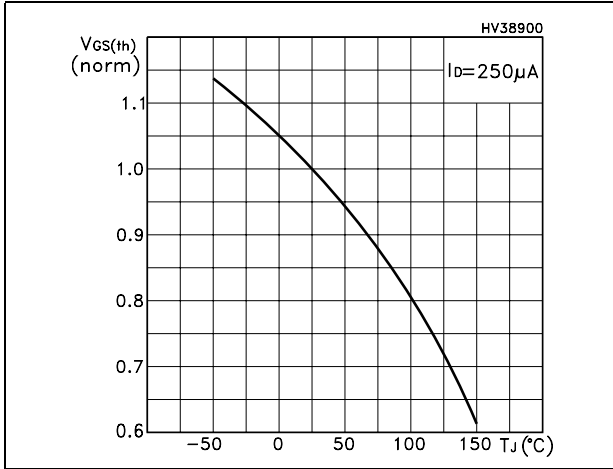


Figure 15. Normalized on resistance vs temperature

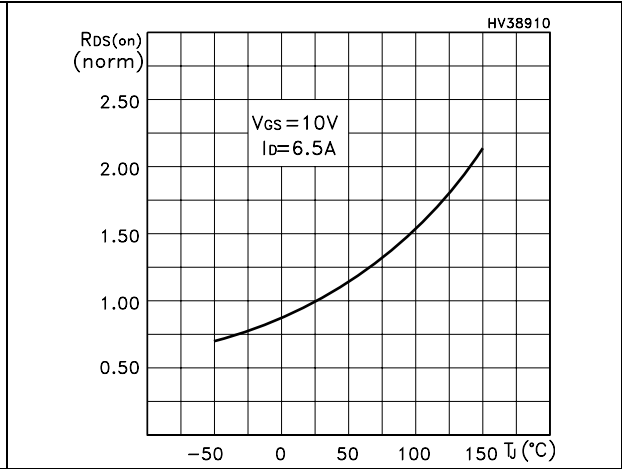


Figure 16. Source-drain diode forward characteristics

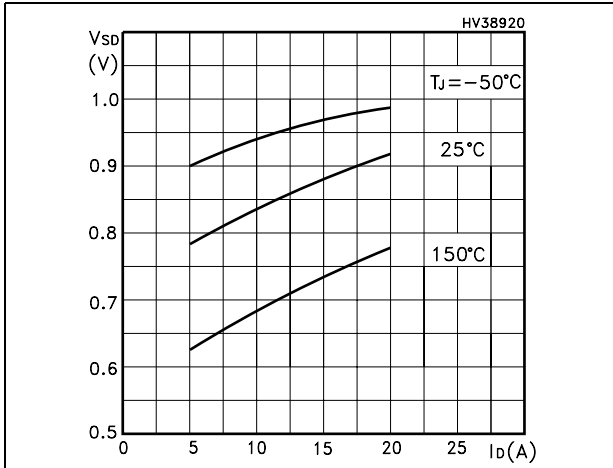
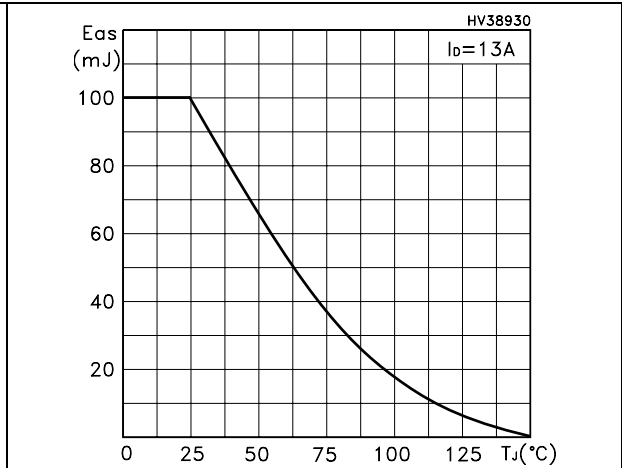


Figure 17. Maximum avalanche energy vs starting Tj





### 3 Test circuit

Figure 18. Switching times test circuit for resistive load



Figure 19. Gate charge test circuit

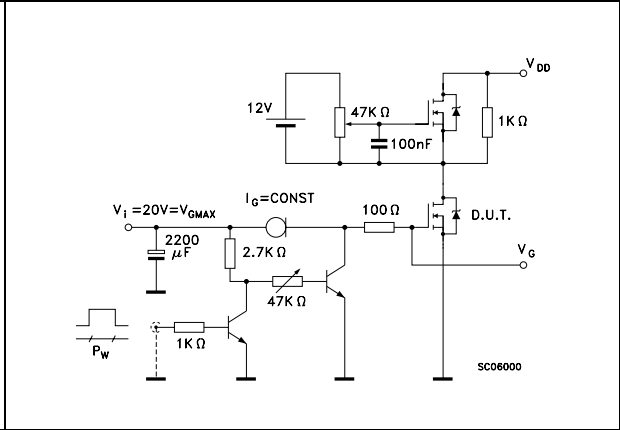


Figure 20. Test circuit for inductive load switching and diode recovery times



Figure 21. Unclamped Inductive load test circuit

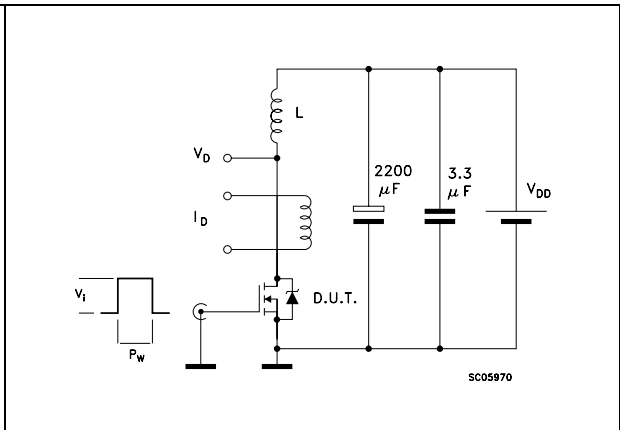
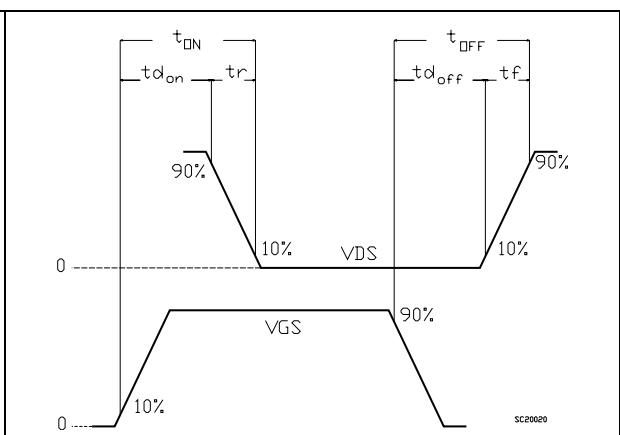


Figure 22. Unclamped inductive waveform



Figure 23. Switching time waveform

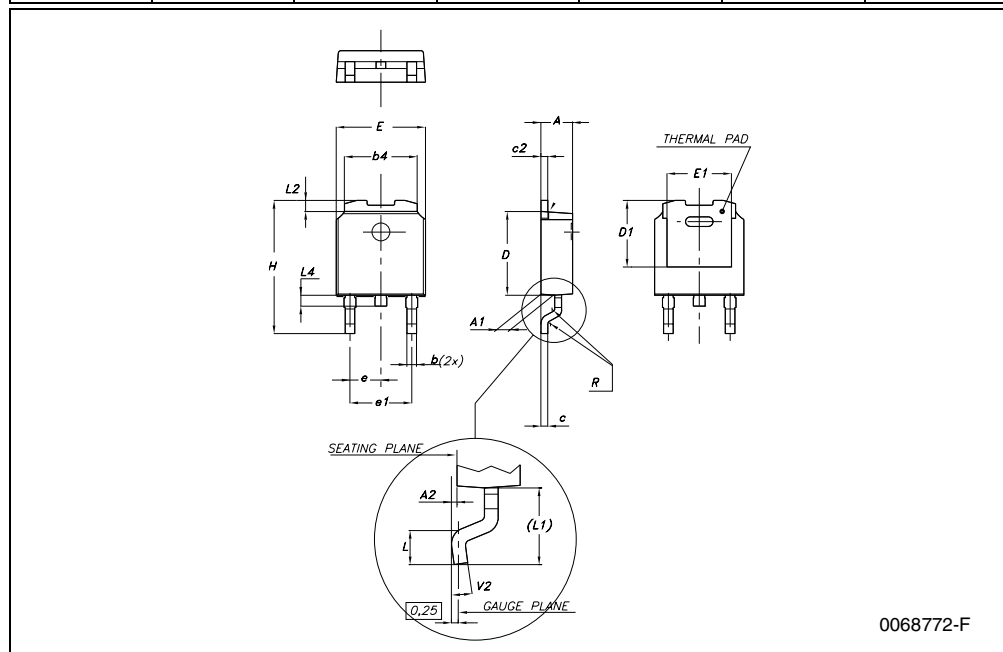


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

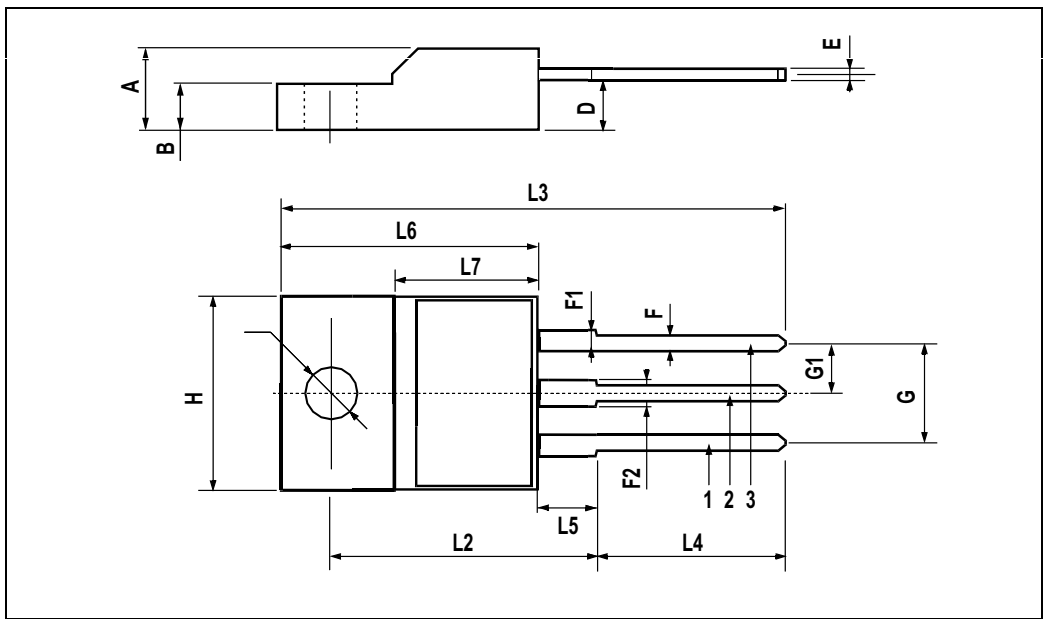
**DPAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



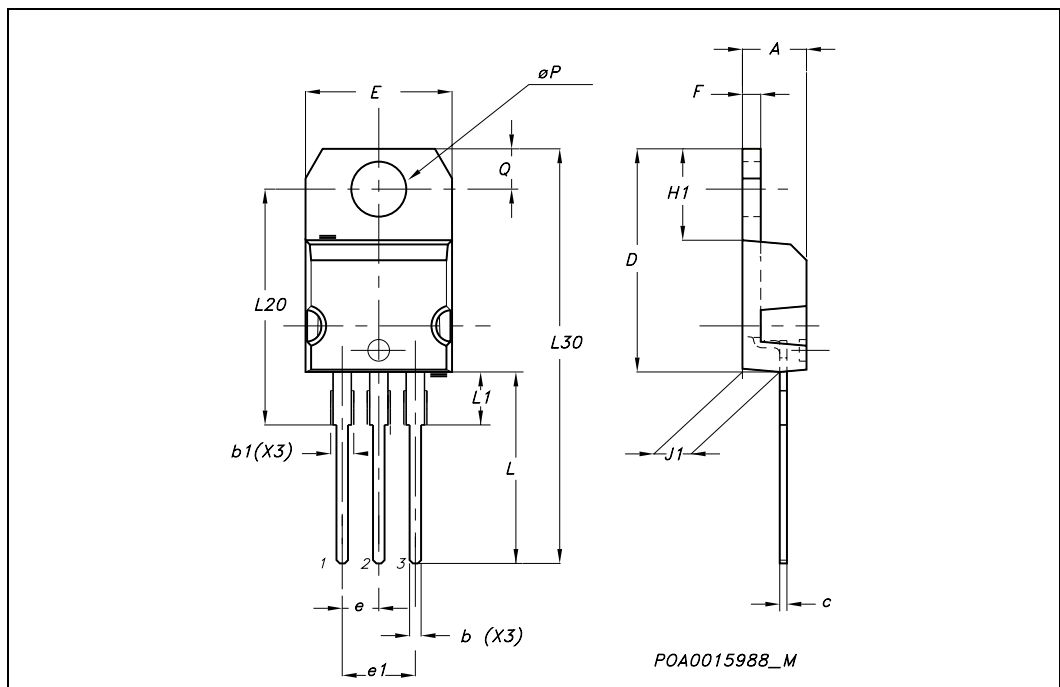
**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



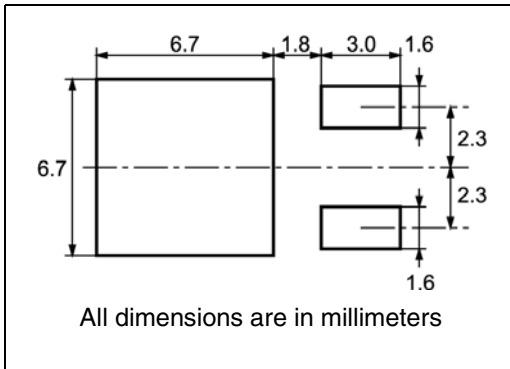
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY		BULK QTY	
2500		2500	

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
12-Oct-2007	1	Initial release
16-Oct-2007	2	Modified: <a href="#">Figure 13: Capacitance variations</a>

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