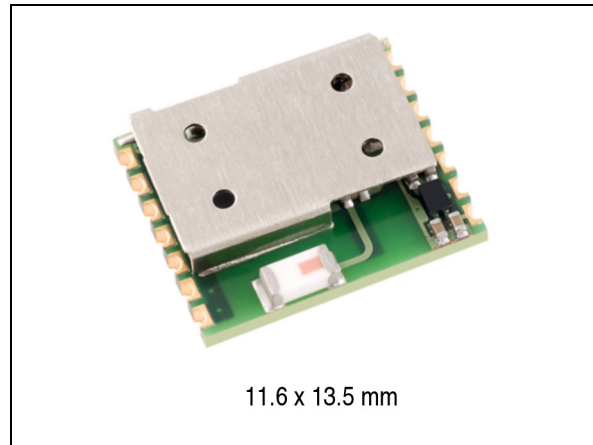


Features

- Bluetooth® radio
 - Fully embedded Bluetooth® v3.0 with profiles
 - Class 2 module
 - Complete RF ready module
 - 128-bit encryption security
 - Integrated antenna
 - Multipoint capability
- ST micro Cortex-M3 microprocessor up to 72 MHz
- Memory
 - 256 kb Flash memory
 - 48 kb RAM memory
- Data rate
 - 1.5 Mbps maximum data rate
- Serial interface
 - UART up to 2.0 Mbps
 - SPI interface
- General I/O
 - 7 general purpose I/Os
 - 1 LPO input
- User interface
 - AT2 command set (abSerial)
 - Firmware upgrade over UART
- FCC and Bluetooth® qualified
- EPL (end product listing) fulfilled
- Single voltage supply: 2.5 V typical
- Micro-sized form factor: 11.6 x 13.5 x 2.9 mm
- Operating temperature range: -40 °C to 85 °C.



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1 Description

The SPBT2632C2A.AT2 is an easy to use Bluetooth module, compliant with Bluetooth v3.0.

The module is the smallest form factor available which provides a complete RF platform. The SPBT2632C2A.AT2 enables electronic devices with wireless connectivity, not requiring any RF experience or expertise for integration into the final product. The SPBT2632C2A.AT2 module, being a certified solution, optimizes the time to market of the final applications.

The module is designed for maximum performance in a minimal space including fast speed UART and 7 general purpose I/O lines, several serial interface options, and up to 1.5 Mbps data throughput.

Optimized design allows the integration of a complete working Bluetooth modem, including antenna, in the minimum possible size; only an additional external LPO (low power oscillator) is required to enable low power mode capability.

The SPBT2632C2A.AT2 is a surface mount PCB module that provides fully embedded, ready to use Bluetooth wireless technology. The reprogrammable Flash memory contains embedded firmware for serial cable replacement using the Bluetooth SPP profile. Embedded Bluetooth AT2 command firmware is a friendly interface, which realizes a simple control for cable replacement, enabling communication with most Bluetooth enabled devices, provided that the devices support the SPP profile. The SPBT2632C2A.AT2 , supporting iAP profile, provides communication with Android, smartphone, and Apple® iOS Bluetooth enabled devices.

An Apple authentication IC is required to exchange data with an Apple device or access an Apple device application. The AT2 FW includes the Bluetooth SPP profile capable of recognizing the Apple authentication chip.

Customers using the Apple authentication IC must register as developers to become an Apple certified MFI member. License fees may apply, for additional information visit: <http://developer.apple.com/programs/which-program/index.html>.

Certified MFI developers developing electronic accessories that connect to the iPod®, iPhone®, and iPad® gain access to technical documentation, hardware components, technical support and certification logos.

Customized firmware for peripheral device interaction, power optimization, security, and other proprietary features may be supported and can be ordered pre-loaded and configured.

2 RoHS compliance

ST modules are RoHS compliant and comply with ECOPACK® norms.

3 Applications

- Serial cable replacement
- M2M industrial control
- Service diagnostic
- Data acquisition equipment
- Machine control
- Sensor monitoring
- Security system
- Mobile health.

4 Software architecture

4.1 Lower layer stack

- Bluetooth v3.0
- Device power modes: active, sleep and deep sleep
- Wake on Bluetooth feature optimized power consumption of host CPU
- Authentication and encryption
- Encryption key length from 8 bits to 128 bits
- Persistent Flash memory for BD address and user parameter storage
- All ACL (asynchronous connection less) packet types
- Multipoint capability
- Sniff mode: fully supported to maximum allowed intervals
- Master slave switch supported during connection and post connection
- Dedicated inquiry access code for improved inquiry scan performance
- Dynamic packet selection channel quality driven data rate to optimize link performance
- Dynamic power control
- 802.11b co-existence AFH.

4.2 Upper layer stack: Amp'ed UP

- SPP, IAP, SDAP and GAP protocols
- RFComm, SDP, and L2CAP supported
- Multipoint with simultaneous slaves.

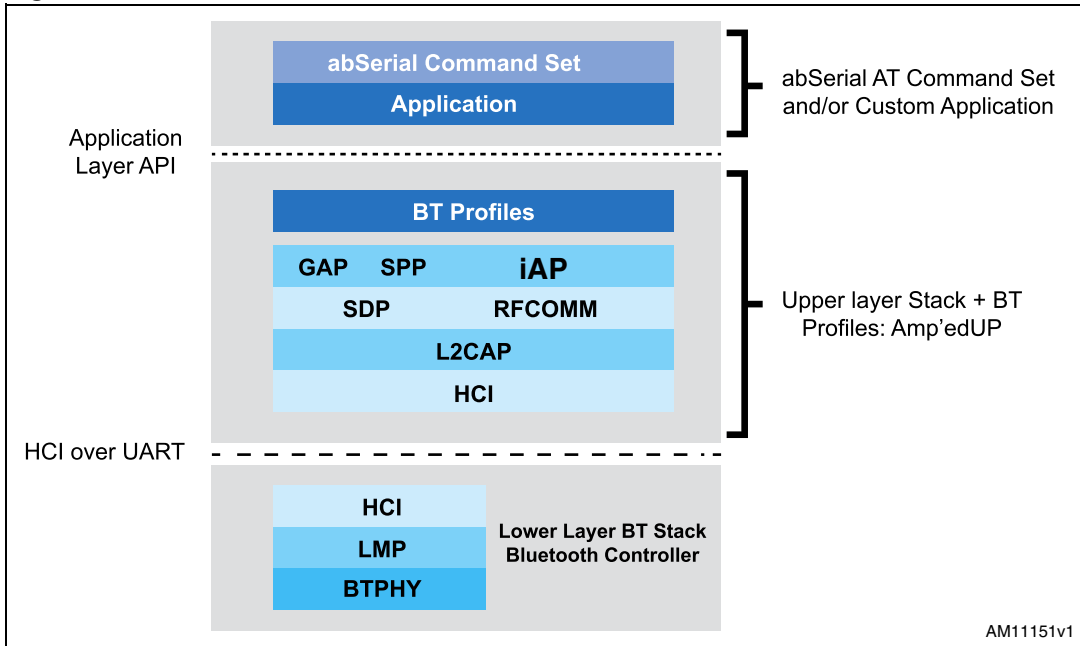
4.3 AT command set: abSerial

Please see command list reported in the SPBT2532C2.AT datasheet, Appendix D, for details.

The complete command list including the iAP commands will be reported in the user manual UM1547.

4.4 Bluetooth firmware implementation

Figure 1. FW architecture



5 Hardware specifications

General conditions ($V_{IN} = 2.5\text{ V}$ and 25 °C).

5.1 Recommended operating conditions

Table 1. Recommended operating conditions

Rating	Min.	Typical	Max.	Unit
Operating temperature range	-40	-	85	°C
Supply voltage V_{IN}	2.1	2.5	3.6	V
Signal pin voltage	-	2.1	-	V
RF frequency	2400	-	2483.5	MHz

5.2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Rating	Min.	Typical	Max.	Unit
Storage temperature range	-55	-	+105	°C
Supply voltage, V_{IN}	-0.3	-	+ 5.0	V
I/O pin voltage, V_{IO}	-0.3	-	+ 5.5	V
RF input power	-	-	-5	dBm

5.3 High speed CPU mode current consumption

- High speed CPU mode
 - CPU 32 MHz
 - UART supports up to 921 Kbps
 - Data throughput up to 1.5 Mbps
 - Shallow sleep enabled.

Table 3. High speed CPU mode current consumption

Modes (typical power consumption)	Avg.	Unit
ACL data 115 K baud UART at max. throughput (master)	23	mA
ACL data 115 K baud UART at max. throughput (slave)	27.5	mA
Connection, no data traffic, master	9.1	mA
Connection, no data traffic, slave	11.2	mA
Connection 375 ms sniff (external LPO required)	490	μA
Standby, without deep sleep	8.6	mA
Standby, with deep sleep, no external LPO	1.7	mA
Standby, with deep sleep, with external LPO	70	μA
Page/inquiry scan, with deep sleep, no external LPO	2.7	mA
Page/inquiry scan, with deep sleep, with external LPO	520	μA
Bluetooth power down / CPU standby, no external LPO	25	μA

5.4 Standard CPU mode current consumption

- Standard CPU mode
 - CPU 8 MHz
 - UART supports up to 115 Kbps
 - Data throughput up to 200 Kbps
 - Shallow sleep enabled.

Table 4. Standard CPU mode current consumption

Modes (typical power consumption)	Avg.	Unit
ACL data 115 K baud UART at max. throughput (master)	16.7	mA
ACL data 115 K baud UART at max. throughput (slave)	18	mA
Connection, no data traffic, master	4.9	mA
Connection, no data traffic, slave	7.0	mA
Connection 375 ms sniff (external LPO required)	490	μA
Standby, without deep sleep	4.2	mA
Standby, with deep sleep, no external LPO	1.7	mA

Table 4. Standard CPU mode current consumption (continued)

Modes (typical power consumption)	Avg.	Unit
Standby, with deep sleep, with external LPO	70	μA
Page/inquiry scan, with deep sleep, no external LPO	2.6	mA
Page/inquiry scan, with deep sleep, with external LPO	520	μA
Bluetooth power-down / CPU standby, no external LPO	25	μA

5.5 I/O operating characteristics

Table 5. I/O operating characteristics

Symbol	Parameter	Min.	Max.	Unit	Conditions
V _{IL}	Low-level input voltage	-	0.6	V	V _{IN} , 2.1 V
V _{IH}	High-level input voltage	1.4	-	V	V _{IN} , 2.1 V
V _{OL}	Low-level output voltage	-	0.4	V	V _{IN} , 2.1 V
V _{OH}	High-level output voltage	1.8	-	V	V _{IN} , 2.1 V
I _{OL}	Low -level output current	-	4.0	mA	V _{OL} = 0.4 V
I _{OH}	High-level output current	-	4.0	mA	V _{OH} = 1.8 V
R _{PU}	Pull-up resistor	80	120	kΩ	Resistor turned on
R _{PD}	Pull-down resistor	80	120	kΩ	Resistor turned on

5.6 Selected RF characteristics

Table 6. Selected RF characteristics

Parameters	Conditions	Typical ⁽¹⁾	Unit
Antenna load		50	ohm
Radio receiver			
Sensitivity level	BER < .001 with DH5	-86	dBm
Maximum usable level	BER < .001 with DH1	0	dBm
Input VSWR		2.5:1	
Radio transmitter			
Maximum output power	50 Ω load	0	dBm
Initial carrier frequency tolerance		0	kHz
20 dB bandwidth for modulated carrier		935	kHz

1. RF characteristics can be influenced by physical characteristics of final application.

5.7 Pin assignment

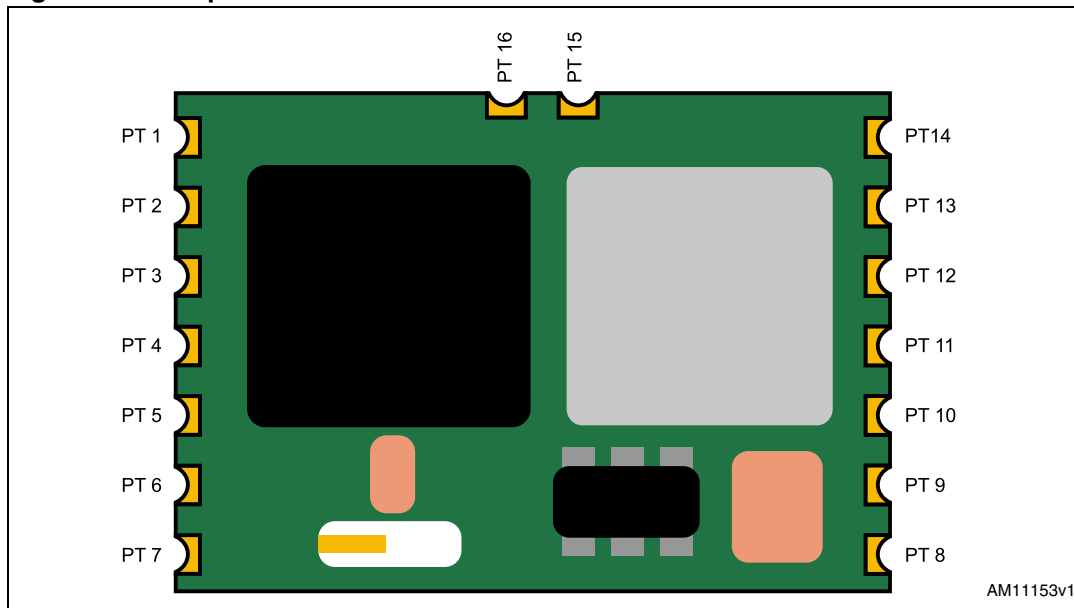
Table 7. Pin assignment

Name	Type	Pin#	Description	ALT function ⁽¹⁾	5 V tolerant
UART interface					
RXD	I	13	Receive data	ADC 3	Y
TXD	O	14	Transmit data	ADC 2	Y
RTS	O	12	Request to send (active low)	ADC 0 I ² C clock/aux UART Rx	Y
CTS	I	11	Clear to send (active low)	ADC 1 I ² C data/aux UART Tx	Y
Boot loader					
Boot 0	I	9	Boot 0		
Power and ground					
V _{in}		8	V _{in}		
GND		7	GND		
Reset					
RESETN	I	10	Reset input (active low for 5 ms)		2.5 V max.
LPO					
LPO	I	15	LPO input		
GPIO - general purpose input/output					
GPIO [1]	I/O	1	General purpose input/output	SPI MISO	Y
GPIO [2]	I/O	2	General purpose input/output	SPI MOSI/I2S_SD	Y
GPIO [3]	I/O	3	General purpose input/output	SPI SCLK/I2S_CK	Y
GPIO [4]	I/O	4	General purpose input/output	SPI SS/I2S_WS	Y
GPIO [5]	I/O	5	General purpose input/output		Y
GPIO [6]	I/O	6	General purpose input/output	DAC	Y
GPIO [7]	I/O	16	General purpose input/output	ADC 4	Y

1. Please note that the usage of ALT function is dependant upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT command interface uses the main UART by default.

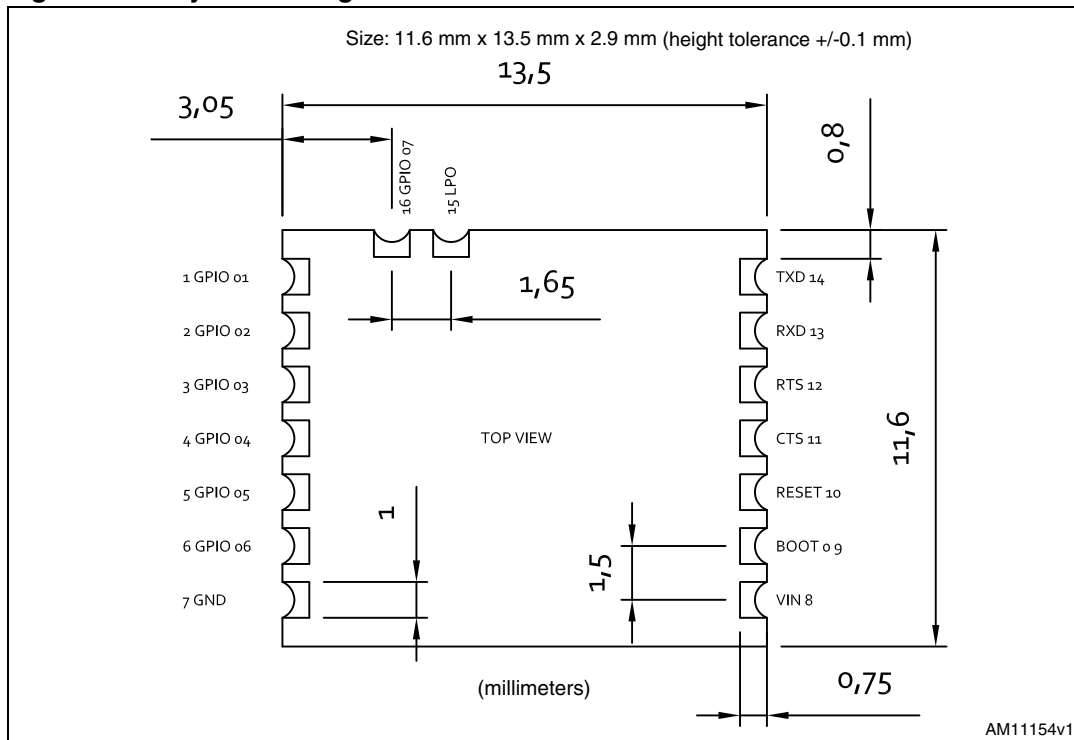
5.8 Pin placement

Figure 2. Pin placement



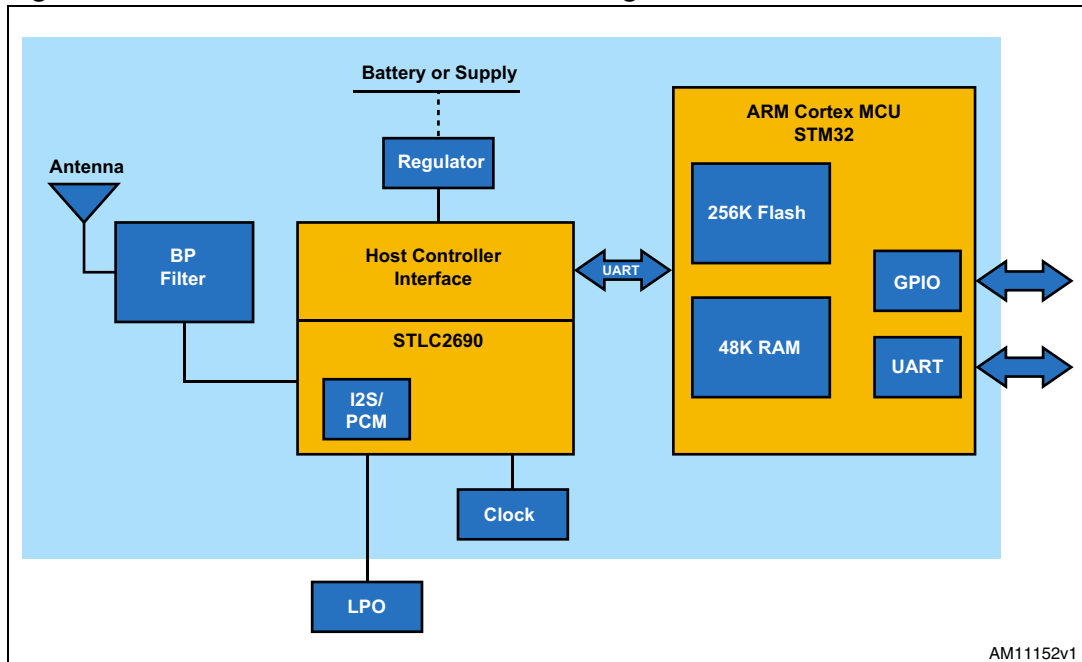
5.9 Layout drawing

Figure 3. Layout drawing



6 Hardware block diagram

Figure 4. SPBT2632C2A.AT2 module block diagram



AM11152v1

7 Hardware design

The SPBT2632C2A module without AT2 command embedded FW supports UART, SPI, I²C and GPIO hardware interfaces. Note that the usage of these interfaces is dependent upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT2 command interface uses the main UART by default.

- Note:*
- 1 All unused pins should be left floating; do not ground.
 - 2 All GND pins must be well grounded.
 - 3 The area around the module should be free of any ground planes, power planes, trace routings, or metal for 6 mm from the antenna in all directions.
 - 4 Traces should not be routed underneath the module.

7.1 Module reflow installation

The SPB2632C2A is a surface mount Bluetooth module supplied on a 16-pin, 6-layer PCB. The final assembly recommended reflow profiles are indicated here below.

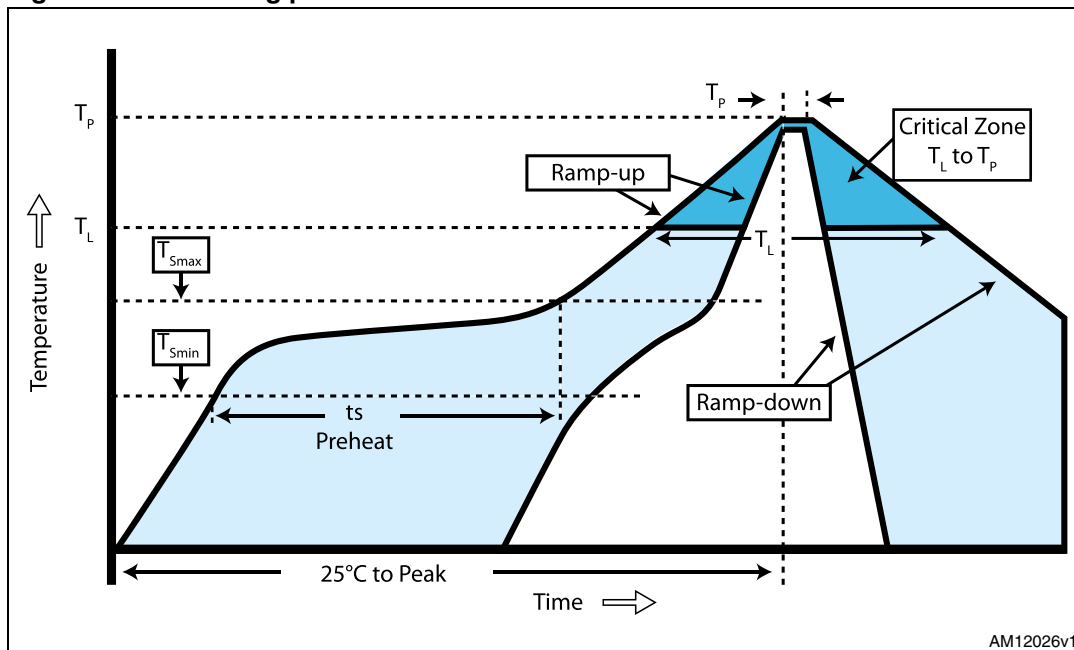
The soldering phase must be executed with care: In order to avoid undesired melting phenomenon, particular attention must be paid to the setup of the peak temperature.

The following are some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations.

Table 8. Soldering

Profile feature	PB-free assembly
Average ramp-up rate (T _S MAX to T _P)	3 °C/sec max
Preheat:	
– Temperature min. (T _S min.)	150 °C
– Temperature max. (T _S max.)	200 °C
– Time (t _S min. to t _S max.)(t _S)	60-100 sec
Time maintained above:	
– Temperature T _L	217 °C
– Temperature T _L	60-70 sec
Peak temperature (T _P)	240 + 0 °C
Time within 5 °C of actual peak temperature (T _P)	10-20 sec
Ramp-down rate	6 °C/sec
Time from 25 °C to peak temperature	8 minutes max.

Figure 5. Soldering profile



7.2 GPIO interface

All GPIOs are capable of sinking and sourcing 4 mA of I/O current. GPIO [1] to GPIO [7] are internally pulled down with 100 kΩ (nominal) resistors.

7.3 UART interface

The UART is compatible with the 16550 industry standard. Four signals are provided with the UART interface. The TXD and RXD pins are used for data while the CTS and RTS pins are used for flow control.

Figure 6. Connection to host device

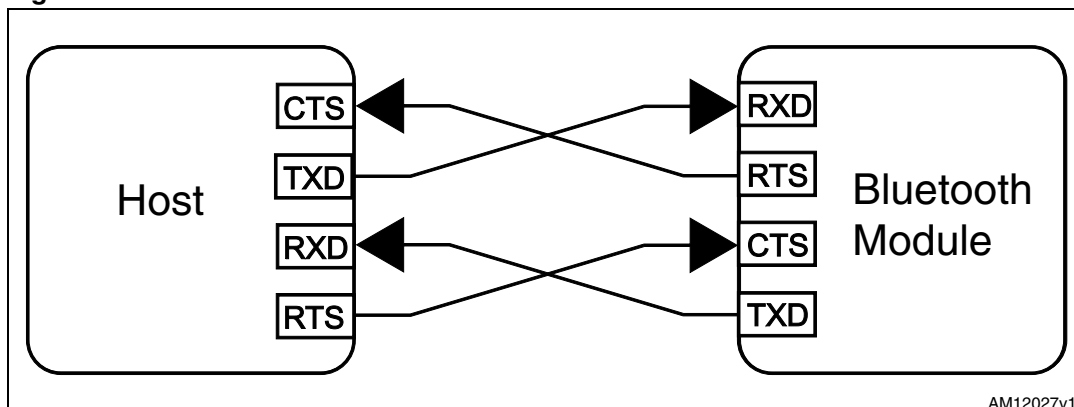
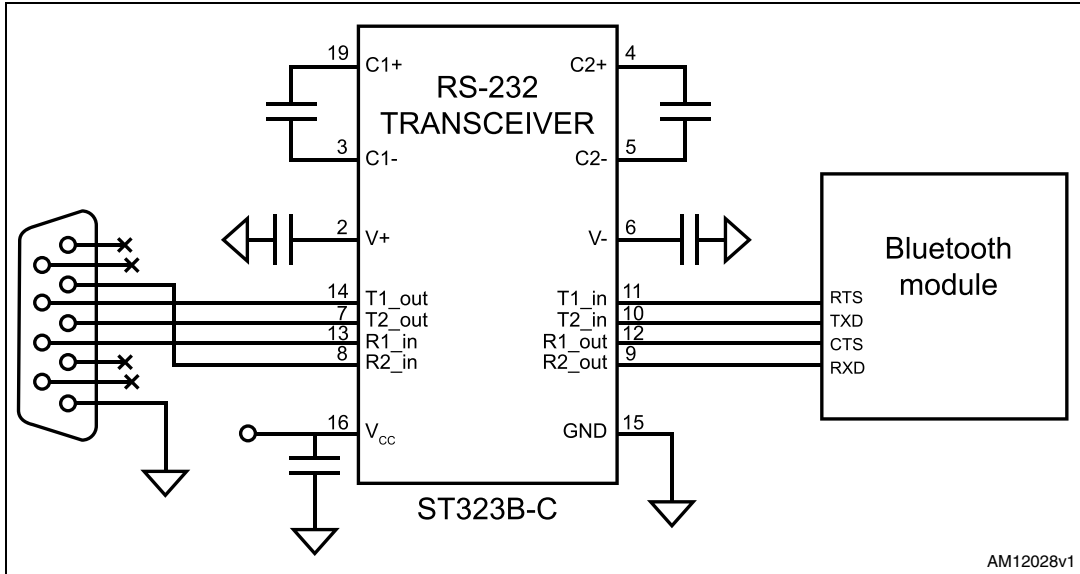
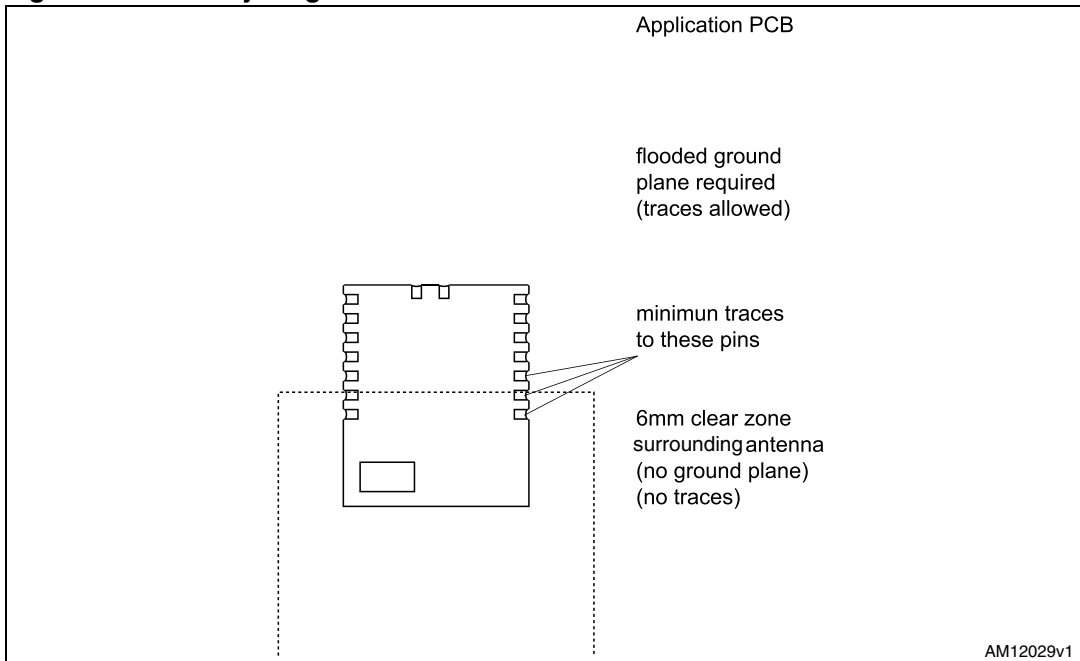


Figure 7. Typical RS232 circuit



7.4 PCB layout guidelines

Figure 8. PCB layout guidelines

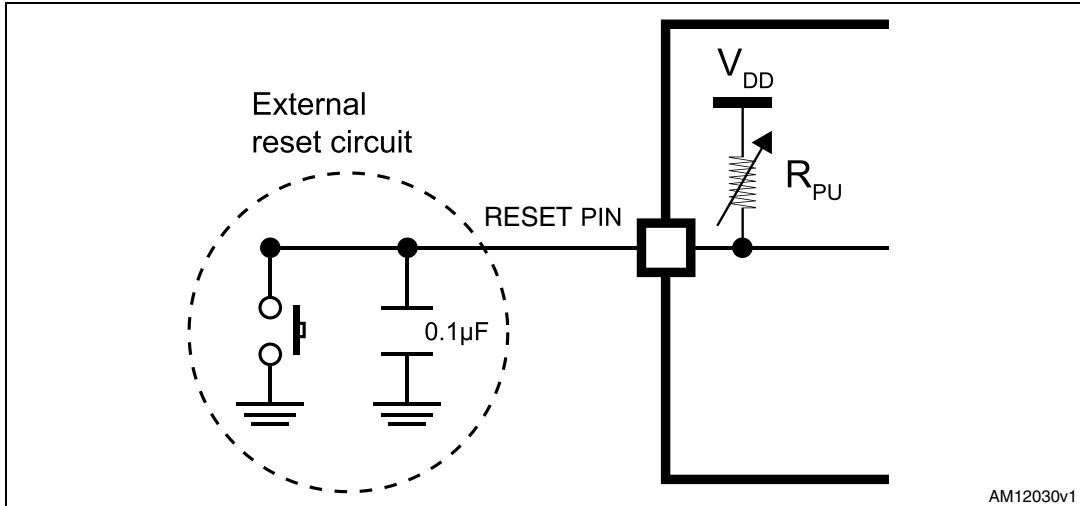


7.5 Reset circuit

Two types of system reset circuits are detailed below.

7.5.1 External reset circuit

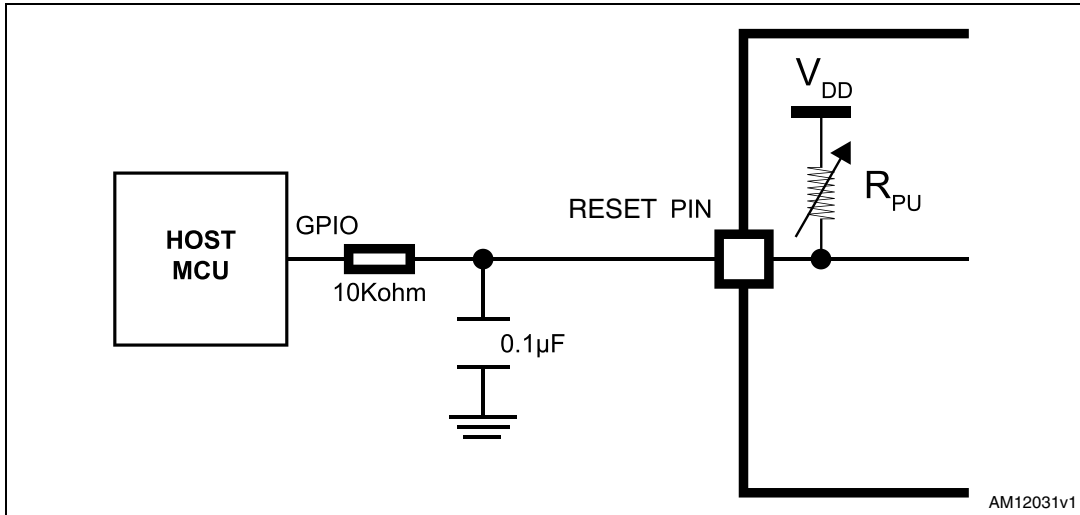
Figure 9. External reset circuit



Note: R_{PU} ranges from 30 k Ω to 50 k Ω internally.

7.5.2 Internal reset circuit

Figure 10. Internal reset circuit



- Note:
- 1 R_{PU} ranges from 30 k Ω to 50 k Ω internally.
 - 2 R_{RST} should be from 1 k Ω to 10 k Ω .

7.6 External LPO input circuit

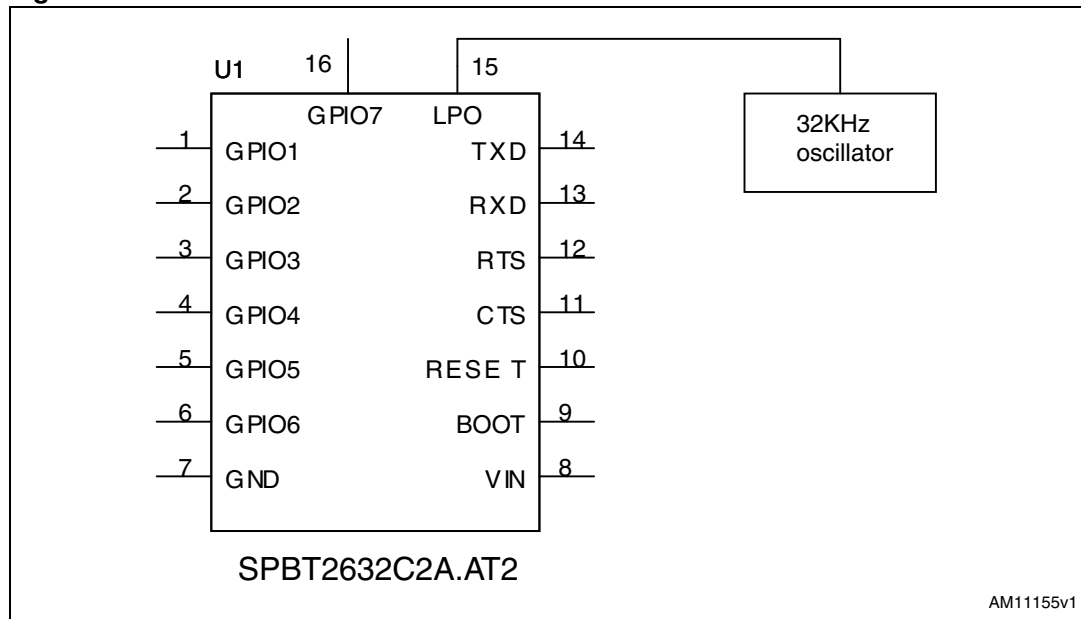
An optional low power oscillator input may be added to allow Deep sleep and Sniff modes.

- LPO parameters:
 - Frequency: 32.768 kHz
 - Tolerance: 150 ppm
 - Voltage levels
 - Low: 0.5 V
 - High: 1.8 V
 - Input capacitance: 2.5 pF maximum
- Configurations:
 - Use two configuration variables: UseExtLPO and AllowSniff.

Table 9. System configuration variables

Variable	Name	Default	Description
Var37	UseExtLPO	True	True when a 32.768 kHz low power oscillator is present, and false if not present
Var43	AllowSniff	True	Enables Sniff mode.

Figure 11. External LPO circuit



7.7 Apple iOS CP reference design

The figures below give an indicative overview of what the hardware concept looks like. A specific MFI co-processor layout is available for licensed MFI developers from the MFI program.

Figure 12. BT module

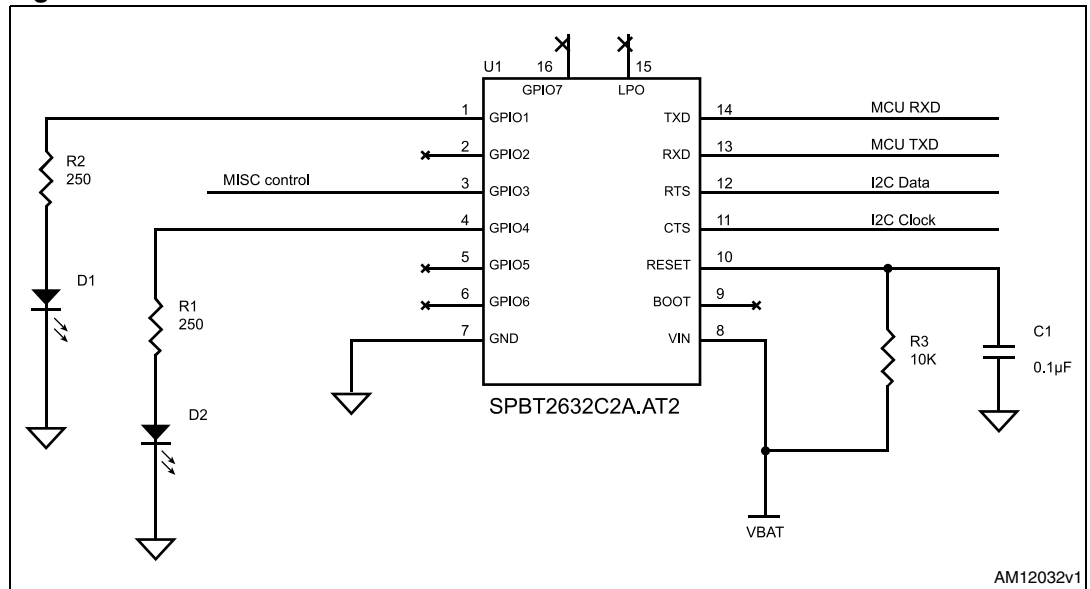


Figure 13. Co-processor

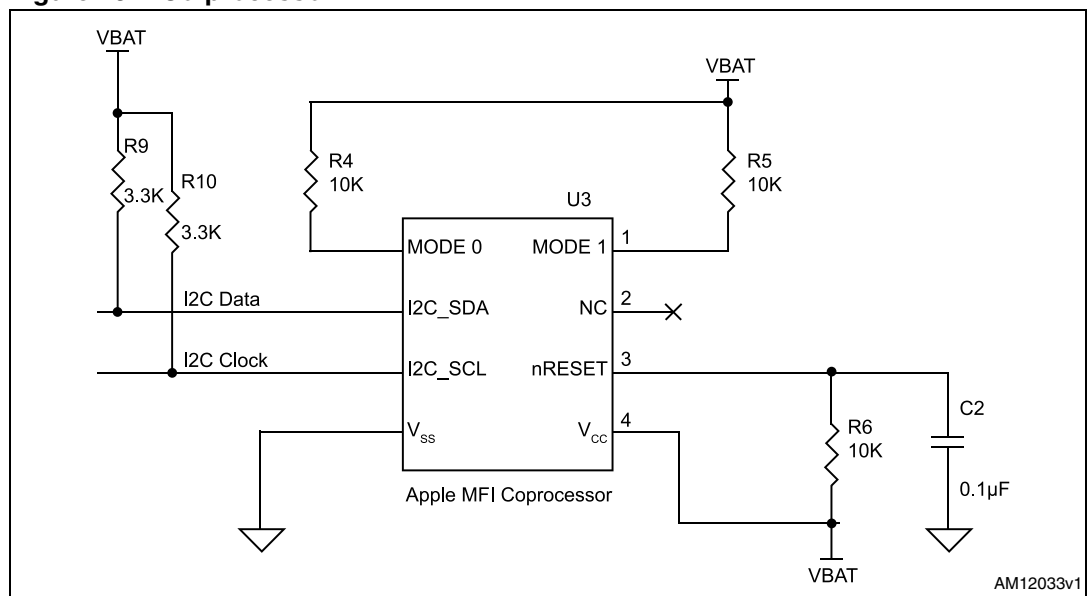
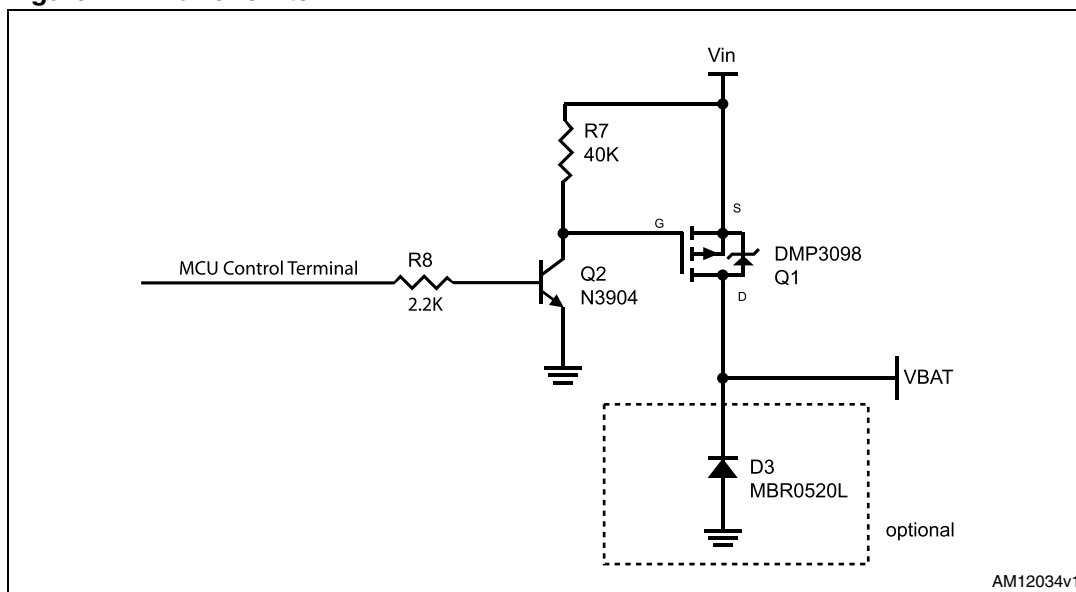


Figure 14. Power switch



8 Regulatory compliance

- FCC and IC
 - This module has been tested and found to comply with the FCC part 15 and IC RSS-210 rules. These limits are designed to provide reasonable protection against harmful interference in approved installations. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference may not occur in a particular installation.
This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Modifications or changes to this equipment not expressly approved by the part responsible for compliance may render void the user's authority to operate this equipment.
 - Modular approval, FCC and IC
FCC ID: X3ZBTMOD4
IC: 8828A-MOD4
In accordance with FCC part 15, the SPBT2632C2A.AT2 is listed above as a modular transmitter device.
 - Label instructions
When integrating the SPBT2632C2A.AT2 into the final product, it must be ensured that the FCC labelling requirements, as specified below, are satisfied. Based on the Public Notice from FCC, the product into which the ST transmitter module is installed must display a label referring to the enclosed module. The label should use wording such as the following:
Contains Transmitter Module
FCC ID: X3ZBTMOD4
IC: 8828A-MOD4
Any similar wording that expresses the same meaning may be used.
- BQB
 - BQB qualified design, QD ID: B019224
 - Product type: End Product
 - TGP version: Core 3.0
 - Core spec version: 3.0
 - Product descriptions: Bluetooth module, spec V3.0

- CE
 - CE Expert opinion: 0448-ARAM00003
 - Measurements have been performed in accordance with (report available on request):
 - EN 300 328 V 1.7.1 (2006-10) ^(a)
 - EN 301 489-17 V 2.1.1 (2009) ^(b)
 - EN60950-1:2006 +A11:2009+A1:2010 ^(c)
- CE certified:



-
- a. EN 300 328 V 1.7.1 (2006-10): “electromagnetic compatibility and radio spectrum Matters (ERM); Wideband transmission systems; data transmission equipment operating in the 2.4 GHz ISM band and using wideband modulation techniques; harmonized EN covering essential requirements under article 3.2 of the R&TTE directive”.
- b. EN 301 489-17 V 2.1.1 (2009): “electromagnetic compatibility and radio spectrum Matters (ERM); electromagnetic compatibility (EMC) standard for radio equipment and services; part 17: specific condition for 2.4 GHz wideband transmission systems and 5 GHz high performance RLAN equipment”.
- c. EN60950-1:2006 +A11:2009+A1:2010: “Information technology equipment - safety”.

9 Ordering information

Table 10. Ordering information

Order code	Description
SPBT2632C2A.AT2	Class 2 OEM Bluetooth antenna module

10 Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Apr-2012	1	First release.
16-Apr-2012	2	Modified: Section 8
12-Jun-2012	3	– Document status promoted from preliminary data to production data – Modified: Figure 1
07-Aug-2012	4	– Added: notes in Table 6 and 7 – Modified: Section 7

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