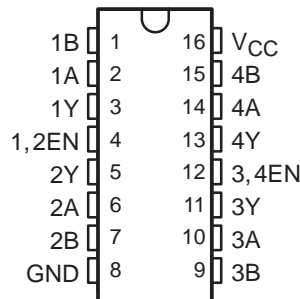


SN55LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVER

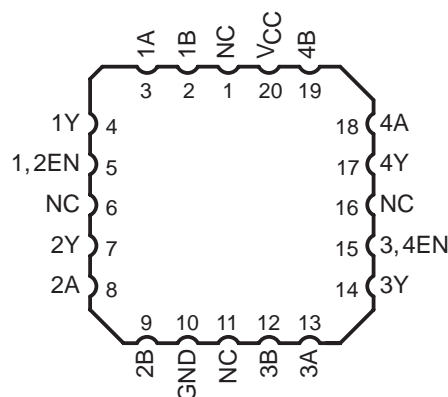
SGLS083A – MARCH 1995 – REVISED JUNE 2000

- Meets EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11
- Designed to Operate With Pulse Durations as Short as 20 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Input Sensitivity . . . ± 200 mV
- Low-Power Consumption . . . 20 mA Max
- Open-Circuit Fail-Safe Design
- Common-Mode Input Voltage Range of -7 V to 12 V

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC175 is a monolithic quadruple differential line receiver with 3-state outputs and is designed to meet the requirements of the EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The receivers are enabled in pairs with an active-high enable input. Each differential receiver input features high impedance, hysteresis for increased noise immunity, and sensitivity of ± 200 mV over a common-mode input voltage range of 12 V to -7 V. Fail-safe design ensures that if the inputs are open-circuited, the outputs are always high. This device is designed using the Texas Instruments proprietary LinBiCMOS™ technology allowing low power consumption, high switching speeds, and robustness.

This device offers optimum performance when used with the SN55LBC174 quadruple line driver. The SN55LBC175 is available in the 16-pin CDIP (J) package, a 16-pin CPAK (W) package, or a 20-pin LCCC (FK) package.

The SN55LBC175 is characterized over the military temperature range of -55°C to 125°C .

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

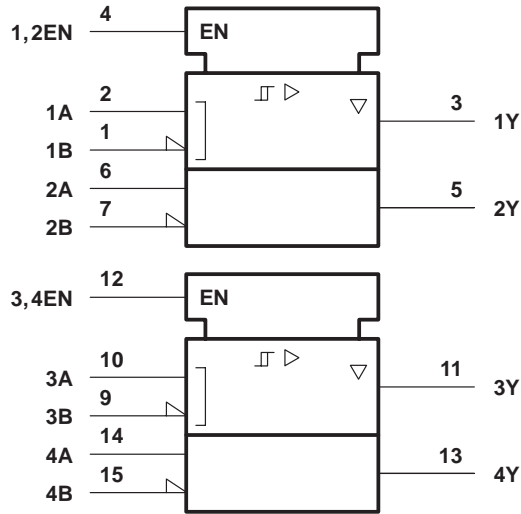
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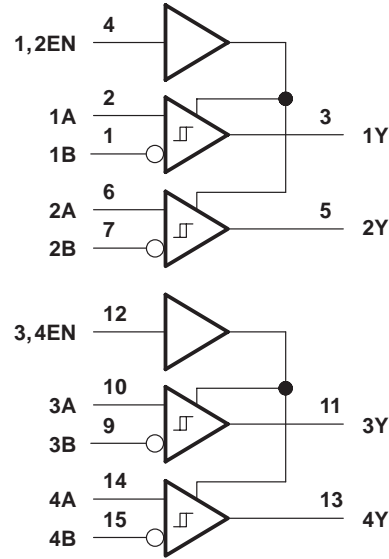
SN55LBC175 QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVER

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logic symbol†



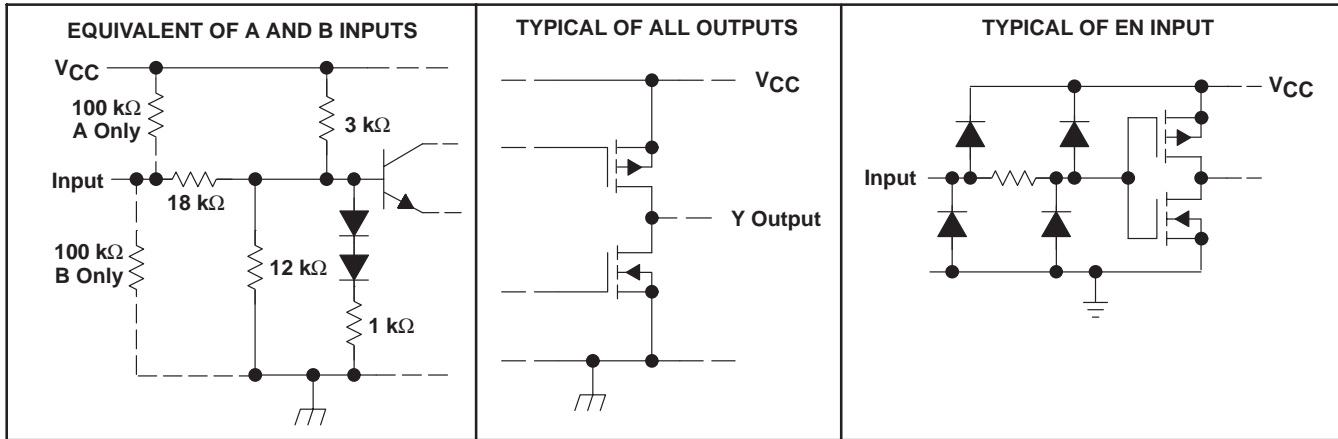
logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J or W package.

schematics of inputs and outputs



SN55LBC175

QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Input voltage, A or B inputs, V_I	±25 V
Differential input voltage, V_{ID} (see Note 2)	±25 V
Data and control voltage range	–0.3 V to 7 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}	–7		12	V
Differential input voltage, V_{ID}			±6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}				
			0.8	V
High-level output current, I_{OH}			–8	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	–55		125	°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V_{IT+}	Positive-going input threshold voltage	$I_O = -8$ mA			0.2	V	
V_{IT-}	Negative-going input threshold voltage	$I_O = 8$ mA	-0.2			V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			45		mV	
V_{IK}	Enable input clamp voltage	$I_I = -18$ mA		-0.9	-1.5	V	
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA	3.5	4.5		V	
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 8$ mA		0.3	0.5	V	
		$V_{ID} = -200$ mV, $I_{OL} = 8$ mA, $T_A = 125^\circ\text{C}$			0.7		
I_{OZ}	High-impedance-state output current	$V_O = 0$ V to V_{CC}			± 20	μA	
I_I	Bus input current	A or B inputs	$V_{IH} = 12$ V, $V_{CC} = 5$ V, Other inputs at 0 V		0.7	1	mA
			$V_{IH} = 12$ V, $V_{CC} = 0$ V, Other inputs at 0 V		0.8	1	
			$V_{IH} = -7$ V, $V_{CC} = 5$ V, Other inputs at 0 V		-0.5	-0.8	
			$V_{IH} = -7$ V, $V_{CC} = 0$ V, Other inputs at 0 V		-0.4	-0.8	
I_{IH}	High-level enable input current	$V_{IH} = 5$ V			± 20	μA	
I_{IL}	Low-level enable input current	$V_{IL} = 0$ V			-20	μA	
I_{OS}	Short-circuit output current	$V_O = 0$		-80	-120	mA	
I_{CC}	Supply current	Outputs enabled, $I_O = 0$, $V_{ID} = 5$ V		11	20	mA	
		Outputs disabled		0.9	1.4		

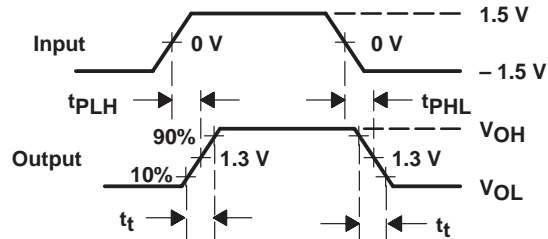
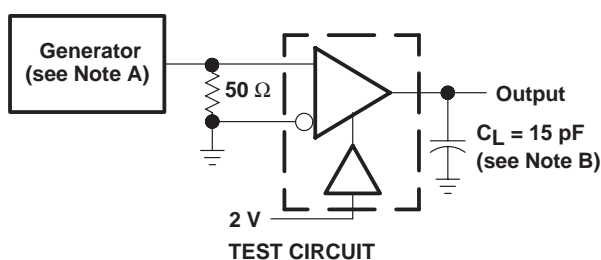
† All typical values are at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5$ V, $C_L = 15$ pF

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	$V_{ID} = -1.5$ V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			-55°C to 125°C			35	
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5$ V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			-55°C to 125°C			35	
t_{PZH}	Output enable time to high level	See Figure 2	25°C		17	40	ns
			-55°C to 125°C			45	
t_{PZL}	Output enable time to low level	See Figure 3	25°C		18	30	ns
			-55°C to 125°C			35	
t_{PHZ}	Output disable time from high level	See Figure 2	25°C		30	40	ns
			-55°C to 125°C			55	
t_{PLZ}	Output disable time from low level	See Figure 3	25°C		23	30	ns
			-55°C to 125°C			45	
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)	See Figure 1	25°C		4	6	ns
			-55°C to 125°C			7	
t_t	Transition time	See Figure 1	25°C		3	10	ns
			-55°C to 125°C			16	



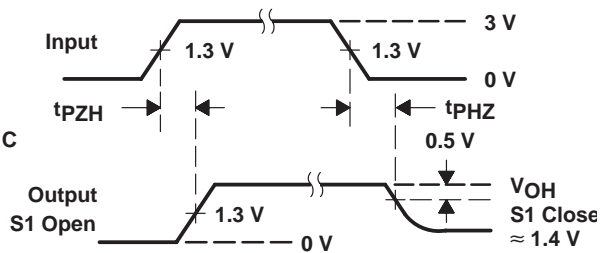
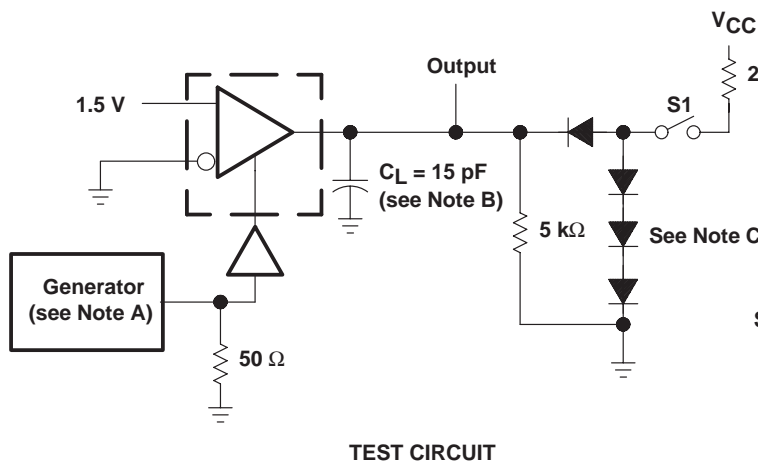
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle $\leq 50\%$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



VOLTAGE WAVEFORMS

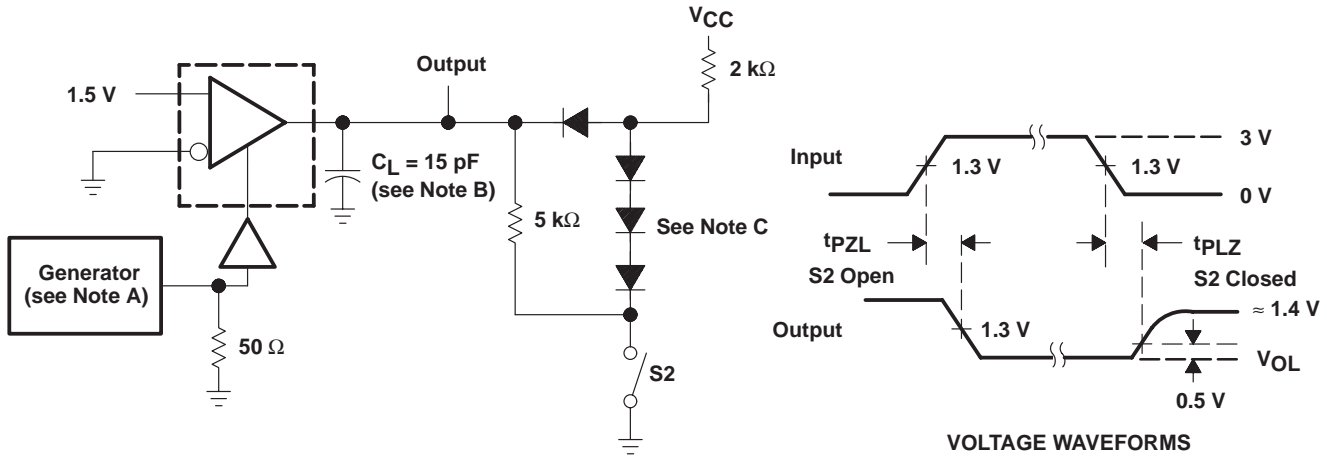
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle $\leq 50\%$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N916 or equivalent.

Figure 2. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N916 or equivalent.

Figure 3. t_{pZL} and t_{PLZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

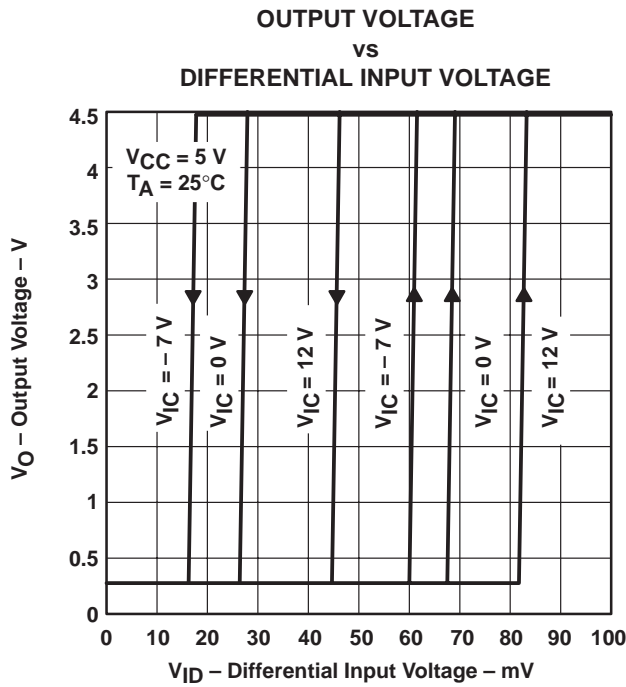


Figure 4

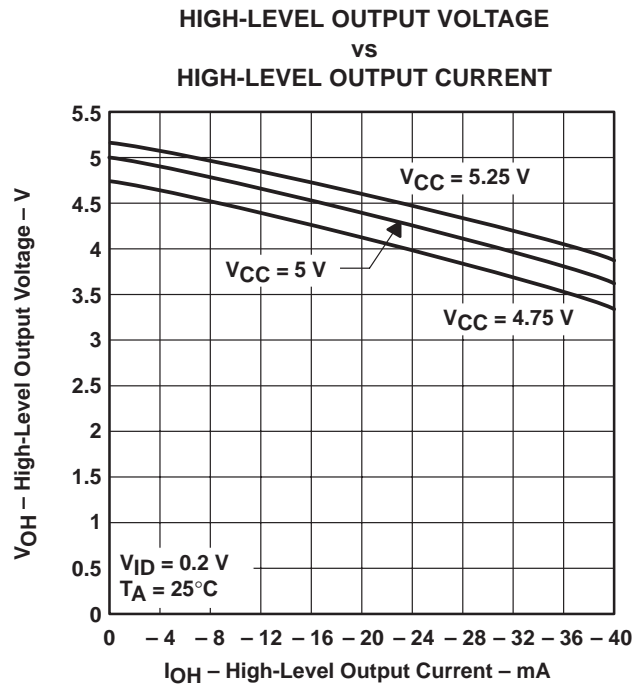


Figure 5

TYPICAL CHARACTERISTICS

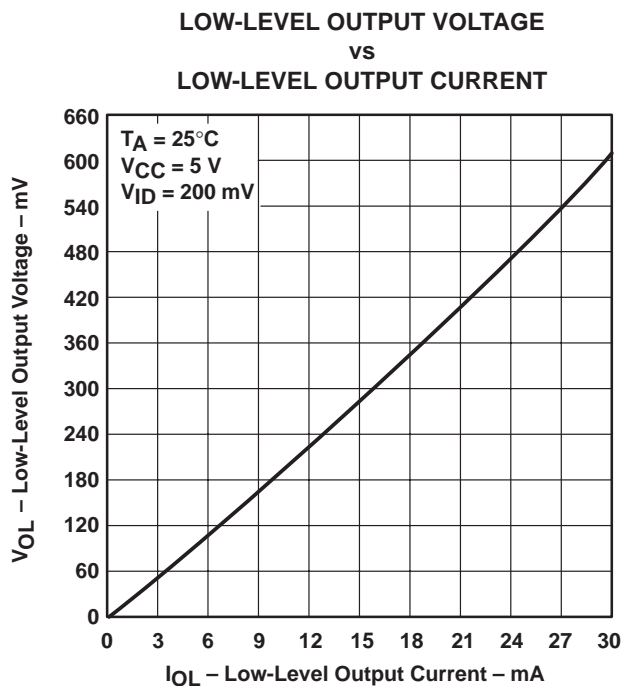


Figure 6

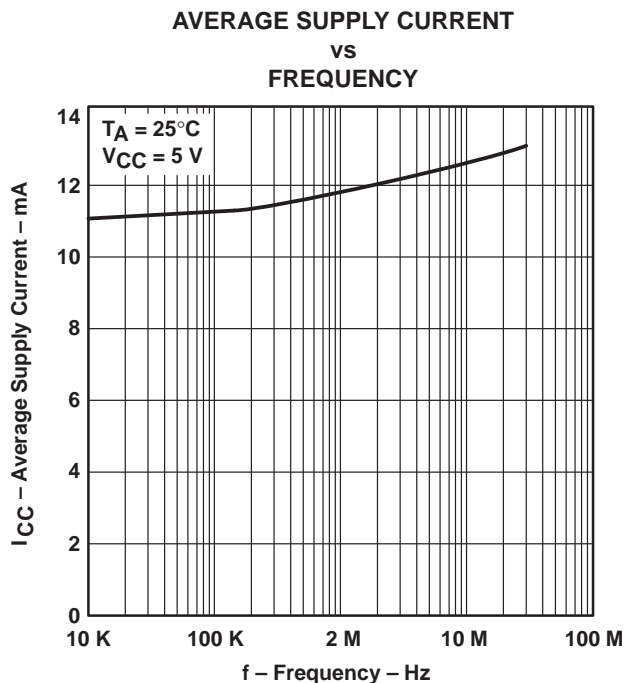


Figure 7

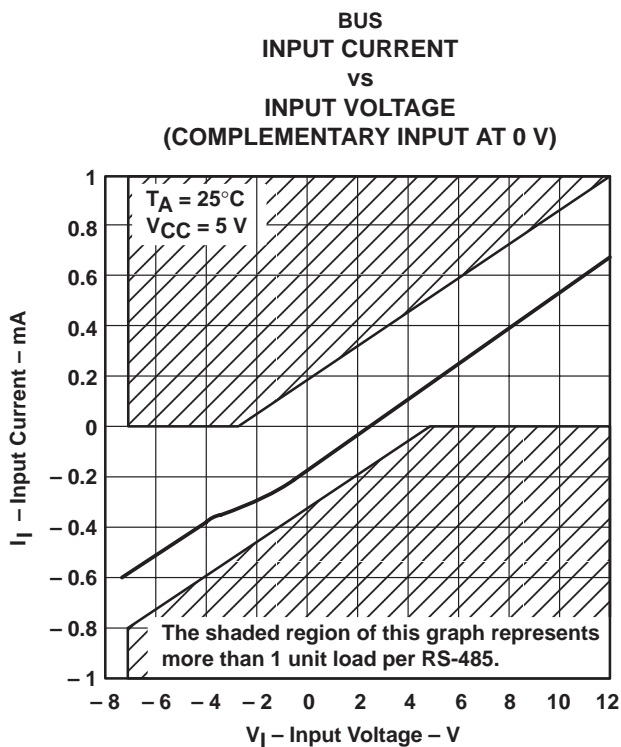


Figure 8

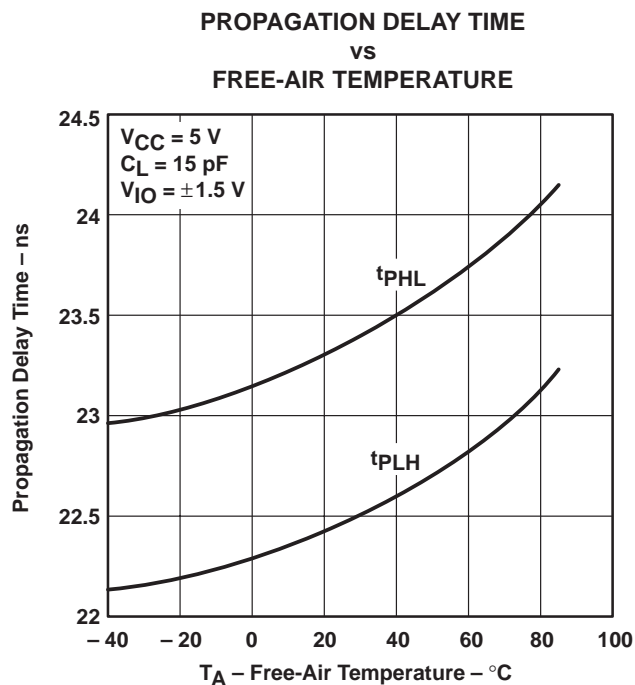


Figure 9

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9076603Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9076603QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9076603QFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN55LBC175J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55LBC175FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55LBC175J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55LBC175W	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

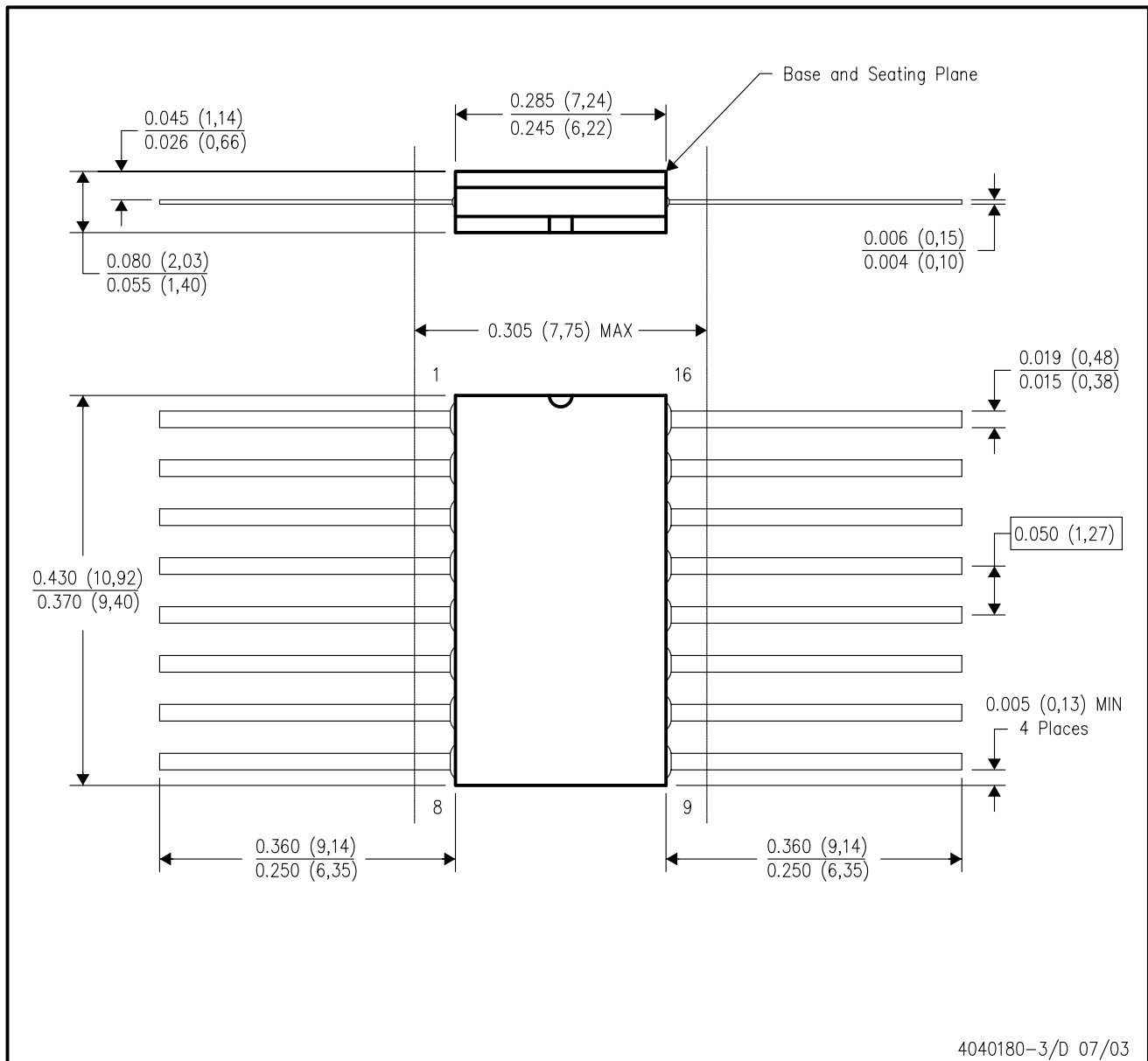


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

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