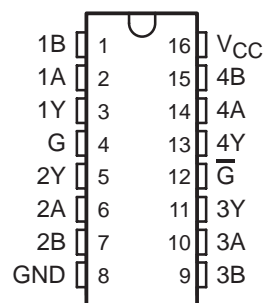


SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

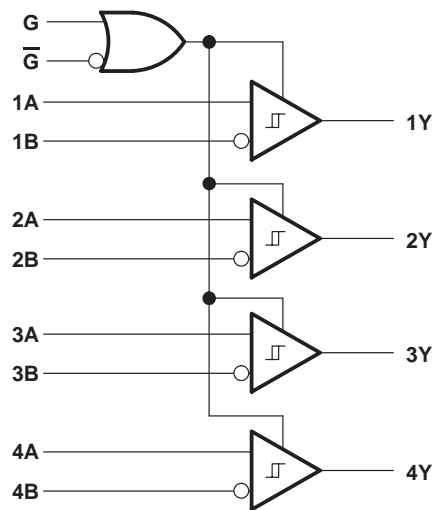
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- Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 Applications
- Signaling Rate† Exceeding 50 Mbps
- Fail-Safe in Bus Short-Circuit, Open-Circuit, and Idle-Bus Conditions
- ESD Protection on Bus Inputs Exceeds 6 kV
- Common-Mode Bus Input Range –7 V to 12 V
- Propagation Delay Times <16 ns
- Low Standby Power Consumption <20 μ A
- Pin-Compatible Upgrade for AM26LS32, DS96F173, LTC488, and SN75173

SN65LBC173A (Marked as 65LBC173A)
SN75LBC173A (Marked as 75LBC173A)
D or N PACKAGE
(TOP VIEW)



logic diagram



description

The SN65LBC173A and SN75LBC173A are quadruple differential line receivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications.

These devices are optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

Each receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS™, facilitating low power consumption and robustness.

The G and \bar{G} inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

The SN75LBC173A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC173A is characterized over the temperature range from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

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FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B (V_{ID})	ENABLES		OUTPUT Y
	G	\bar{G}	
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	
-0.2 V $< V_{ID} < -0.01$ V	H	X	?
	X	L	
-0.01 V $\leq V_{ID}$	H	X	H
	X	L	
X	L	H	Z
	OPEN	OPEN	
Short circuit	H	X	H
	X	L	
Open circuit	H	X	H

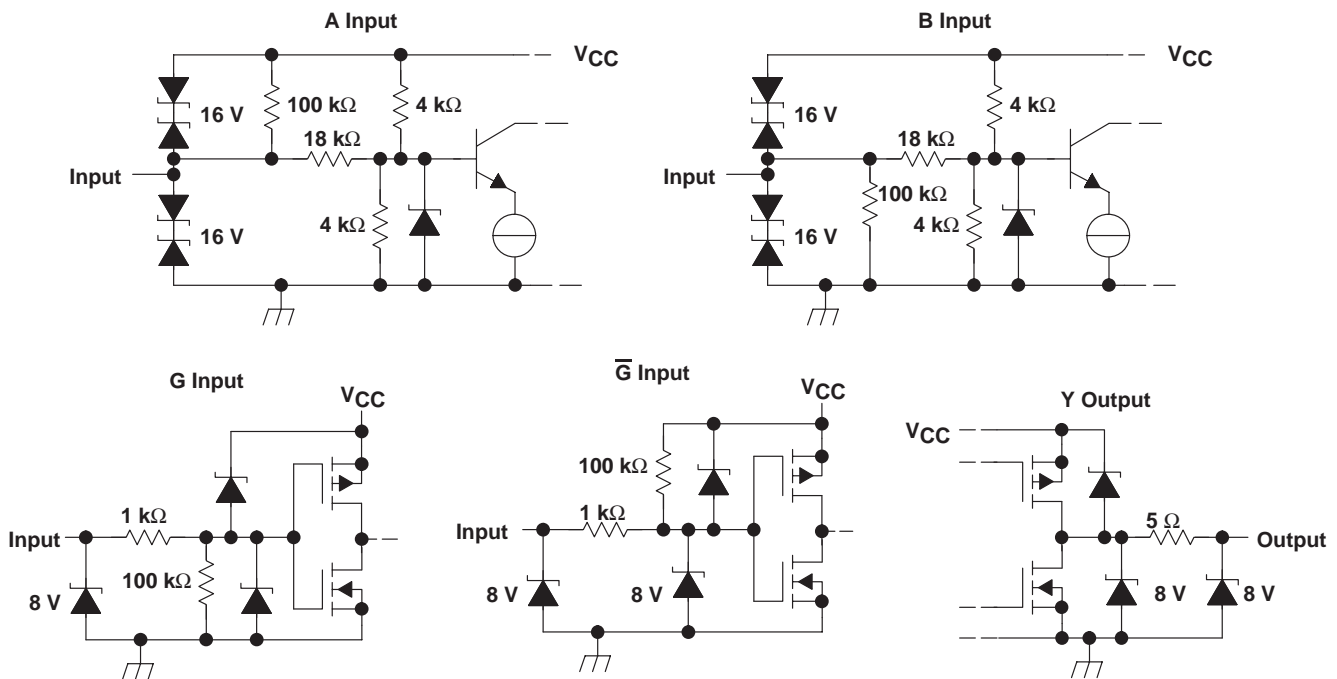
H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

AVAILABLE OPTIONS

T_A	PACKAGE	
	PLASTIC SMALL OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE (JEDEC MS-001)
0°C to 70°C	SN75LBC173AD	SN75LBC173AN
-40°C to 85°C	SN65LBC173AD	SN65LBC173AN

† Add an R suffix for taped and reeled

equivalent input and output schematic diagrams



SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Voltage range at any bus input (DC)	–10 V to 15 V
Voltage range at any bus input (transient pulse through 100 Ω , see Figure 5)	–30 V to 30 V
Voltage input range at G and \overline{G} , V_I	–0.5 V to $V_{CC} + 0.5$ V
Receiver output current, I_O	± 10 mA
Electrostatic discharge:	
Human body model (see Note 2):	A and B to GND 6 kV
	All pins 5 kV
Charged-device model (see Note 3):	All pins 2 kV
Continuous power dissipation	See Power Dissipation Rating Table

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to GND, and are steady-state (unless otherwise specified).
 2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
 3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	1080 mW	8.7 mW/ $^\circ\text{C}$	690 mW	560 mW
N	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW	598 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	A, B	–7		12	V
High-level input voltage, V_{IH}	G, \overline{G}	2	V_{CC}		V
Low-level input voltage, V_{IL}		0		0.8	
Output current	Y	–8		8	mA
Operating free-air temperature, T_A	SN75LBC173A	0		70	°C
	SN65LBC173A	–40		85	

SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

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electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	$-7\text{ V} \leq V_{CM} \leq 12\text{ V}$ ($V_{CM} = (V_A + V_B)/2$)	-80	-10		mV
V_{IT-}	Negative-going differential input voltage threshold		-200	-120		
V_{HYS}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		40			mV
V_{IK}	Input clamp voltage	$I_I = -18\text{ mA}$	-1.5	-0.8		V
V_{OH}	High-level output voltage	$V_{ID} = 200\text{ mV}$, $I_{OH} = -8\text{ mA}$	2.7	4.8		V
V_{OL}	Low-level output voltage	$V_{ID} = -200\text{ mV}$, $I_{OL} = 8\text{ mA}$				
I_{OZ}	High-impedance-state output current	$V_O = 0\text{ V}$ to V_{CC}	-1		1	μA
I_I	Line input current	Other input at 0 V, $V_{CC} = 0\text{ V}$ or 5 V	$V_I = 12\text{ V}$		0.9	mA
			$V_I = -7\text{ V}$		-0.7	
I_{IH}	High-level input current	Enable inputs G, \bar{G}			100	μA
I_{IL}	Low-level input current				-100	μA
R_I	Input resistance	A, B inputs	12			$\text{k}\Omega$
I_{CC}	Supply current	$V_{ID} = 5\text{ V}$	G at 0 V, \bar{G} at V_{CC}		20	μA
		No load	G at V_{CC} , \bar{G} at 0 V		11 16	mA

† All typical values are at $V_{CC} = 5\text{ V}$ and 25°C .

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Output rise time	$V_{ID} = -3\text{ V}$ to 3 V , See Figure 2		2	4	ns
t_f	Output fall time			2	4	ns
t_{PLH}	Propagation delay time, low-to-high level output		9	12	16	ns
t_{PHL}	Propagation delay time, high-to-low level output		9	12	16	ns
t_{pZH}	Propagation delay time, high-impedance to high-level output	See Figure 3		27	38	ns
t_{pHZ}	Propagation delay time, high-level to high-impedance output			7	16	ns
t_{pZL}	Propagation delay time, high-impedance to low level output	See Figure 4		29	38	ns
t_{pLZ}	Propagation delay time, low-level to high-impedance output			12	16	ns
$t_{sk(p)}$	Pulse skew ($ t_{PLH} - t_{PHL} $)			0.2	1	ns
$t_{sk(o)}$	Output skew (see Note 4)				2	ns
$t_{sk(pp)}$	Part-to-part skew (see Note 5)				2	ns

† All typical values are at $V_{CC} = 5\text{ V}$ and 25°C .

- NOTES:
- Outputs skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
 - Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

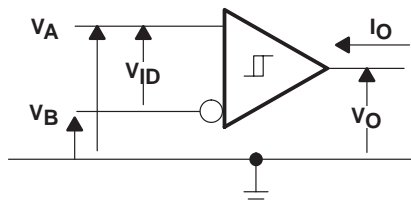


Figure 1. Voltage and Current Definitions

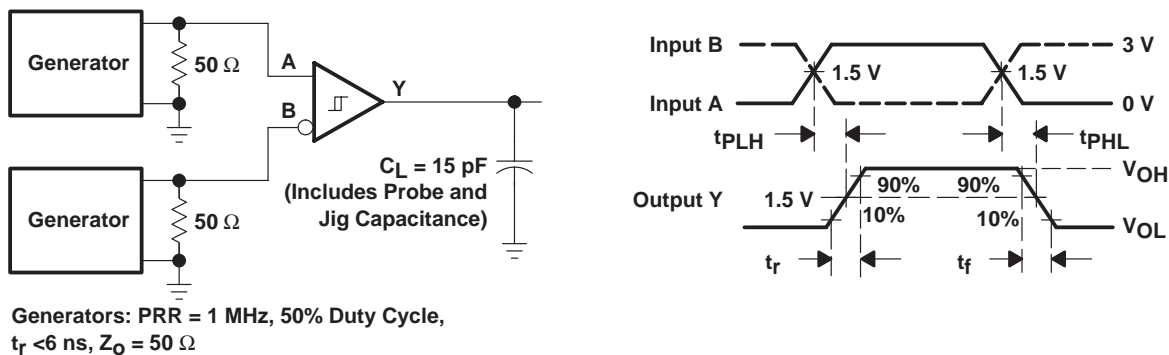


Figure 2. Switching Test Circuit and Waveforms

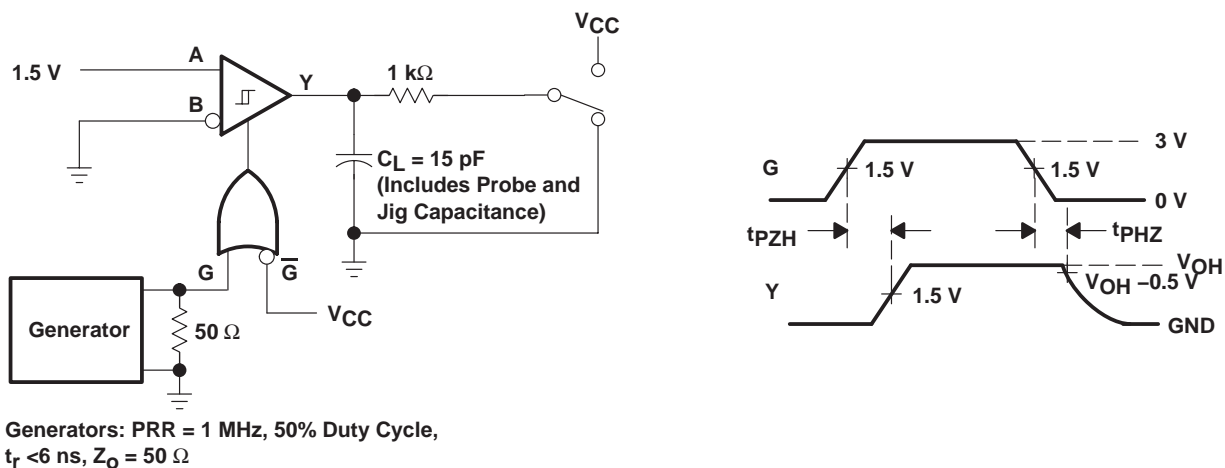
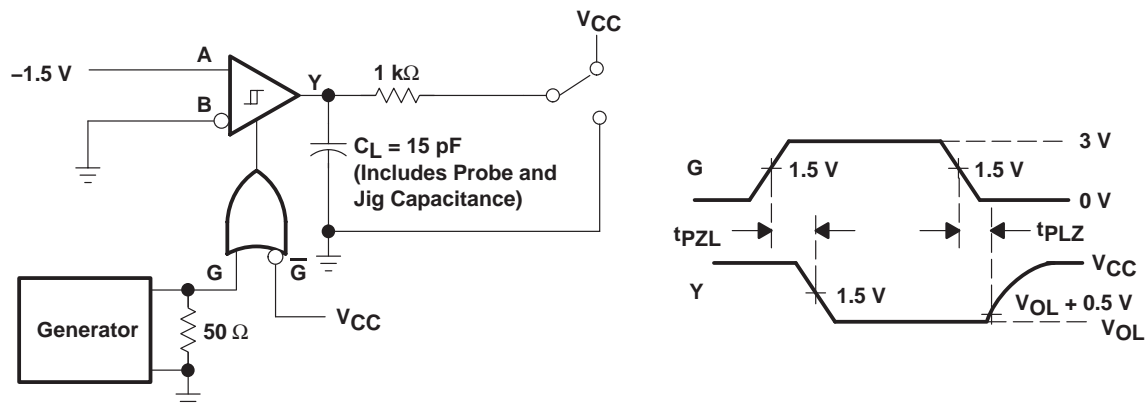


Figure 3. Test Circuit Waveforms, t_{PZH} and t_{PHZ}

SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

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PARAMETER MEASUREMENT INFORMATION



Generators: PRR = 1 MHz, 50% Duty Cycle,
 $t_r < 6 \text{ ns}$, $Z_o = 50 \Omega$

Figure 4. Test Circuit Waveforms, t_{pZL} and t_{pLZ}

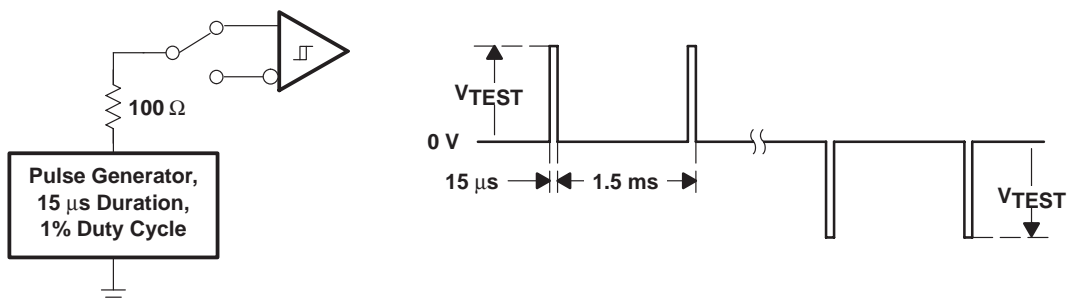


Figure 5. Test Circuit and Waveform, Transient Over-Voltage Test

TYPICAL CHARACTERISTICS

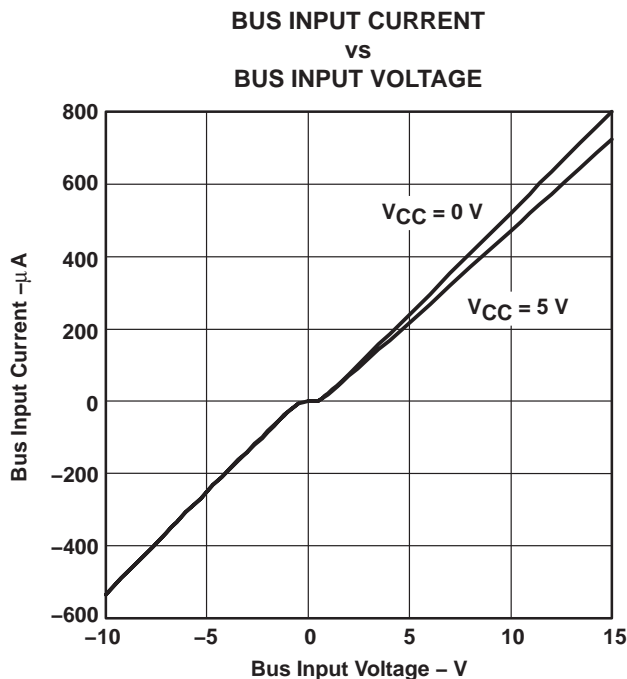


Figure 6

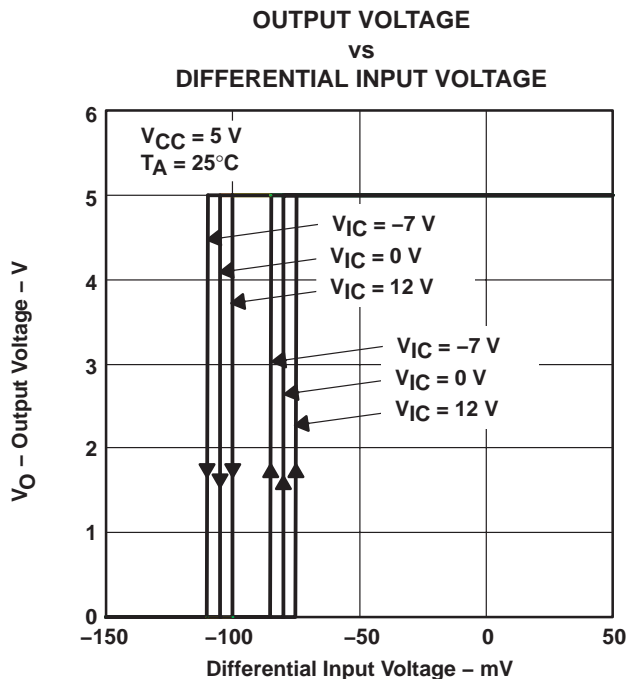


Figure 7

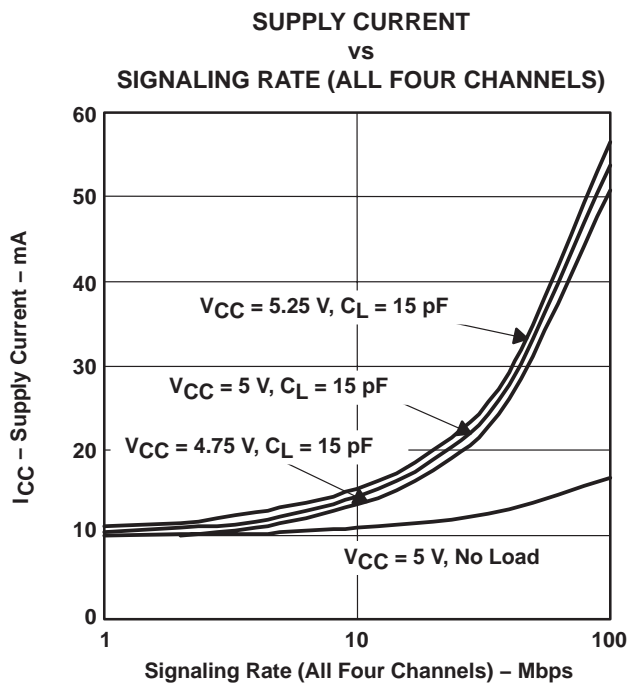


Figure 8

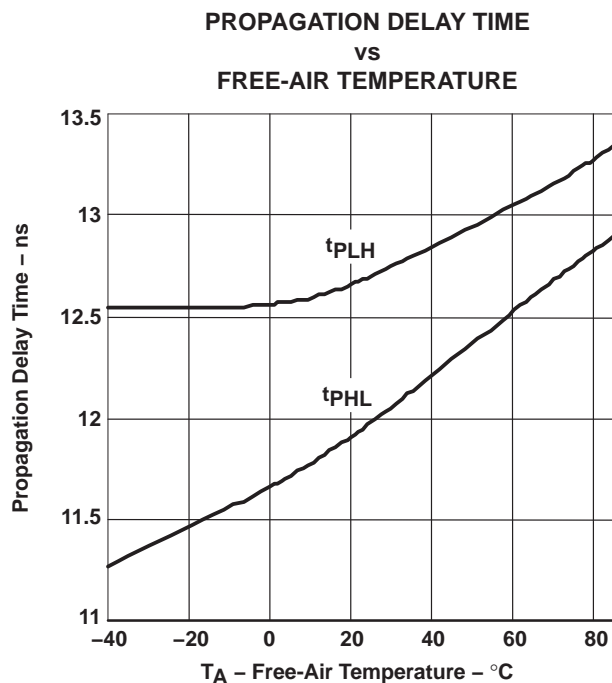


Figure 9

SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

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TYPICAL CHARACTERISTICS

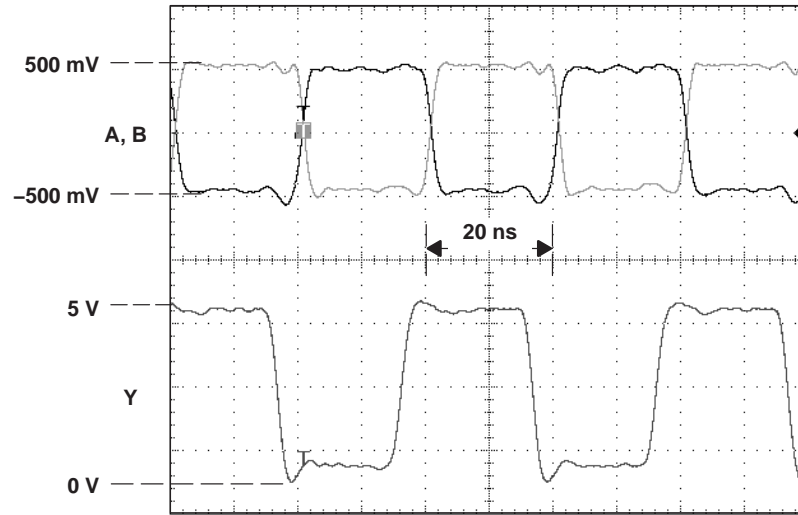


Figure 10. Receiver Inputs and Outputs, 50 Mbps Signaling Rate

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APPLICATION INFORMATION

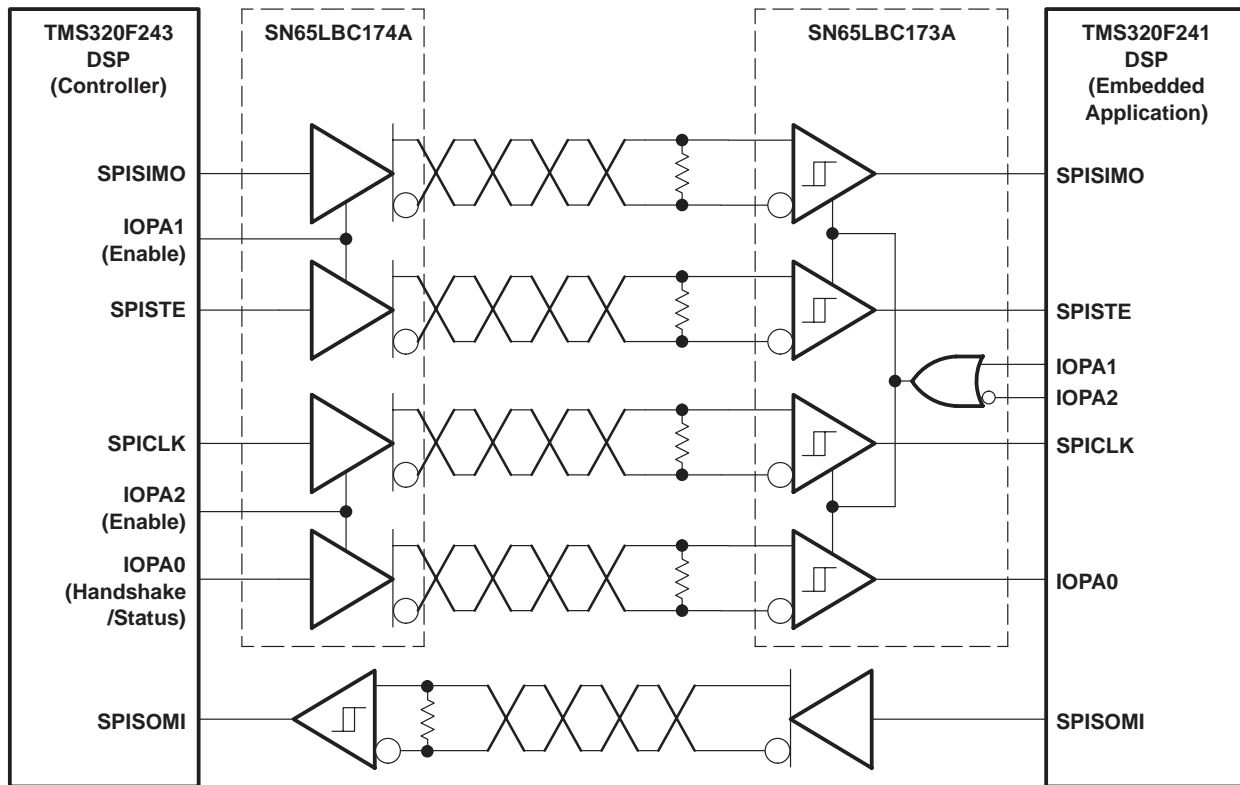


Figure 11. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

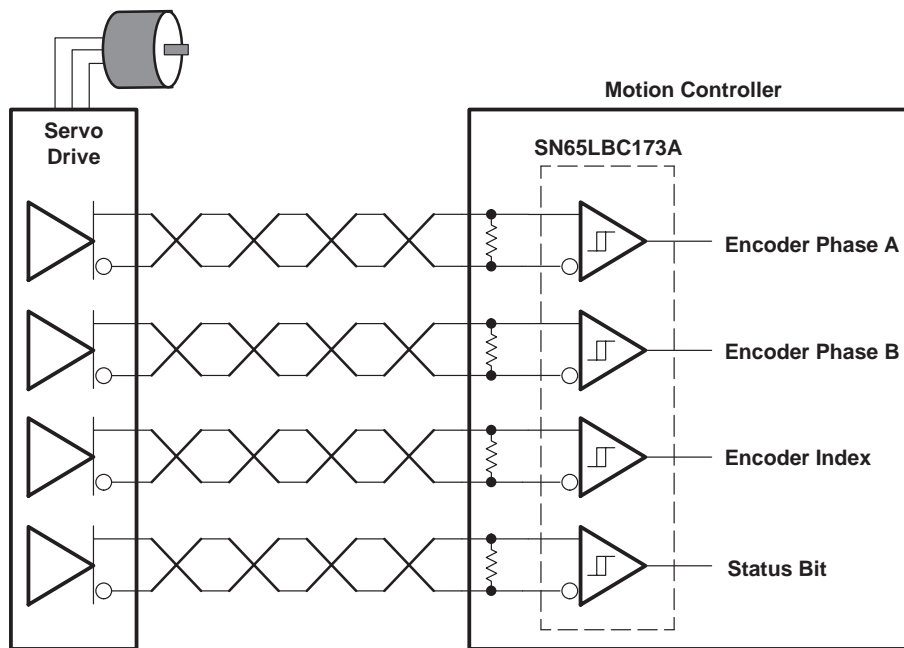


Figure 12. Typical Application Circuit, High-Speed Servomotor Encoder Interface

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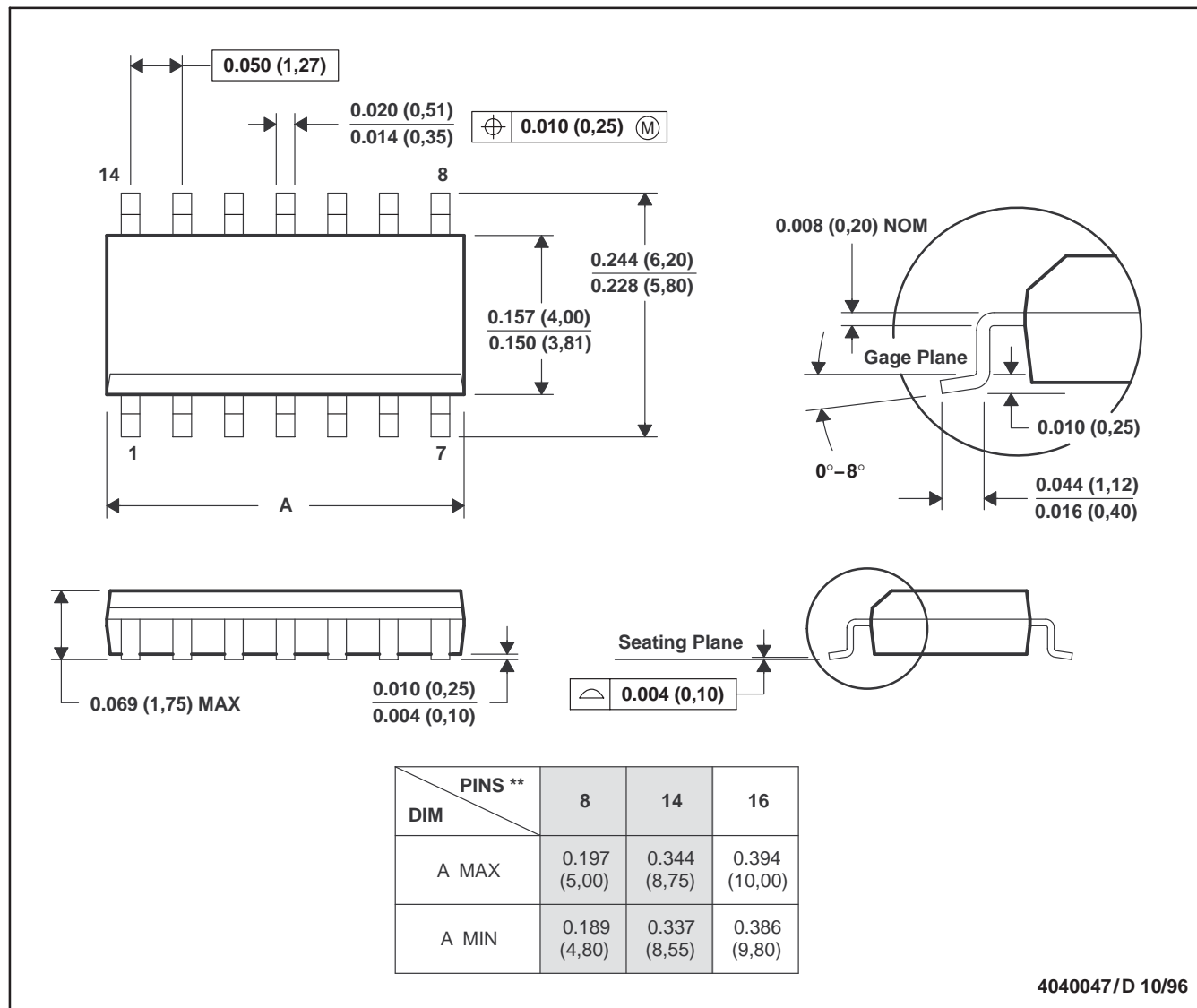
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

SN65LBC173A, SN75LBC173A QUADRUPLE RS-485 DIFFERENTIAL LINE RECEIVERS

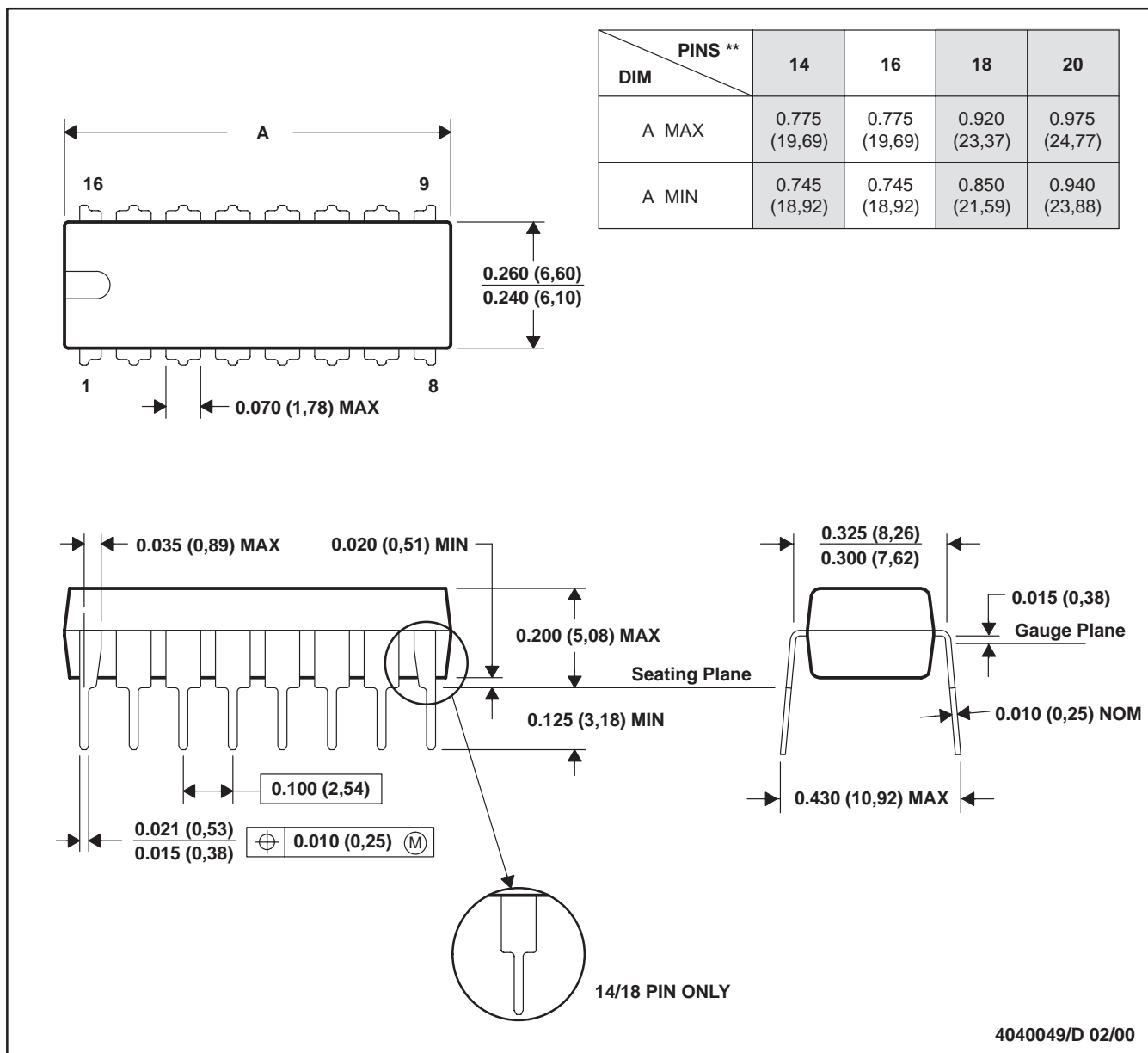
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MECHANICAL DATA

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LBC173AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC173ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC173ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC173ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC173AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC173ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC173AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC173ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC173ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC173ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC173AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC173ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

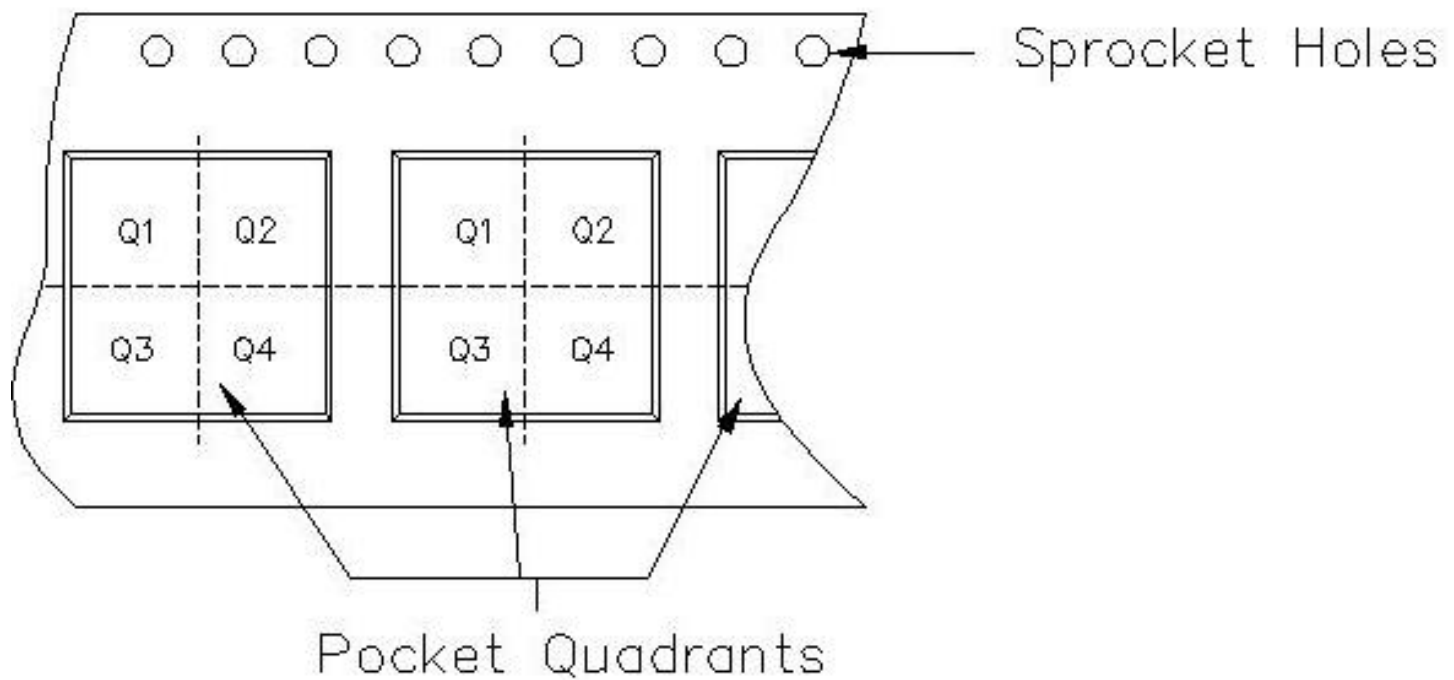
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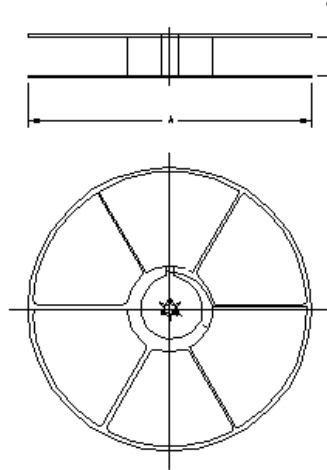
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



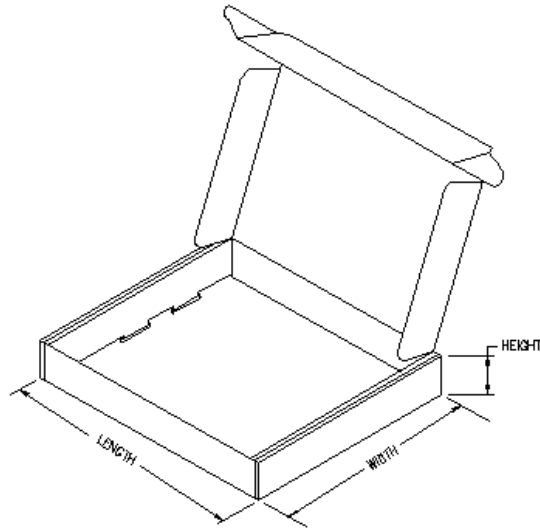
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC173ADR	D	16	FMX	330	0	6.5	10.3	2.1	8	16	Q1
SN75LBC173ADR	D	16	FMX	330	0	6.5	10.3	2.1	8	16	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65LBC173ADR	D	16	FMX	342.9	336.6	28.58
SN75LBC173ADR	D	16	FMX	342.9	336.6	28.58



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

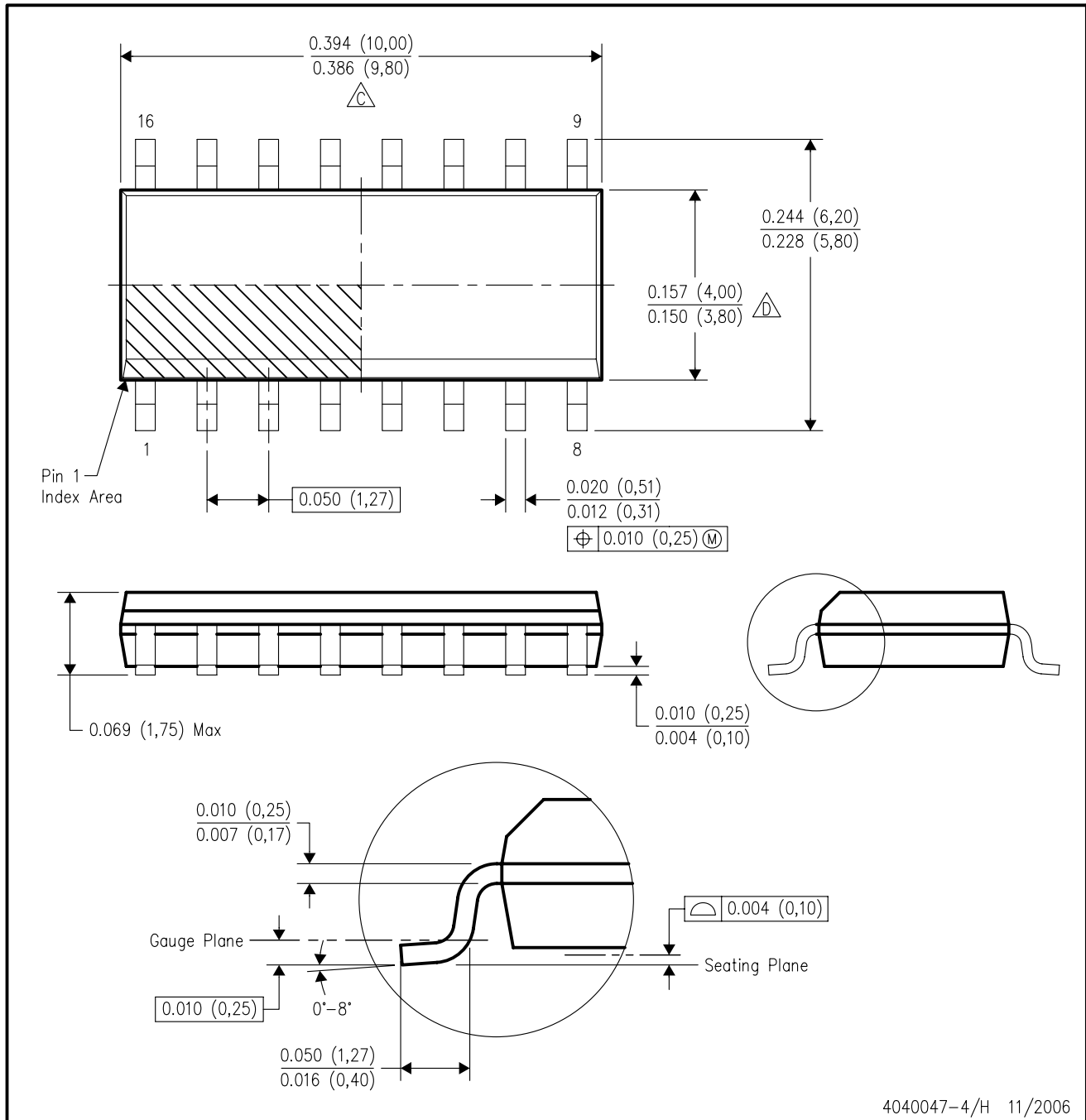
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

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