

SN74LVC1G80-Q1 Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - ± 4000 -V Human-Body Model (HBM) ESD Classification Level 3A
 - ± 1000 -V Charged-Device Model (CDM) ESD Classification Level C5
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 6 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} supports Partial-Power-Down Mode and Back-Drive Protection

2 Applications

- Automotive Infotainment
- Automotive Cluster
- Automotive ADAS
- Automotive Body Electronics
- Automotive HEV/EV Powertrain

3 Description

The SN74LVC1G80-Q1 device is an automotive AEC-Q100 qualified, single positive-edge-triggered D-type flip-flop that is designed for 1.65-V to 5.5-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the \bar{Q} output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

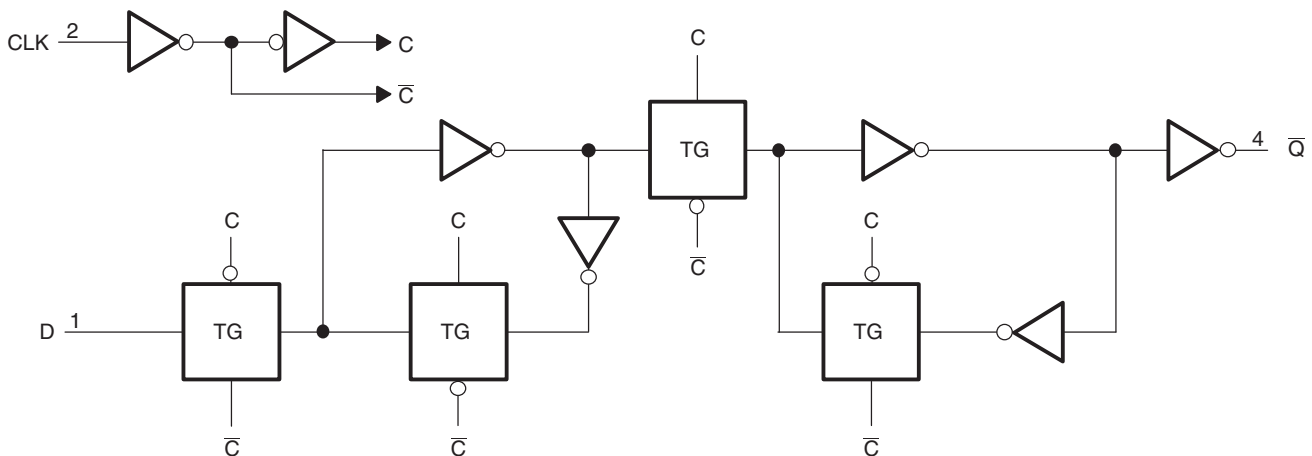
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC1G80-Q1	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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(1) TG - Transmission Gate



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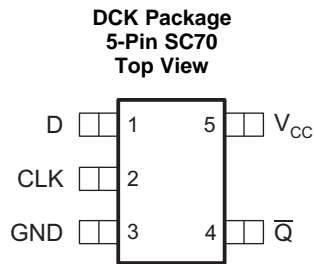
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2017	*	Initial release.

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

PIN		I/O	DESCRIPTION
NO.	NAME		
1	D	I	Data input
2	CLK	I	Positive-Edge-Triggered Clock input
3	GND	—	Ground pin
4	\bar{Q}	O	Inverted output
5	V _{CC}	—	Positive Supply

(1) See [Mechanical, Packaging, and Orderable Information](#) for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
V _{CC} Supply voltage	–0.5	6.5	V
V _I Input voltage ⁽²⁾	–0.5	6.5	V
V _O Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	–0.5	V _{CC} + 0.5	V
I _{IK} Input clamp current	V _I < 0		–50 mA
I _{OK} Output clamp current	V _O < 0		–50 mA
I _O Continuous output current			±50 mA
Continuous current through V _{CC} or GND			±100 mA
T _J Junction temperature			150 °C
T _{stg} Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in .

6.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000
	Charged-device model (CDM), per AEC Q100-011	±1000

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4	mA
		V _{CC} = 2.3 V		–8	
		V _{CC} = 3 V		–16	
		V _{CC} = 4.5 V		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature	–40	125	°C	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G80-Q1	UNIT
		DCK (SC70)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	278.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	121.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	65.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	64.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OH}	I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} - 0.1			V	
	I _{OH} = -4 mA	1.65 V	1.2				
	I _{OH} = -8 mA	2.3 V	1.9				
	I _{OH} = -16 mA	3 V	2.4				
	I _{OH} = -24 mA		2.3				
	I _{OH} = -32 mA	4.5 V	3.8				
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V	0.1			V	
	I _{OL} = 4 mA	1.65 V	0.45				
	I _{OL} = 8 mA	2.3 V	0.3				
	I _{OL} = 16 mA	3 V	0.4				
	I _{OL} = 24 mA		0.55				
	I _{OL} = 32 mA	4.5 V	0.55				
I _I	CLK or D inputs	V _I = 5.5 V or GND	0 to 5.5 V		±10	μA	
I _{off}		V _I or V _O = 5.5 V	0		±10	μA	
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	μA	
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	μA	
C _i		V _I = V _{CC} or GND	T _A = -40°C to 85°C		3.3 V	3.5	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements: T_A = -40°C to +85°C

over recommended operating free-air temperature range, T_A = -40°C to +85°C (unless otherwise noted) (see [Figure 3](#))

		V _{CC}	MIN	MAX	UNIT
f _{clock}	Clock frequency	V _{CC} = 1.8 V ± 0.15 V	160		MHz
		V _{CC} = 2.5 V ± 0.2 V			
		V _{CC} = 3.3 V ± 0.3 V			
		V _{CC} = 5.5 V ± 0.5 V			
t _w	Pulse duration, CLK high or low	V _{CC} = 1.8 V ± 0.15 V	2.5		ns
		V _{CC} = 2.5 V ± 0.2 V			
		V _{CC} = 3.3 V ± 0.3 V			
		V _{CC} = 5.5 V ± 0.5 V			
t _{su}	Data high	V _{CC} = 1.8 V ± 0.15 V	2.3		ns
		V _{CC} = 2.5 V ± 0.2 V			
		V _{CC} = 3.3 V ± 0.3 V			
		V _{CC} = 5.5 V ± 0.5 V			
	Data low	V _{CC} = 1.8 V ± 0.15 V	2.5		
		V _{CC} = 2.5 V ± 0.2 V			
		V _{CC} = 3.3 V ± 0.3 V			
		V _{CC} = 5.5 V ± 0.5 V			
t _h	Hold time, data after CLK↑	V _{CC} = 1.8 V ± 0.15 V	0		ns
		V _{CC} = 2.5 V ± 0.2 V			
		V _{CC} = 3.3 V ± 0.3 V			
		V _{CC} = 5.5 V ± 0.5 V			

6.7 Timing Requirements: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

 over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted) (see [Figure 3](#))

		V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160	160	MHz
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_w	Pulse duration, CLK high or low	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.5	2.5	ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_{su}	Data high	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.3	2.3	ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
	Data low	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	2.5	2.5	
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			
t_h	Hold time, data after CLK \uparrow	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	0	0	ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
		$V_{CC} = 5.5\text{ V} \pm 0.5\text{ V}$			

6.8 Switching Characteristics: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 15\text{ pF}$

 over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 15\text{ pF}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160	160	MHz
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			
t_{pd}	CLK	\bar{Q}	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	3	9.1	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			

6.9 Switching Characteristics: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF

 over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160	160	MHz
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			
t_{pd}	CLK	\bar{Q}	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	4.4	9.9	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			

6.10 Switching Characteristics: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF

over recommended operating free-air temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $C_L = 30\text{ pF}$ or 50 pF (unless otherwise noted) (see [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	160		MHz
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			
t_{pd}	CLK	\bar{Q}	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	4.4	12.5	ns
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	2.3	8.5	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2	6	
			$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1.3	5.5	

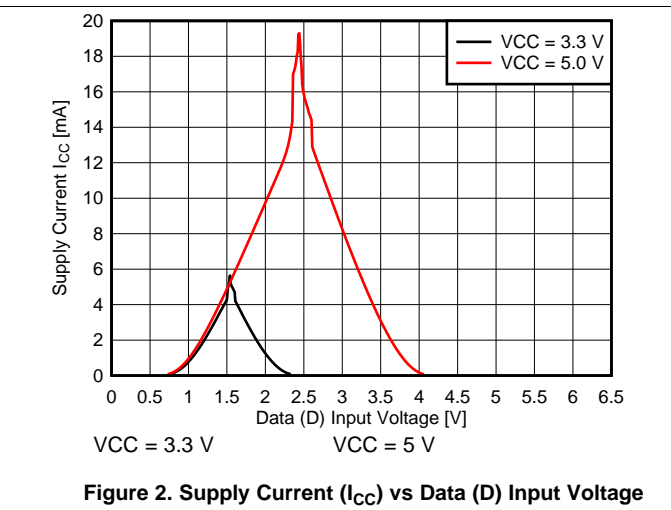
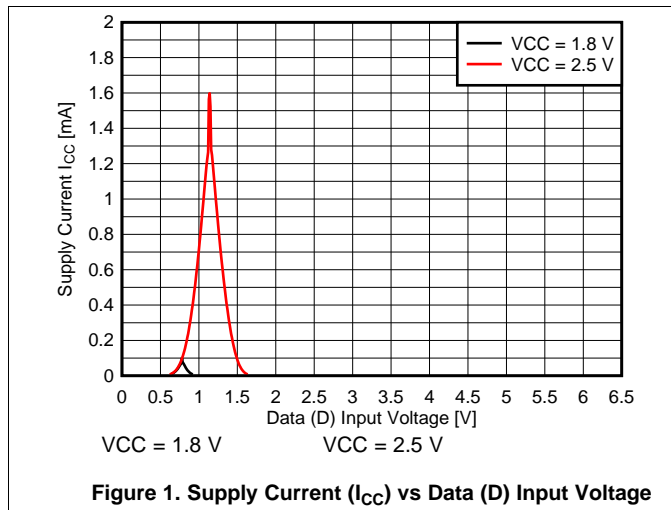
6.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

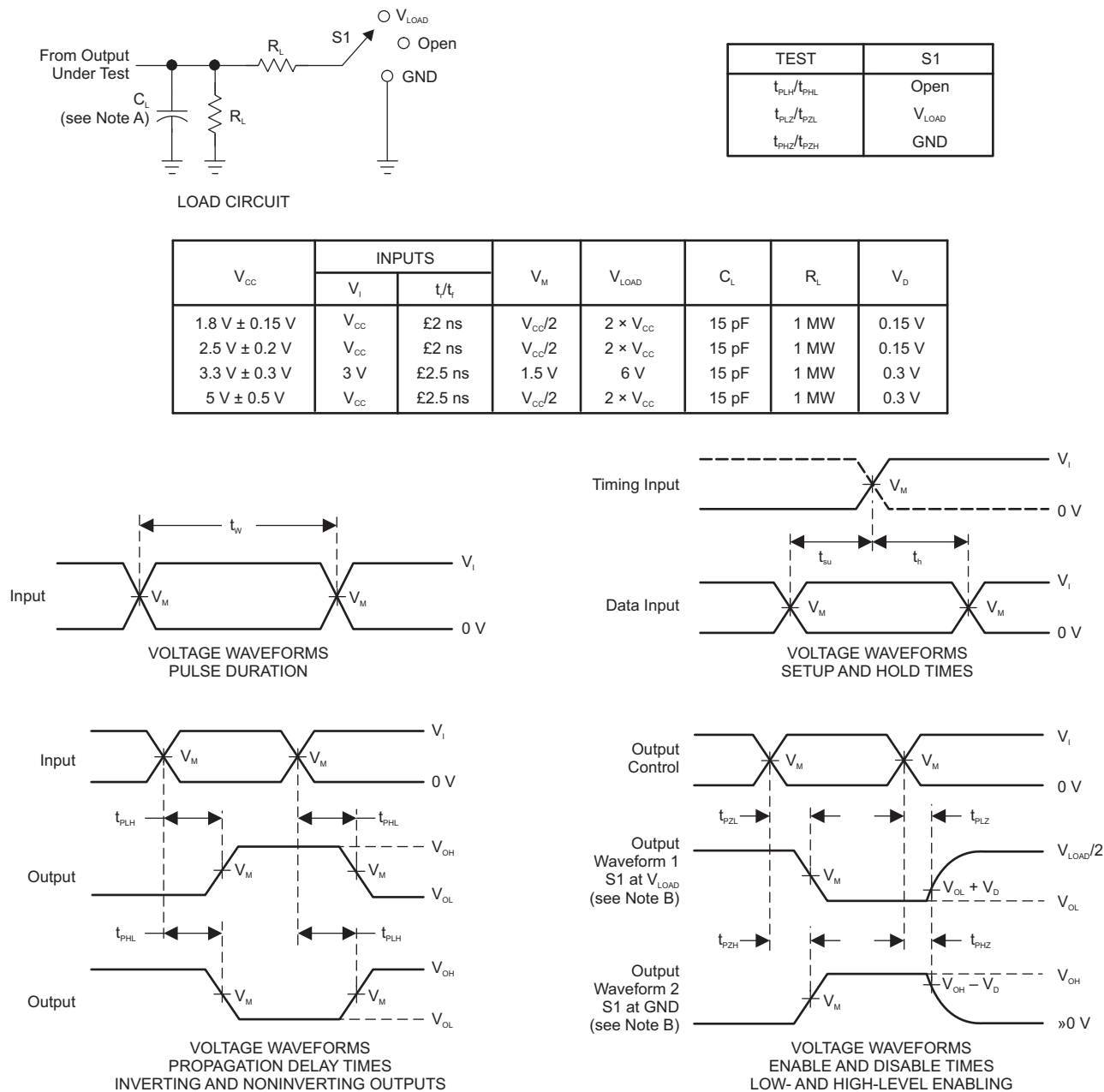
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	24	pF
			$V_{CC} = 2.5\text{ V}$	24	
			$V_{CC} = 3.3\text{ V}$	25	
			$V_{CC} = 5\text{ V}$	27	

6.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0 V to 6.5 V.



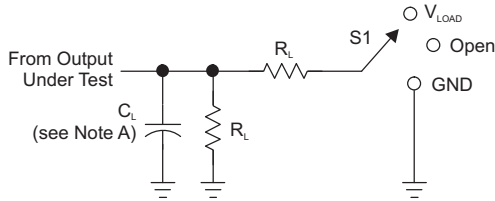
7 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

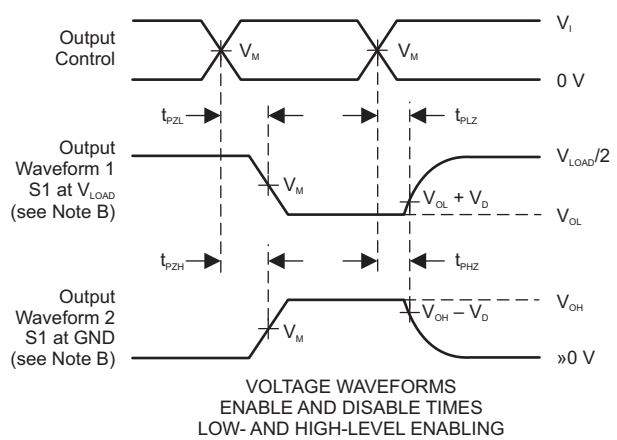
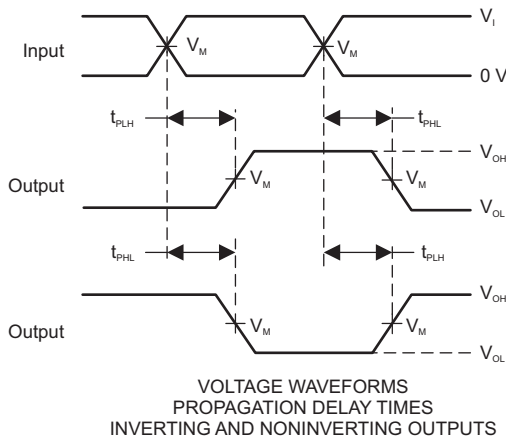
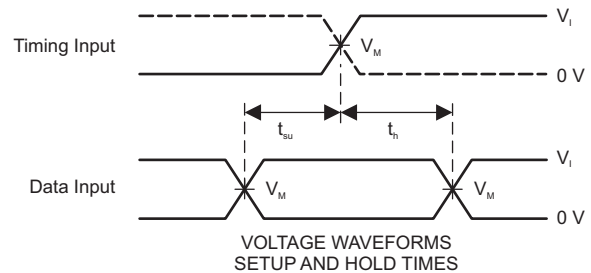
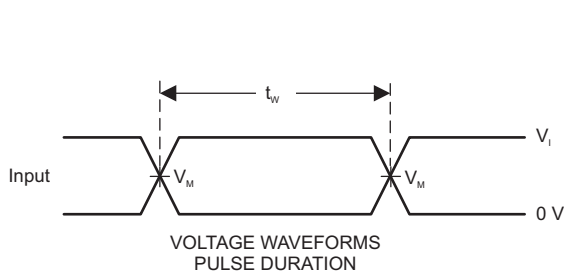
Parameter Measurement Information (continued)



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t/t_i					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	£2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	£2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 W	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	£2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 W	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, $Z_o = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

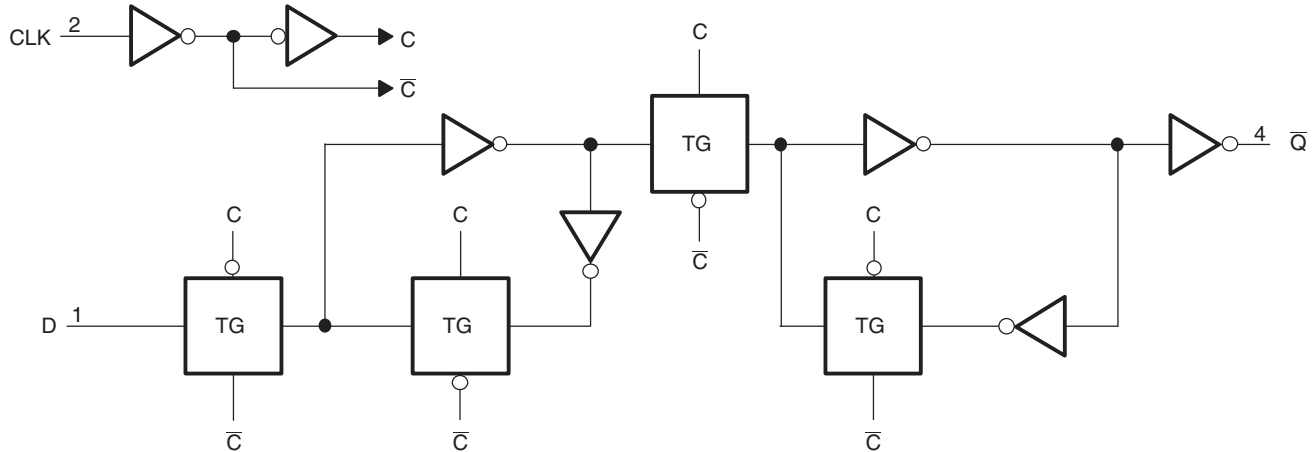
Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G80-Q1 is a single positive-edge-trigger D-type flip-flop and is AEC-Q100 qualified for automotive applications. Data at the input (D) is transferred to the output (\bar{Q}) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

8.2 Functional Block Diagram



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Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Recommended Operating Conditions](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Recommended Operating Conditions](#) to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

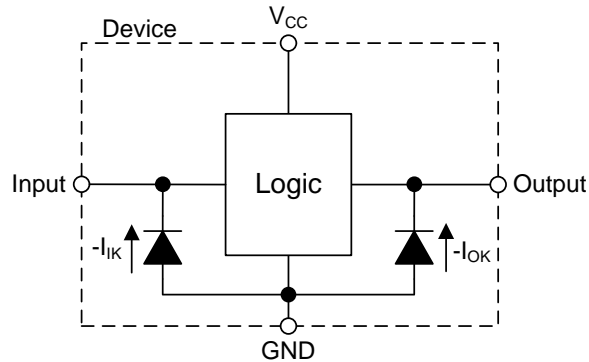


Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#).

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74LVC1G80-Q1.

Table 1. Function Table

INPUTS		OUTPUT Q
CLK	D	
↑	H	L
↑	L	H
L	X	Q_0

9 Application and Implementation

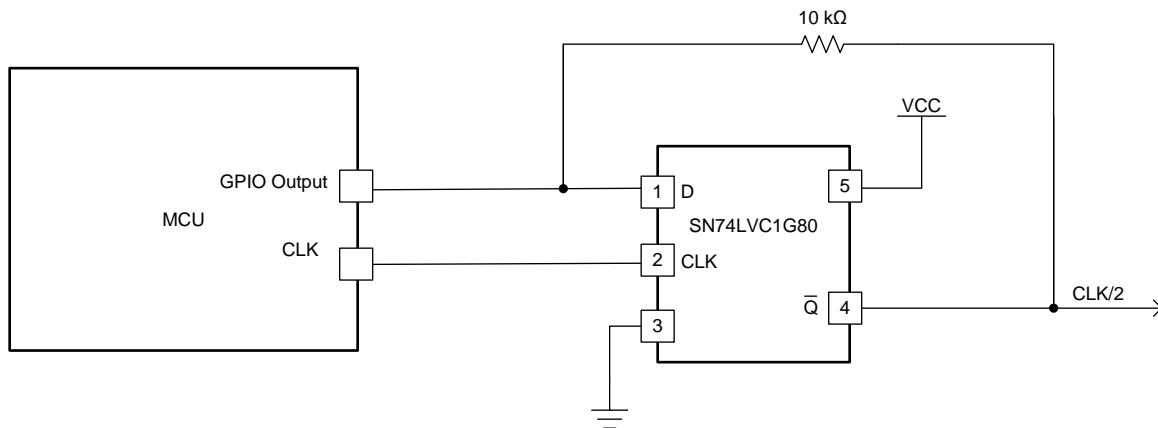
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A useful application for the SN74LVC1G80-Q1 is using it as a frequency divider. By feeding back the output (\overline{Q}) to the input (D), the output will toggle on every rising edge of the clock waveform. The output goes HIGH once every two clock cycles so essentially the frequency of the clock signal is divided by a factor of two. The SN74LVC1G80-Q1 does not have preset or clear functions so the initial state of the output is unknown. This application implements the use of a microcontroller GPIO pin to initially set the input HIGH, so the output LOW. Initialization is not needed, but should be kept in mind. Post initialization, the GPIO pin is set to a high impedance mode. Depending on the microcontroller, the GPIO pin could be set to an input and used to monitor the clock division.

9.2 Typical Application



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Figure 7. Clock Frequency Division

9.2.1 Design Requirements

For this application, a resistor needs to be placed on the feedback line in order for the initialization voltage from the microcontroller to overpower the signal coming from the output (\overline{Q}). Without it the state at the input would be challenged by the GPIO from the microcontroller and from the output of the SN74LVC1G80-Q1.

The SN74LVC1G80-Q1 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in *Recommended Operating Conditions*.
 - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
 - Input voltages are recommended to not go below 0 V and not exceed 5.5 V for any V_{CC} . See *Recommended Operating Conditions*.
2. Recommended output conditions:
 - Load currents should not exceed ± 50 mA. See *Absolute Maximum Ratings*.
 - Output voltages are recommended to not go below 0 V and not exceed the V_{CC} voltage. See *Recommended Operating Conditions*.
3. Feedback resistor:
 - A 10-k Ω resistor is chosen here to bias the input so the microcontroller GPIO output can initialize the input and output. The resistor value is important because a resistance too high, say at 1 M Ω , would cause too much of a voltage drop, causing the output to no longer be able to drive the input. On the other hand, a resistor too low, such as a 1 Ω , would not bias enough and might cause current to flow into the microcontroller, possibly damaging the device.

9.2.3 Application Curve

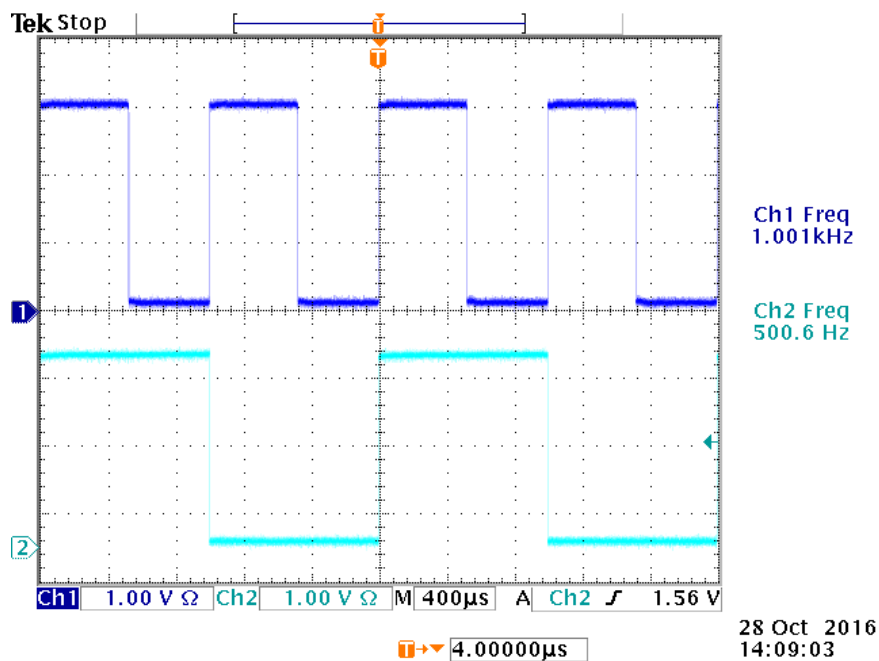


Figure 8. Frequency Division

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in [Recommended Operating Conditions](#). A 0.1- μF bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 9](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

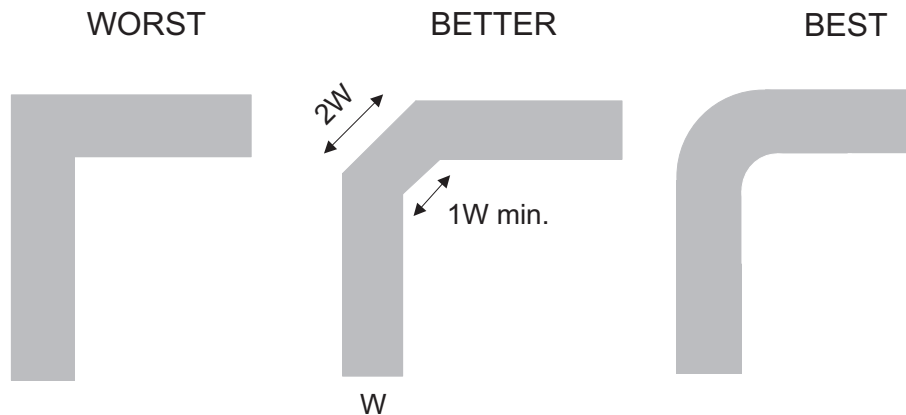


Figure 9. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G80QDCKRQ1	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125	17U	Samples
SN74LVC1G80QDCKTQ1	ACTIVE	SC70	DCK	5	250	TBD	Call TI	Call TI	-40 to 125	17U	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G80-Q1 :

- Catalog: [SN74LVC1G80](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0
SN74LVC1G80QDCKTQ1	SC70	DCK	5	250	340.0	340.0	38.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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