Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

1. Introduction

In case an application requires a higher current than the nominal value of one module, two MagI³C power modules can operate in parallel, doubling the output current. For this reason and the purpose of better understanding of the topic 'current sharing', a reference design board (order code: 178003) is introduced here.

The reference design consists of two MagI³C power modules (171021501) connected in parallel (with 2.5A rated current) with all complementary components needed to achieve current sharing. The two DC-DC converters can be controlled in two modes of operation, from the phase shift perspective, namely, interleaved mode (180° phase shift) and non-interleaved mode (0° phase shift).

Figure 1. MagI³C Current Sharing Reference Design

2. Specifications

Electrical Specifications

- Input Voltage Range 7V – 50V
- Output Voltage Range 2.5V – 15V
- Output Current 0A – 5A
- Maximum Output Power 75W
- Switching Frequency Adjustable (500kHz – 1MHz)

Features

- Symmetrical current-sharing tolerance ± 3% typ.
- Superimposed output voltage ripple < 4mV$_{PP}$
- Selectable synchronization Interleaved or non interleaved
- Discrete clock generator Integrated on the board
- Pads for an LC input filter Integrated on the board

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

3. Functional Diagram

Figure 2 shows the simplified block diagram of the two MagI³C Power Modules connected in parallel.

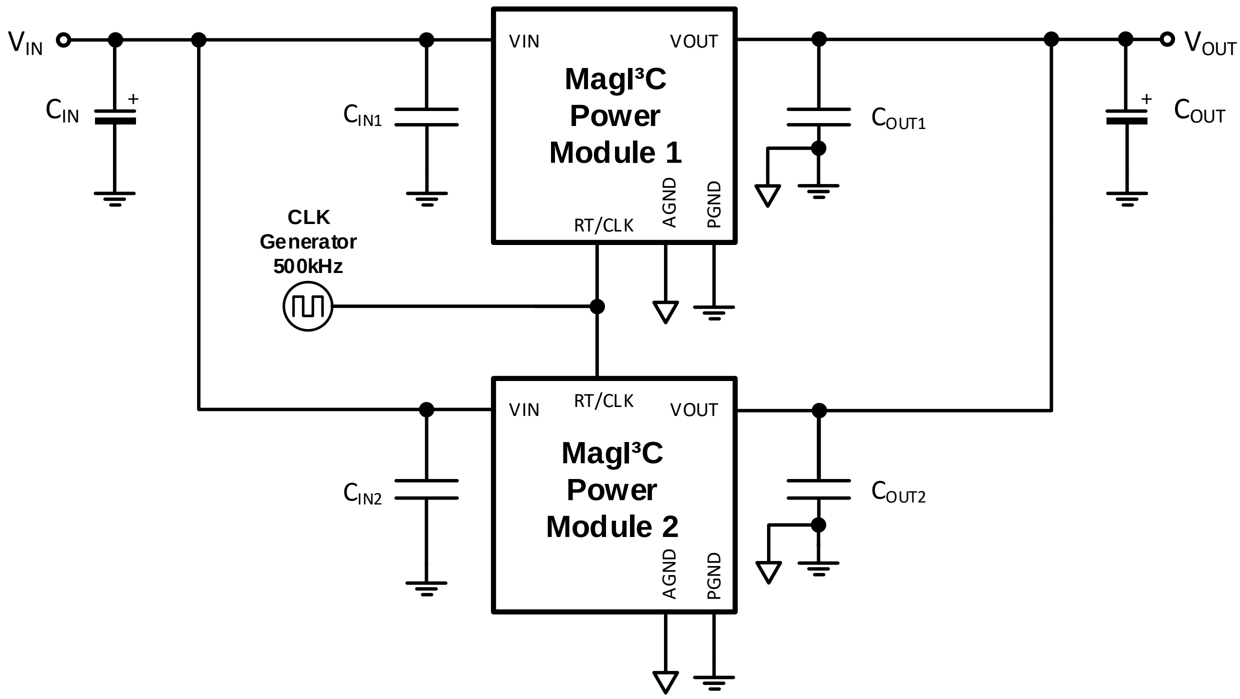


Figure 2. Functional Diagram

In addition, the input and output capacitors of the respective modules are shown. In order to operate the power modules in parallel, it is required to synchronize both devices to an external clock.

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

4. Reference Design Description

The following pictures show the current-sharing reference design board with its features:

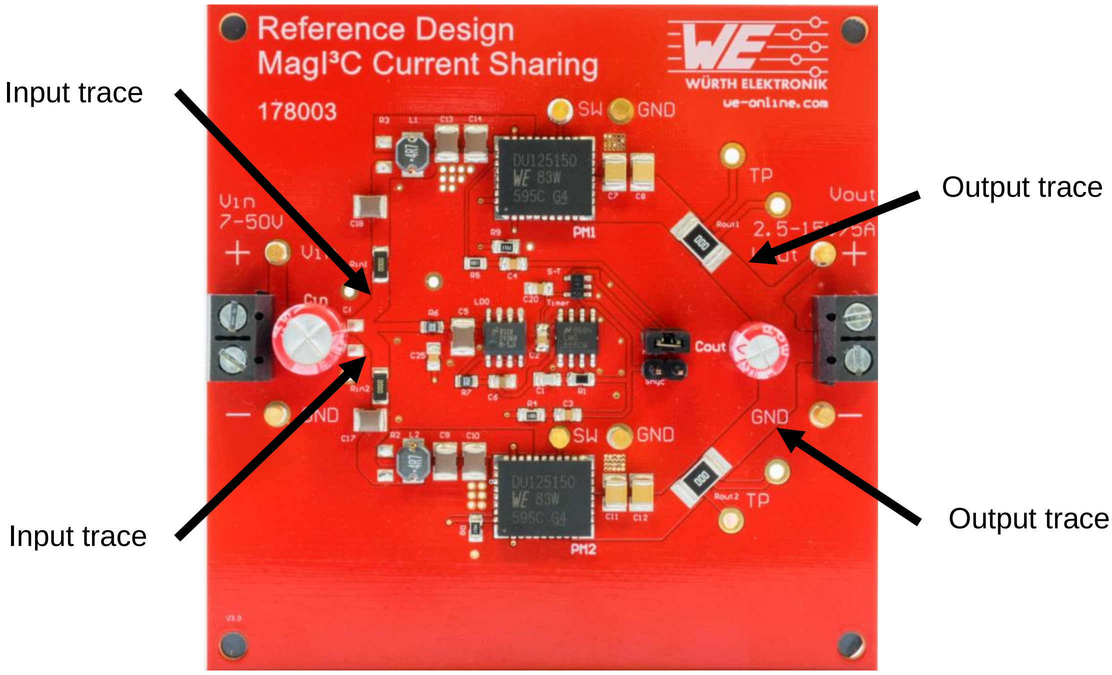


Figure 3. Current-Sharing Reference Design with two MagI³C Power Modules in Parallel

Reference Design Note

Magl^{3}C Power Modules

DNS003 Current-sharing with Magl³C Power Modules

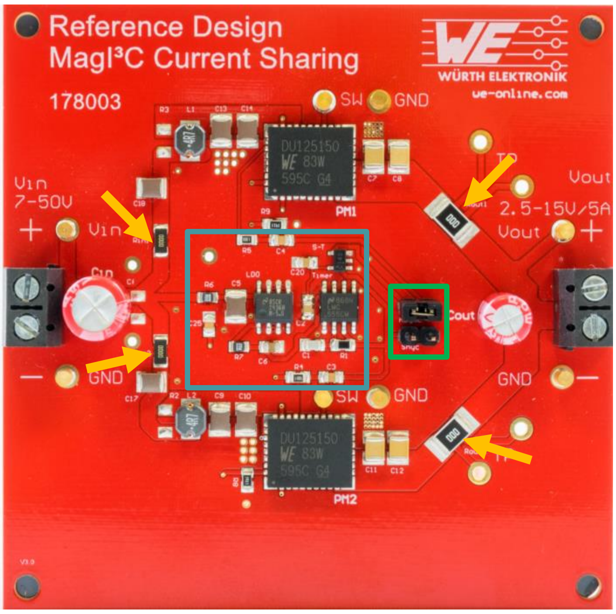


Figure 4. Features – clock, mode select, shunt

- Discrete clock generator
- Selection between inter-leaved (async) and non-interleaved (sync) mode
- Shunt resistors for measuring the input and output current (optional)

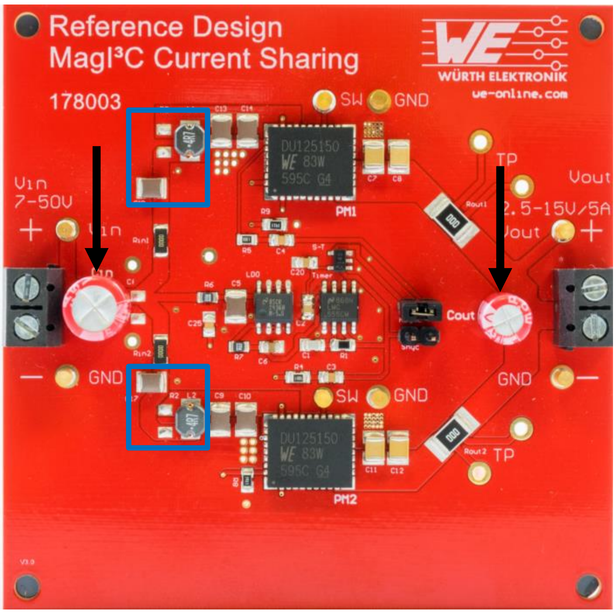


Figure 5. Feature – input filter, input / output capacitor

- Optional input filter implementation
- **Electrolytic capacitor at input:** To prevent undesired oscillations caused by series resonance of long supply wires with the ceramic input capacitors
- **Electrolytic capacitor at output:** improves transient performance

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

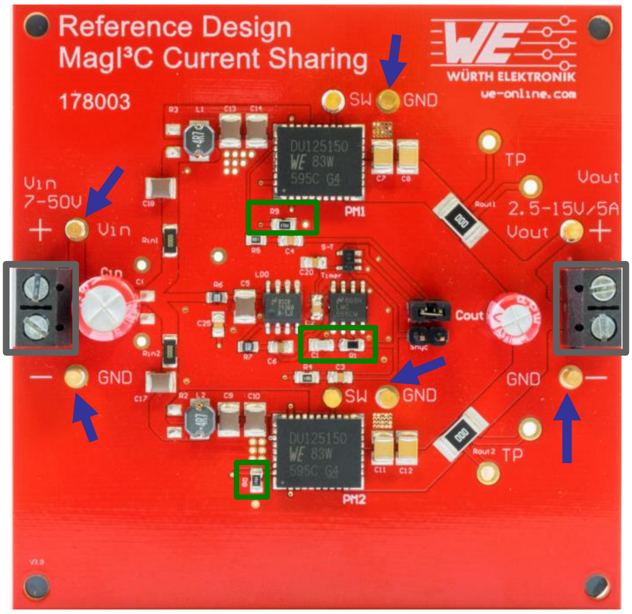


Figure 6. Features – terminals, test points, adjustment

- Solid screw terminals for V_{IN} and V_{OUT}
  - Allows for reliable connections and measurements
  - Standard wires can be used
- Robust test points
  - Measuring wires can be connected separately
  - Easy access to relevant points
- Easy adjustment of V_{OUT} and switching frequency

Values for different output voltages:

V_{OUT}	R_8 and R_9
2.5V	4.7kΩ
3.3V	3.2kΩ
5V	1.9kΩ
9V	976Ω
12V	714Ω
15V	563Ω

Values for different switching frequencies with C_1 = 1nF:

Switching frequency f_{CLK}	Capacitor value C_1	Resistor value R_1
500kHz	1nF	823Ω
600kHz	1nF	632Ω
700kHz	1nF	503Ω
800kHz	1nF	410Ω
900kHz	1nF	342Ω
1MHz	1nF	289Ω

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

5. Paralleling of MagI³C Power Modules

There are three common ways to connect DC/DC-Converters in parallel for the purposes of current sharing and redundancy:

- Brute-force current sharing (no additional circuitry)
- Forced current sharing (also known as active current sharing)
- Droop Regulation (output impedance increase to force the equal currents)

This reference design (two MagI³C Power Module 171021501 in parallel) uses the principle of the brute-force current sharing. This type of parallel connection has the advantage of scalability and is - compared to the other types - inexpensive. To realize this parallel circuitry several steps are necessary, which are explained in detail in the following chapter.

This reference design achieves the advantage of doubling the current capability, independent of the selected mode (non-interleaved / interleaved-mode). Another advantage of connecting in parallel is the improved heat distribution compared to the case of using a single module rated at the full load, i.e. the MagI³C Power Module 171050601 (nominal rated output current of 5A). While this module forms one heat spot on the board due to the power dissipation, the power losses of the parallel version with two modules split and thus heat is distributed. This creates two hot spots that are lower in temperature than a single module with the same output current.

In addition, the used modules of the parallel circuitry have a higher input voltage range ($50V_{max}$) than compared to the single module ($36V_{max}$), which results in a higher usability.

Furthermore paralleling the MagI³C Power Module 171021501, it is possible to select between two different modes: interleaved and non-interleaved, which will be explained now.

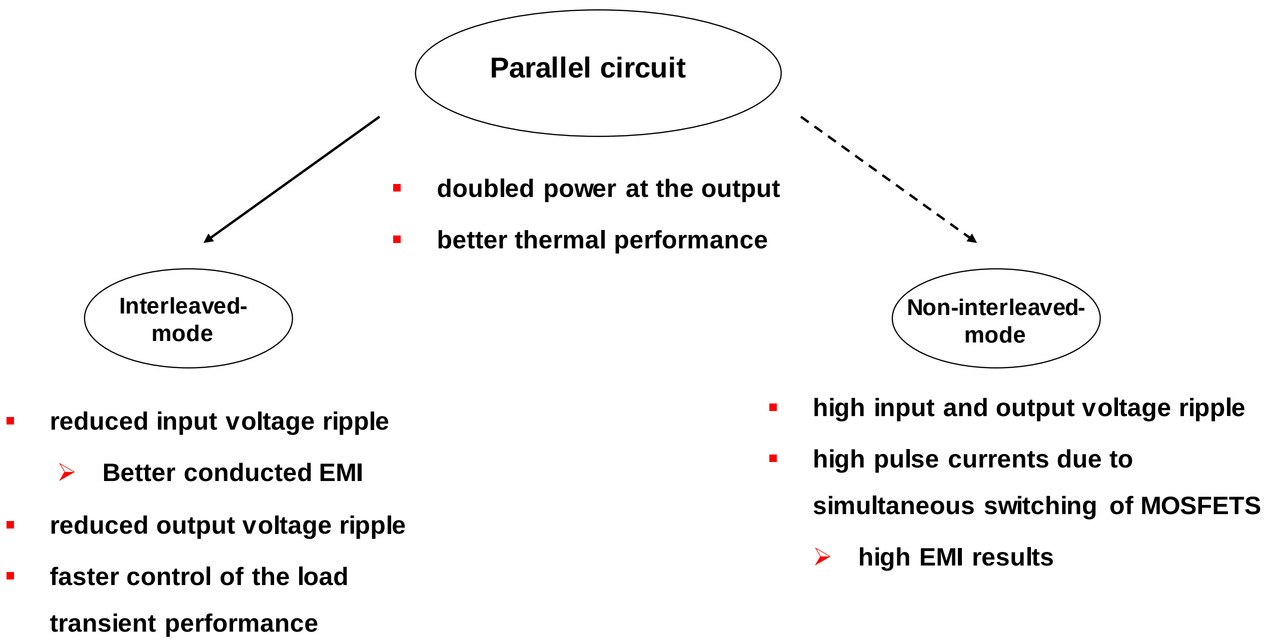


Figure 7. Overview of the Interleaved- and Non-Interleaved-Mode

5.1 Non-Interleaved Mode

The non-interleaved mode means that both PWM signals, which drive the modules, are in phase. This mode can be used if an application has wide limits regarding electromagnetic emission and/or output voltage ripple.
But if an application has strict limits the more complex mode must be used, which will be explained in the following.

5.2 Interleaved Mode

If the PWM signals are 180° out of phase, as showing in figure 8 the power modules work in interleaved mode. Running the converter in interleaved manner brings several benefits. From an electromagnetic interference reduction standpoint, the input voltage ripple is reduced because of the phase shift. Therefore, the requirements for an input filter are more relaxed. The 180° phase shifted output voltage ripple results in a smaller superimposed output voltage ripple on the shared output. This smaller ripple also results in smaller value of the required output capacitor.

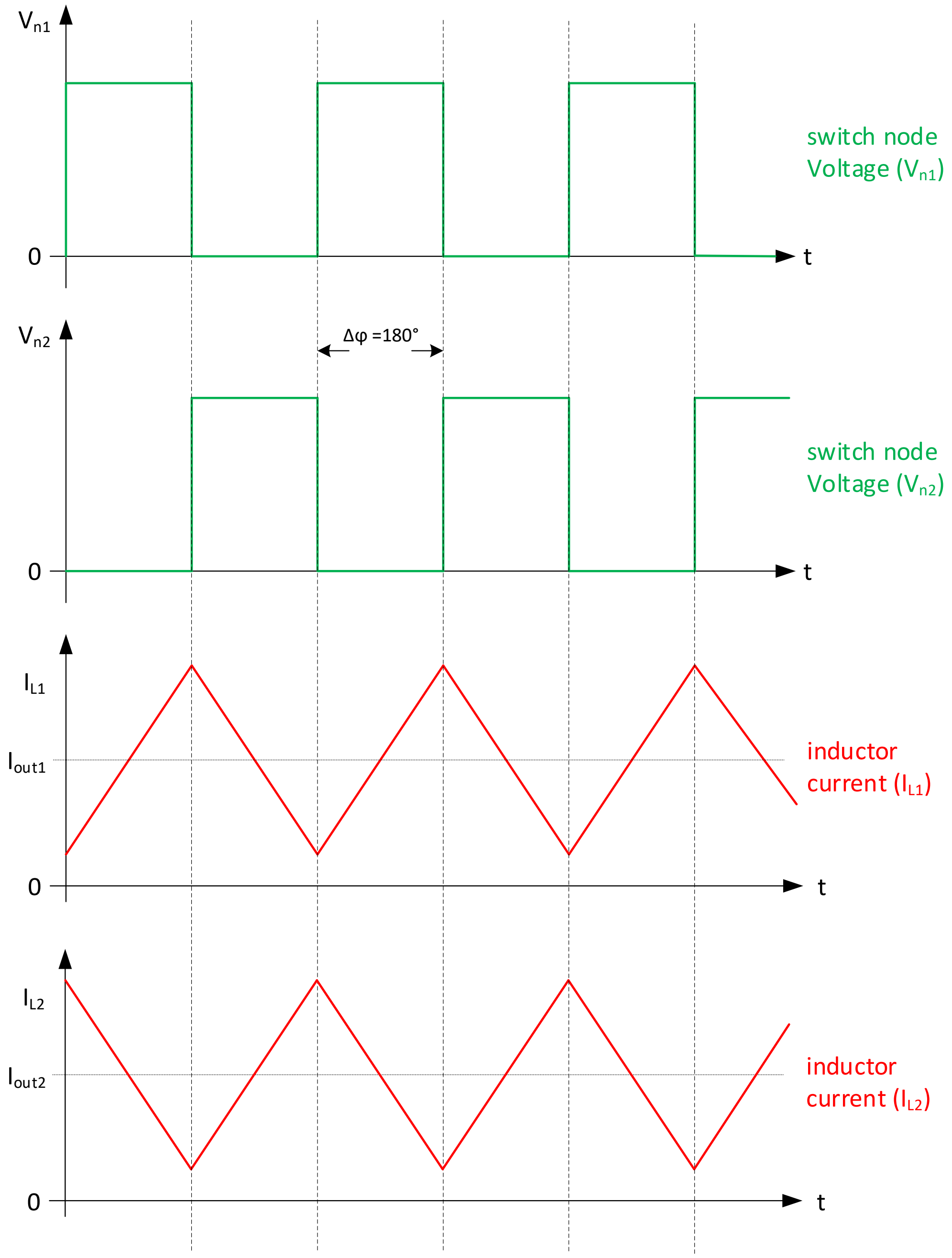


Figure 8. Signal Characteristics of Interleaved-Mode

The first two waveforms show the switching nodes phase-shifted by 180°. Below, the corresponding inductor currents are shown, also phase-shifted by 180°.

Additionally, current-sharing leads also to a faster control of the load transient, which can be described with figure 9 shown below. Therefore, statistically speaking, the possibility to meet the optimal recovery time (where the inductor current reaches its peak) is doubled since two peaks occur. This mode is therefore recommended due to the application limits concerning electromagnetic interference or output voltage ripple.

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

6. Circuit Description

6.1 Parallel circuitry

In the following circuit diagram, the basic connections for current-sharing (in green) and the connection of the clock generator (in red) are shown. The circuitry (number and size of input and output capacitors, synchronization configuration of R and C, etc.) is applied according to the "BILL OF MATERIAL" section. Layout rules (e.g. close placement of the input capacitor to VIN pin) also apply to each individual power module as recommended in their datasheet.

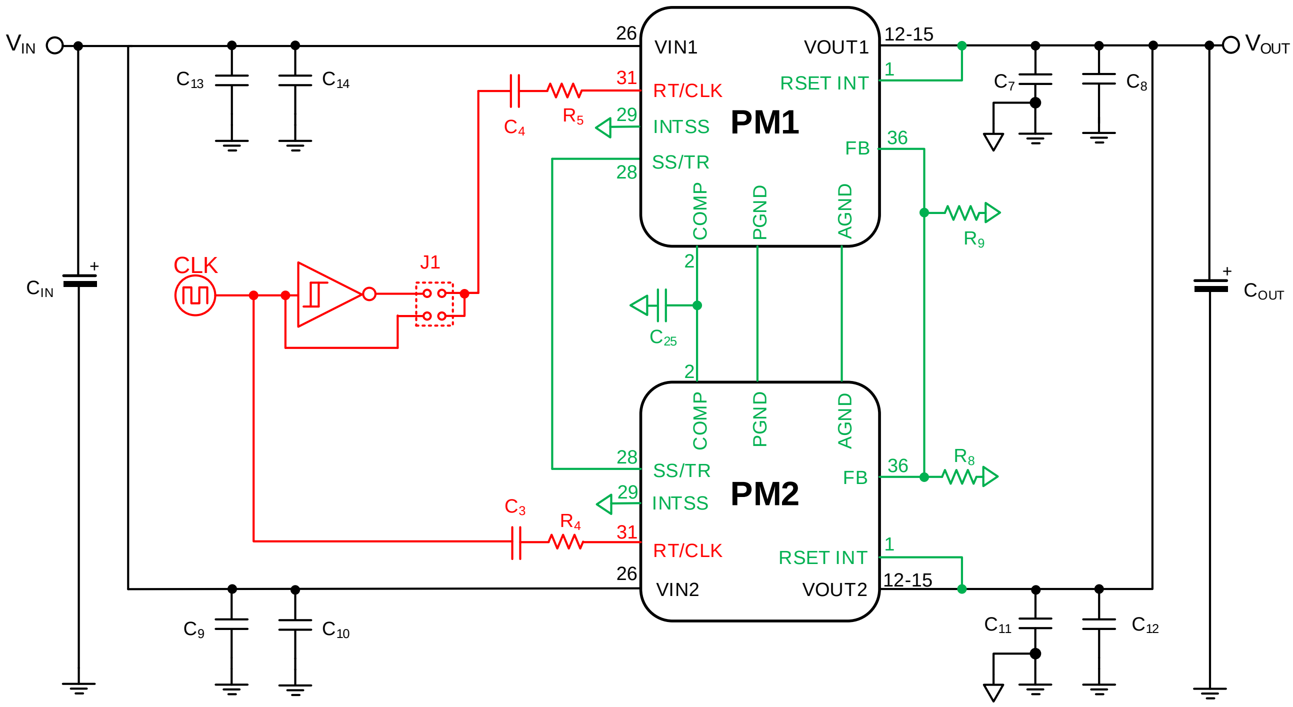


Figure 9. Circuit Diagram of the Current-Sharing Reference Design

Connections between the two MagI³C-Power-Modules:

- Connect VOUT1 and VOUT2 together to operate as a single output
- Both FB pins have to be connected to get the same output voltage on both modules: (RSET has to be selected according to the table in the "BILL OF MATERIAL")
- Both COMP pins have to be connected to force the same duty cycles in both modules (CSHARE is recommended with 100pF and used to filter noise)
- Both SS/TRK pins have to be connected to reach the output voltage at the same time (CSS has to be selected according to the datasheet table or formula or use the pin INTSS)
- The AGND and PGND pins have to be connected to refer to the same ground level
- Synchronization to a clock generator

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

6.2 Clock Generator

For paralleling two Power Modules (171021501) a clock generator with a rectangular signal is essential. Both RT/CLK-Pins have to be synchronized to this rectangular wave. Therefore the power modules can be - as already mentioned - driven in phase (non-interleaved mode) and 180° out-of-phase (interleaved-mode), which has different advantages considering technical issues.

The implemented clock generator for interleaving-mode is shown as follows:

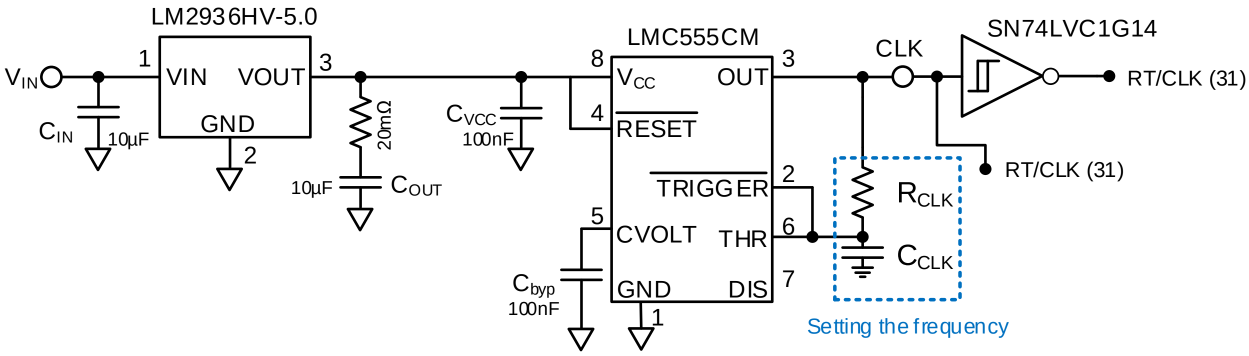


Figure 10: Clock Generator Circuit

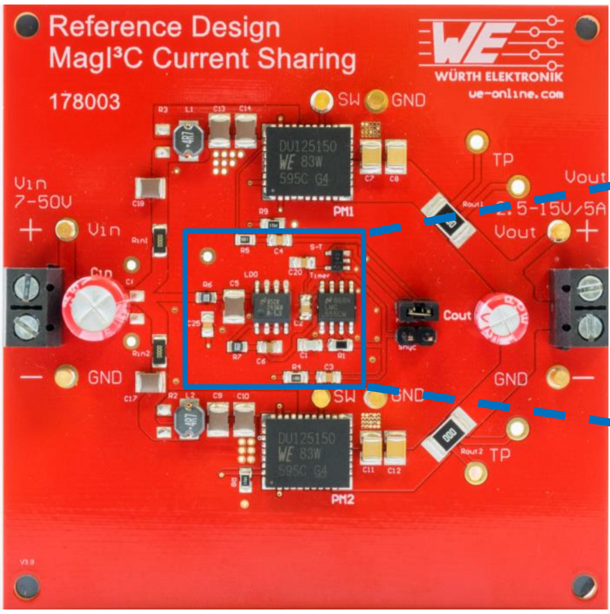
The clock is generated by the timer LMC555CM. It is configured as a 50% duty cycle oscillator. Due to its limited maximum supply voltage of 15V a linear regulator LM2936HV is used to support supply voltages up to 60V same as the MagI³C module. The phase shift of 180° is realized by the Schmitt-trigger-inverter SN74LVC1614. The particular signal with a 180° phase shift is routed to each Pin RT/CLK of the power module.

To reduce disturbances and have short traces, the discrete clock generator is included in the reference design. Therefore short traces and symmetrical distance to the MagI³C power modules are assured, see

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules



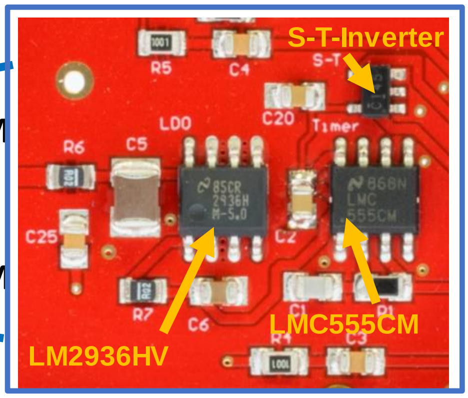


Figure 11: Clock Generator zoom view

Figure 12: Clock Generator on the Board

The 171021501 power module can operate with a user selectable frequency. For this reason R_1 and C_1 have to be chosen. The recommended capacitor C_1 value is 1nF. With this information, the resistor value of R_1 can be calculated.
For different frequencies, the following equation will be helpful to calculate the right resistor value:

$$R_1 \cdot C_1 = \frac{1}{1.4 \cdot f_{CLK} \cdot (1 + \frac{f_{CLK}}{680\ kHz})}$$

7. Filter Suggestions for Conducted EMI

The input filter shown in the schematic below is recommended to achieve conducted compliance according to EN55032 Class B. For radiated EMI the input filter is not necessary. It is useful to comply with the setup recommended in the standard. If two or more modules are connected to a single rail, the individual module's input has to be decoupled by an inductor in each input line in order to avoid mutual oscillations caused by the coupling and additional undesired antenna effect. To decouple these input lines and comply with the standard, two input LC filter designs are recommended:

7.1 LC Input Filter with a Common Filter Capacitor

First of all a LC input filter with one common filter capacitor Cf is recommended:

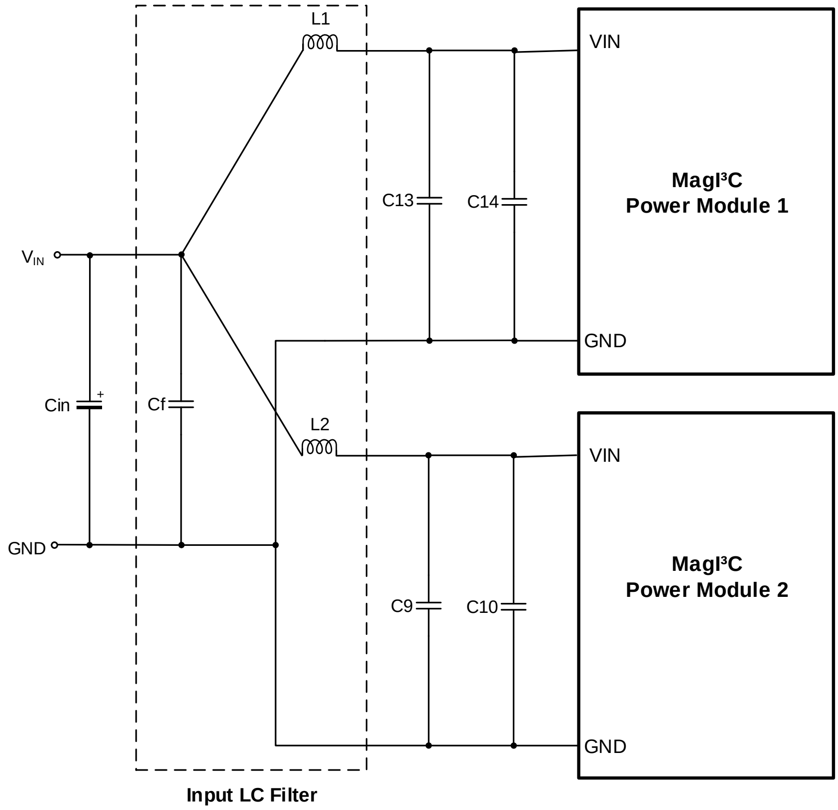


Figure 13: Simplified Schematic with a LC Input Filter (Common Cf)

Bill of Material of the Input LC Filter

Designator	Description	Order Code	Manufacturer
C99 (C_f)	Filter ceramic chip capacitor 4.7µF/50V X7R, 1210	885012209048	Würth Elektronik
L1, L2	Filter inductor, 4.7µH, PD2 family	744773047	Würth Elektronik

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

Interleaved Mode:

Test conditions	Value	Unit
Input voltage V_{IN}	24	V
Output voltage V_{OUT}	5	V
Switching frequency fSW	500	kHz
Output current IOUT	5	A
Filter capacitor Cf	4.7	µF
Filter inductor L1, L2	4.7	µH
Ambient temperature TAMB	22	°C

Conducted EMI Results measured on the reference design board:

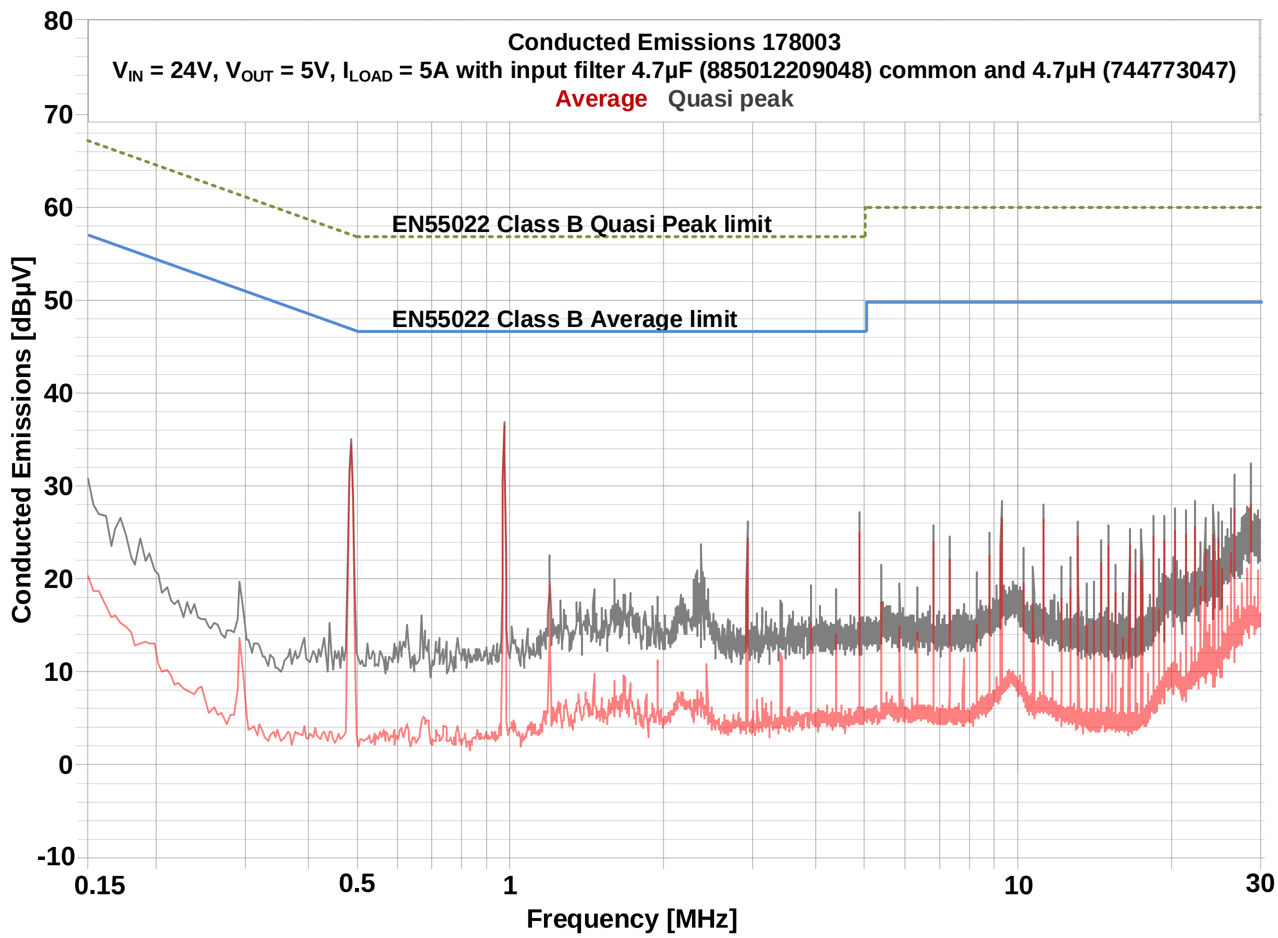


Figure 14: Conducted EMI

The used filter complies with the standard EN55022 Class B.

The reference design board allows also a splitting of the filter capacitor C_f, which is now shown below.

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

7.2 LC Input Filter with a Filter Capacitor in Each Input Line

A LC input filter with a separated filter capacitor C17, C18 in each input trace:

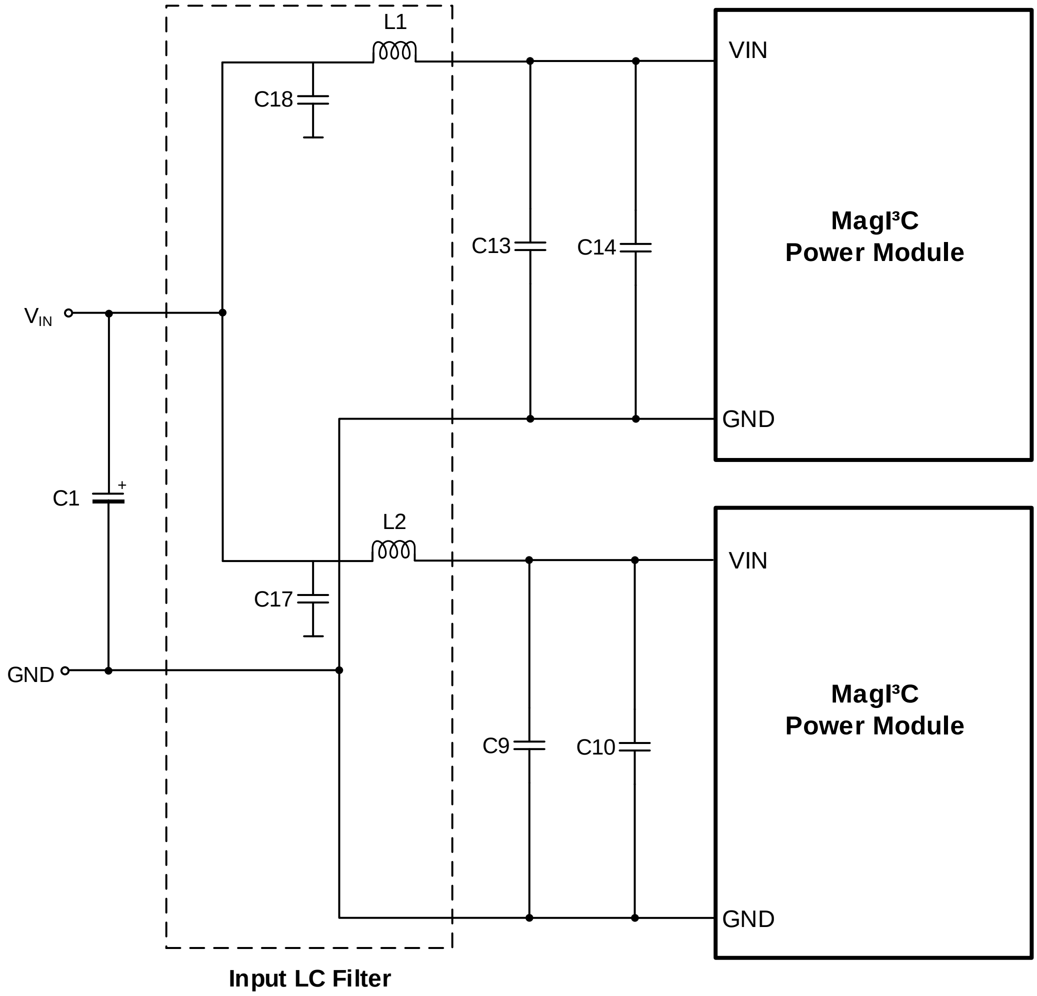


Figure 15: Simplified Schematic with a LC Input Filter (Separated Cf)

Bill of Material of the input LC Filter

Designator	Description	Order Code	Manufacturer
C17, C18	Filter ceramic chip capacitor 2.2µF/100V X7R, 1210	-	Various
L1, L2	Filter inductor, 4.7µH, PD2 family	744773047	Würth Elektronik

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

Interleaved Mode:

Test conditions	Value	Unit
Input voltage V_{IN}	24	V
Output voltage V_{OUT}	5	V
Switching frequency f_{SW}	500	kHz
Output current I_{OUT}	5	A
Filter capacitor C_{17}, C_{18}	**2.2**	**µF**
Filter inductor L_1, L_2	4.7	µH
Ambient temperature T_{AMB}	22	°C

Conducted EMI Results measured on the reference design board:

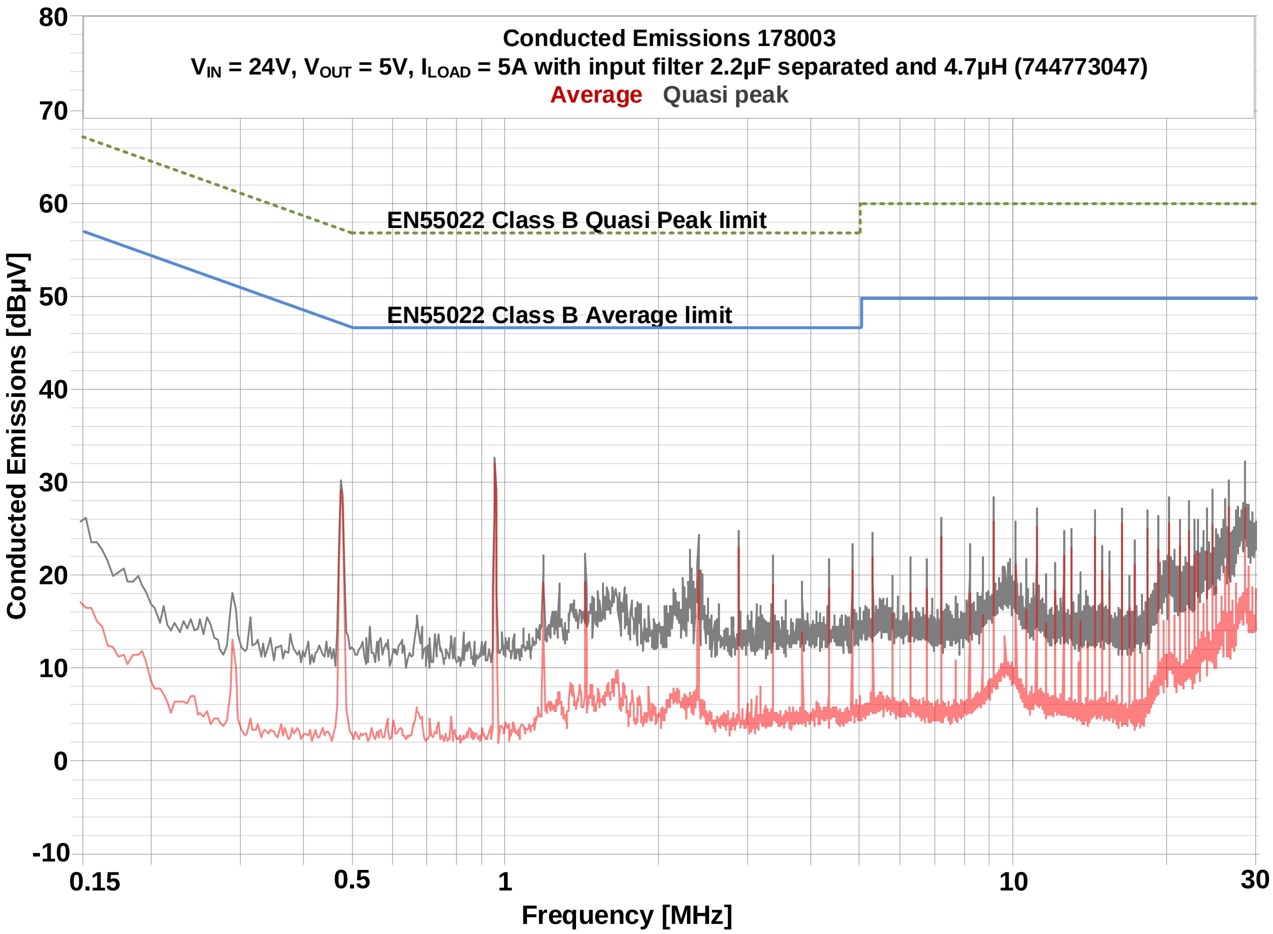


Figure 16: Conducted EMI

Dividing the filter capacitor C_f leads to a minimal (approximately 6-7dBµV) improvement of the EMC. With these results the following final recommendation can be given: With two separated filter capacitors, there is more safety (higher filtering effect) with the layout, if the input lines are not exactly symmetrical because of e.g. space reasons.

Reference Design Note

MagI³C Power Modules
DNS003 Current-sharing with MagI³C Power Modules

8. Thermal Performance and Layout Section

When creating the layout, special care must be taken for the input and output traces. The critical points for a symmetrical current-sharing are the input and output traces. The length and width and therefore the impedance of the input and output trace have to be identical. Additionally the section LAYOUT in the datasheet of the MagI³C Power Module (171021501) is recommended.
The PCB consists of four layer (copper thickness 70µm) which are connected through vias under each power module.

Test conditions	Value	Unit
Input voltage VIN	24	V
Output voltage VOUT	5	V
Switching frequency fSW	500	kHz
Output current IOUT	5	A
Power losses	10.55	W
Ambient temperature TAMB	22	°C

Figure 15 below shows the top side of the current-sharing reference design.

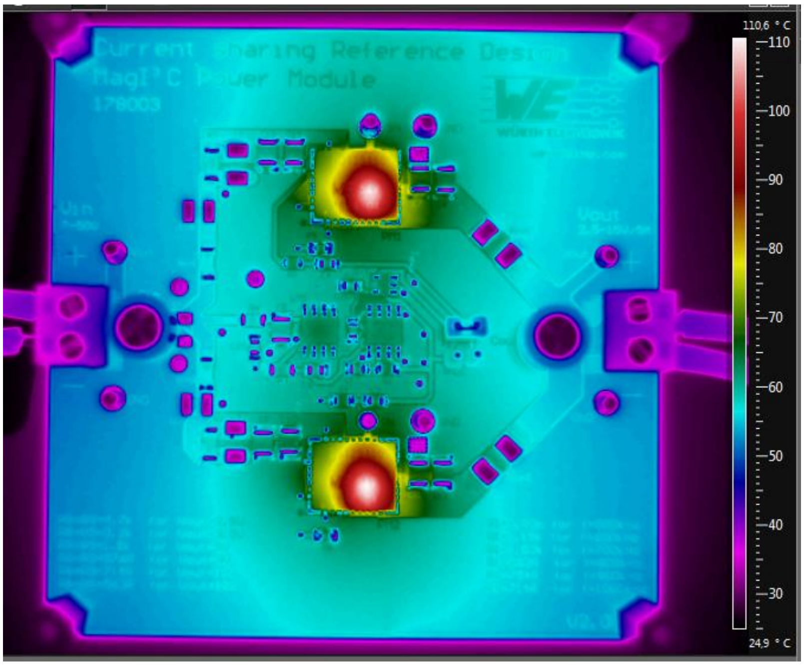


Figure 17: Thermo picture with IR Camera

CONCLUSION

- Both power modules are at the same temperature level
- Symmetrical distribution of the heat on the PCB
- Optimal utilization of PCB area to ensure heat spreading

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

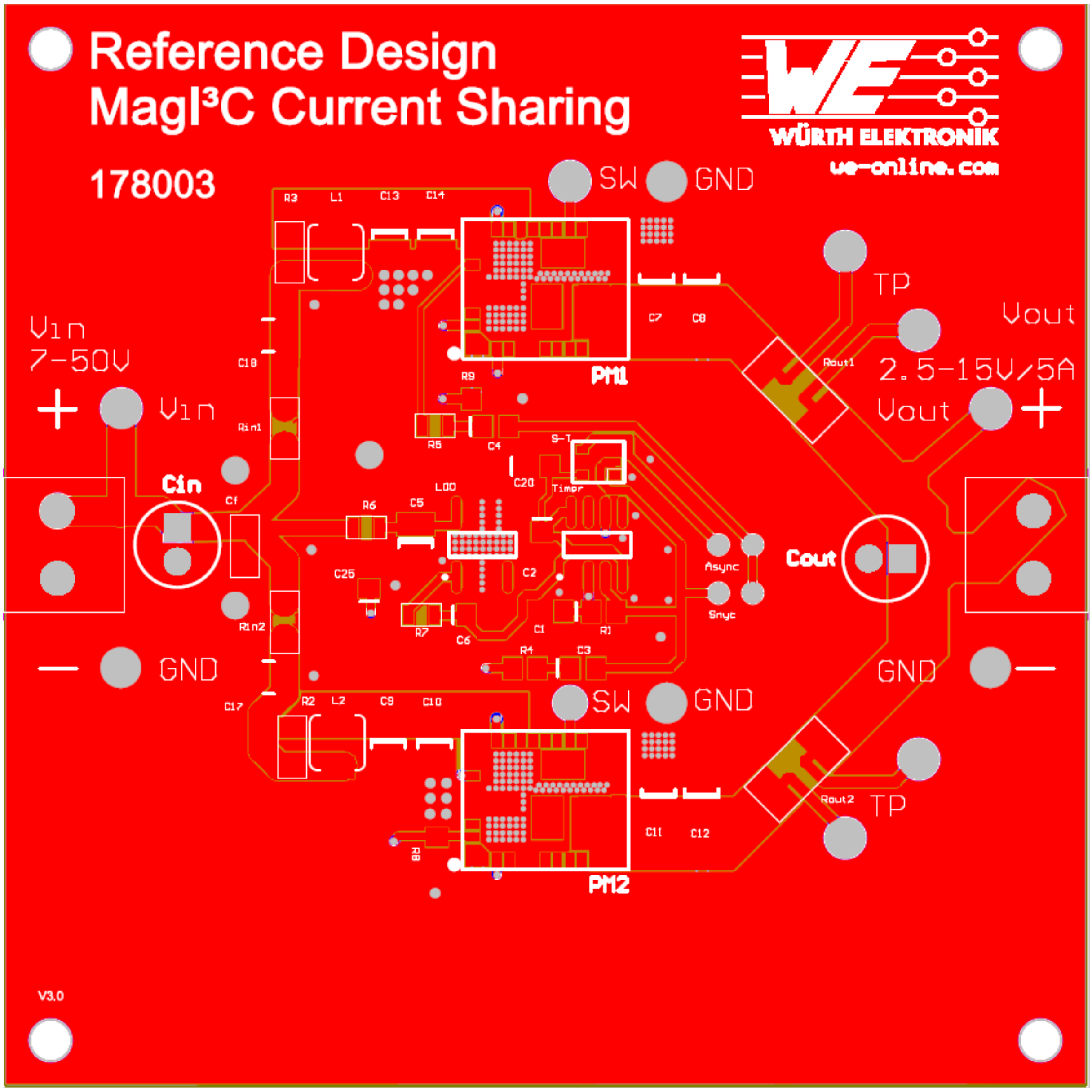


Figure 18: Top View

CONCLUSION

- Symmetrical routing of power paths
- Clock generator placed in center
- Shunt resistors for current measurements
- Input filter option in each path

The next two chapters show the “SCHEMATIC” and the “BILL OF MATERIAL” of the reference design.

Markus Roppel - February 2019

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

9. Schematic

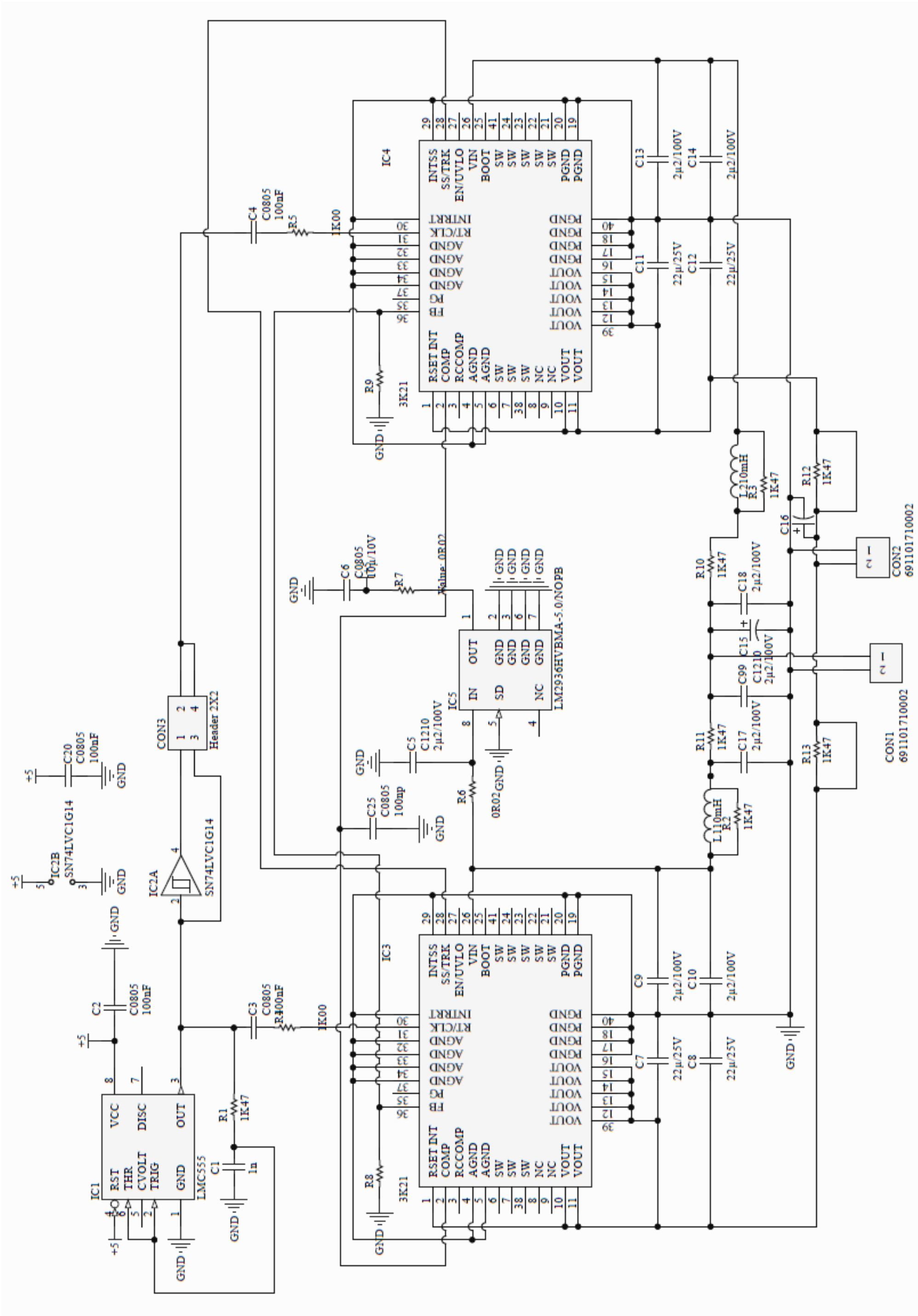


Figure 19: Schematic of the Reference Design

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

10. Assembly Drawing

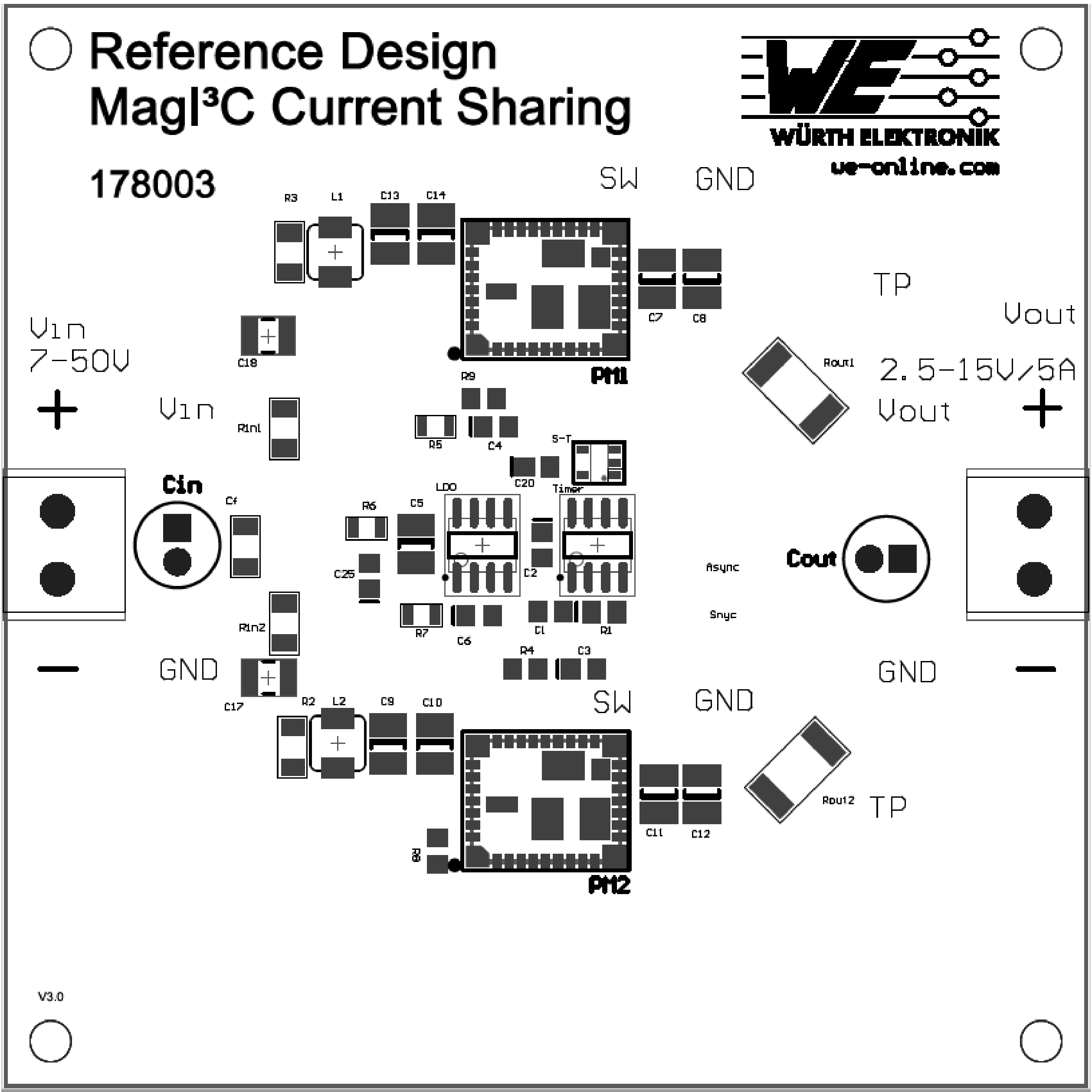


Figure 20: Assembly Drawing

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

11. Bill of Material

Designator	Description	Quantity	Order Code	Manufacturer
IC3, IC4	MagI³C Power Module	2	171021501	Würth Elektronik
R2, R3	SMD bridge 0Ω resistance	2	-	Various
R8, R9	4.7kΩ for V_{OUT} = 2,5V	2	-	Various
	3.2kΩ for V_{OUT} = 3,3V	2	-	Various
	1.9kΩ for V_{OUT} = 5V	2	-	Various
	976Ω for V_{OUT} = 9V	2	-	Various
	714Ω for V_{OUT} = 12V	2	-	Various
	563Ω for V_{OUT} = 15V	2	-	Various
C9, C10, C13, C14	Ceramic chip capacitor 2.2µF/100V, X7R, 1210	4	-	Various
C7, C8, C11, C12	Ceramic chip capacitor 22µF/25V, X7R, 1210	4	-	Various
C15 (Cin), C16 (Cout)	Aluminium electrolytic capacitor 27µF/100V	2	860040874001	Würth Elektronik
R10 (Rin1), R11 (Rin2)	Shunt resistor 1mΩ	2	-	Various
R12 (Rout1), R13 (Rout2)	Shunt resistor 1mΩ	2	-	Various
C25	Ceramic chip capacitor 100pF/10V, X7R, 0805	1	885012207004	Würth Elektronik

Clock generator components:

Designator	Description	Quantity	Order Code	Manufacturer
IC1	Timer	1	LMC555CMX/NOPBCT-ND	Texas Instruments
IC2	Schmitt-Trigger Inverter	1	SN74LVC1G14DBVR	Texas Instruments
IC5	Linear Voltage Regulator	1	LM2936HVMAX-5.0/NOPBCT-ND	Texas Instruments
C1	Ceramic chip capacitor 1nF/50V, X7R, 0805	1	885012207086	Würth Elektronik
R1	823Ω for f = 500kHz	1	-	Various
	632Ω for f = 600kHz	1	-	Various
	503Ω for f = 700kHz	1	-	Various
	410Ω for f = 800kHz	1	-	Various
	342Ω for f = 900kHz	1	-	Various
	289Ω for f = 1000kHz	1	-	Various
C2, C20	Ceramic chip capacitor 100nF/50V, X7R, 0805	2	885012207098	Würth Elektronik
C3, C4	Ceramic chip capacitor 470pF/10V, C0G, 0805	2	885012007007	Würth Elektronik
R4, R5	1kΩ	2	-	Various
C5	Ceramic chip capacitor 2.2µF/100V, X7R, 1210	1	-	Various
C6	Ceramic chip capacitor 10µF/10V, X7R, 0805	1	885012207026	Würth Elektronik
R6, R7	Shunt resistor 20mΩ	2	-	Various

Reference Design Note

MagI³C Power Modules

DNS003 Current-sharing with MagI³C Power Modules

USEFUL LINKS

Application Notes / Reference Design Notes
https://www.we-online.com/app-notes

REDEXPERT Design Tool
https://www.we-online.com/redexpert

Toolbox
https://www.we-online.com/toolbox

MagI³C Product Catalog
https://katalog.we-online.com/en/pm

CONTACT INFORMATION

Technical Support
powermodules@we-online.com

Würth Elektronik eiSos GmbH & CO. KG
Max-Eyth-Str. 1, 74638 Waldenburg
Germany

Tel.: +49 7942 945 0
we-online.com