

SN74HCS126-Q1 Automotive Quadruple Buffer with 3-State Outputs and Schmitt-Trigger Inputs

1 Features

- AEC-Q100 Qualified for automotive applications:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
 - Typical I_{CC} of 100 nA
 - Typical input leakage current of ± 100 nA
- ± 7.8 -mA output drive at 5 V

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Debounce a switch
- Eliminate slow or noisy input signals

3 Description

This device contains four independent buffer with 3-state outputs and Schmitt-trigger inputs. Each gate performs the Boolean function $Y = A$ in positive logic. The outputs can be put into a Hi-Z state by applying a Low on the OE pin

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS126QPWRQ1	TSSOP (14)	5.00 mm × 4.40 mm
SN74HCS126QDRQ1	SOIC (14)	8.70 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Benefits of Schmitt-trigger Inputs

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			



Table of Contents

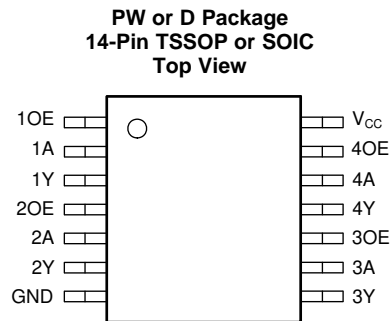
1 Features	1	8.3 Feature Description	7
2 Applications	1	8.4 Device Functional Modes	8
3 Description	1	9 Application and Implementation	9
4 Revision History	2	9.1 Application Information	9
5 Pin Configuration and Functions	3	9.2 Typical Application	9
6 Specifications	3	10 Power Supply Recommendations	11
6.1 Absolute Maximum Ratings	3	11 Layout	11
6.2 ESD Ratings	4	11.1 Layout Guidelines	11
6.3 Recommended Operating Conditions	4	11.2 Layout Example	11
6.4 Thermal Information	4	12 Device and Documentation Support	12
6.5 Electrical Characteristics	4	12.1 Documentation Support	12
6.6 Switching Characteristics	5	12.2 Related Links	12
6.7 Operating Characteristics	5	12.3 Community Resources	12
6.8 Typical Characteristics	5	12.4 Trademarks	12
7 Parameter Measurement Information	6	12.5 Electrostatic Discharge Caution	12
8 Detailed Description	7	12.6 Glossary	12
8.1 Overview	7	13 Mechanical, Packaging, and Orderable Information	12
8.2 Functional Block Diagram	7		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2020	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1OE	1	Input	Channel 1, Output Enable, Active High
1A	2	Input	Channel 1, Input A
1Y	3	Output	Channel 1, Output Y
2OE	4	Input	Channel 2, Output Enable, Active High
2A	5	Input	Channel 2, Input A
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3OE	10	Input	Channel 3, Output Enable, Active High
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4OE	13	Input	Channel 4, Output Enable, Active High
V _{CC}	14	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	−0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}		±20 mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}		±20 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35 mA
I _{CC}	Continuous current through V _{CC} or GND			±70 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS126-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.5	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.5	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.1	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{T+}	Positive switching threshold		2 V	0.7		1.5	V
			4.5 V	1.7		3.15	
			6 V	2.1		4.2	
V_{T-}	Negative switching threshold		2 V	0.3		1	V
			4.5 V	0.9		2.2	
			6 V	1.2		3	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		2 V	0.2		1	V
			4.5 V	0.4		1.4	
			6 V	0.6		1.6	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu A$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$	V
			$I_{OH} = -6 \text{ mA}$	4.5 V	4	4.3	
			$I_{OH} = -7.8 \text{ mA}$	6 V	5.4	5.75	
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu A$	2 V to 6 V	0.002	0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5 V	0.18	0.3	
			$I_{OL} = 7.8 \text{ mA}$	6 V	0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0	6 V		±100	±1000	μA

(1) $T_A = 25^\circ\text{C}$

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{OZ}	Off-state (high-impedance state) output current	V _O = V _{CC} or 0	6 V		0.01	2	μA
I _{CC}	Supply current	V _I = V _{CC} or 0, I _O = 0	6 V		0.1	2	μA
C _i	Input capacitance		2 V to 6 V			5	pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{pd}	Propagation delay	A	Y	2 V		15	50	ns
				4.5 V		8	30	
				6 V		7	26	
t _{en}	Enable time	OE	Y	2 V		18	36	ns
				4.5 V		9	14	
				6 V		7	12	
t _{dis}	Disable time	OE	Y	2 V		15	27	ns
				4.5 V		10	17	
				6 V		9	14	
t _t	Transition-time		Any	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

(1) T_A = 25°C

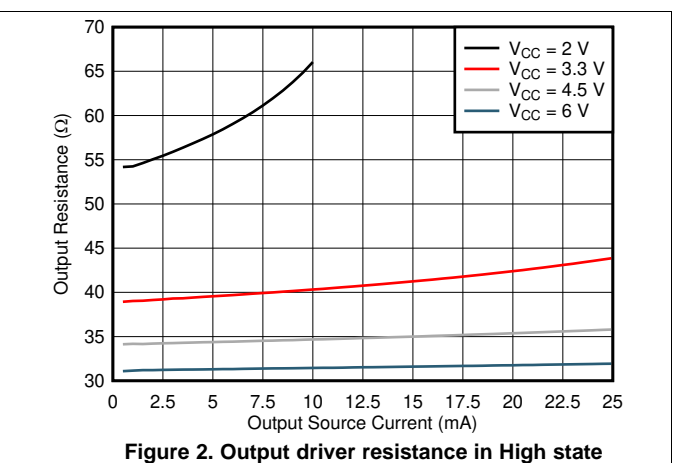
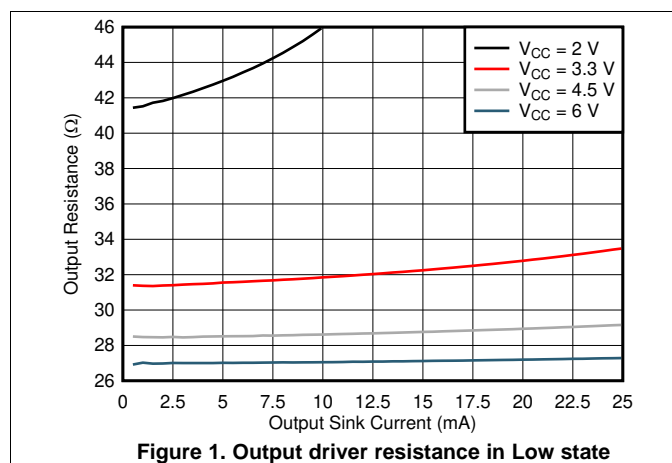
6.7 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
C _{pd}	Power dissipation capacitance per gate	No load		10		pF

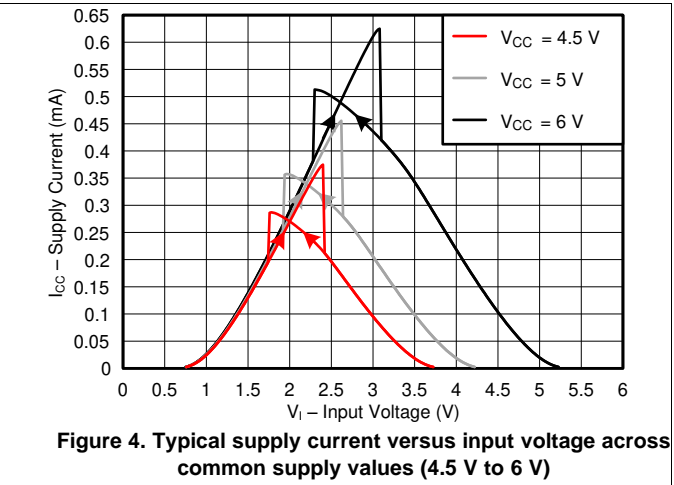
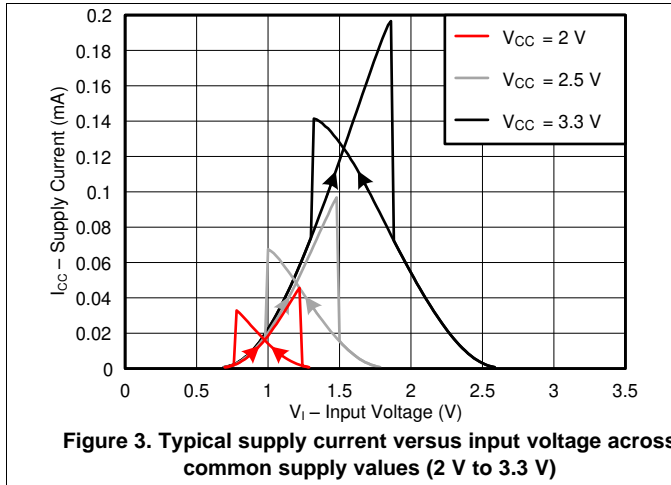
(1) T_A = 25°C

6.8 Typical Characteristics

T_A = 25°C


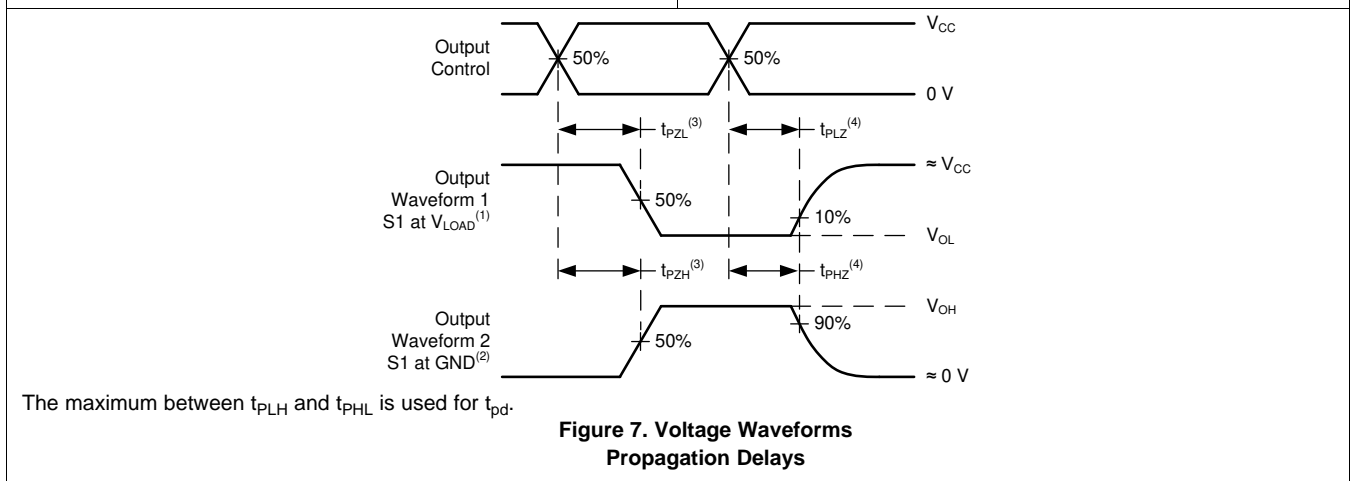
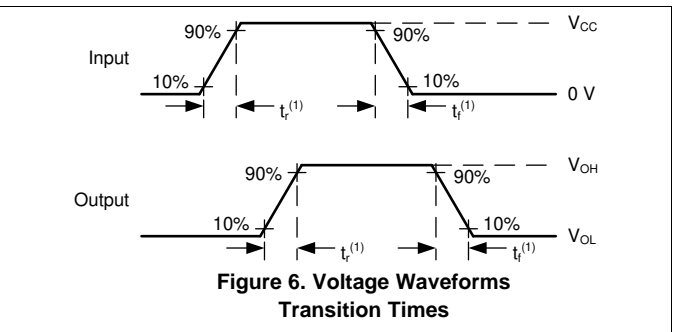
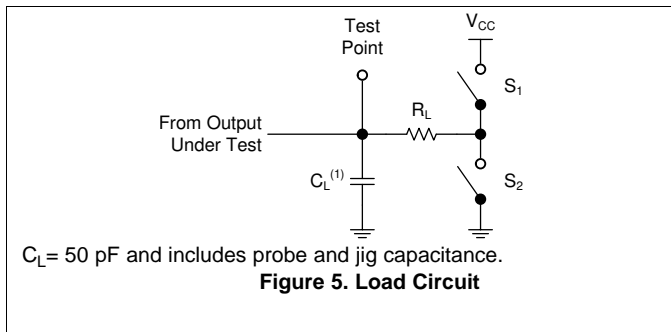
Typical Characteristics (continued)

T_A = 25°C



7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_f < 2.5 ns.
- The outputs are measured one at a time, with one input transition per measurement.

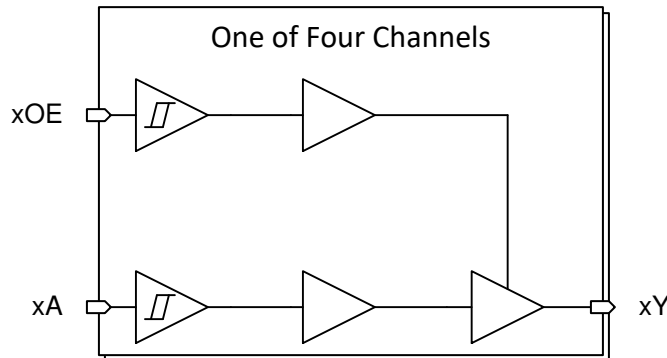


8 Detailed Description

8.1 Overview

This device contains four independent buffer with 3-state outputs and Schmitt-trigger inputs. Each gate performs the Boolean function $Y = A$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

The SN74HCS126-Q1 can drive a load with a total capacitance less than or equal to the maximum load listed in the [Switching Characteristics](#) connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the [Absolute Maximum Ratings](#).

3-State outputs can be placed into a high-impedance state. In this state, the output will neither source nor sink current, and leakage current is defined by the I_{OZ} specification in the [Electrical Characteristics](#). A pull-up or pull-down resistor can be used to ensure that the output remains HIGH or LOW, respectively, during the high-impedance state.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

Feature Description (continued)

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Figure 8](#).

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

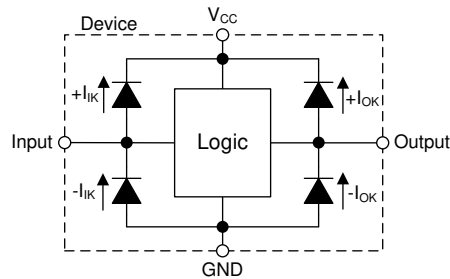


Figure 8. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT
OE	A	Y
L	X	Z
H	L	L
H	H	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In this application, a buffer with a 3-state output is used to disable a data signal as shown in [Figure 9](#). The remaining three buffers can be used for signal conditioning in other places in the system, or the inputs can be grounded and the channels left unused.

9.2 Typical Application

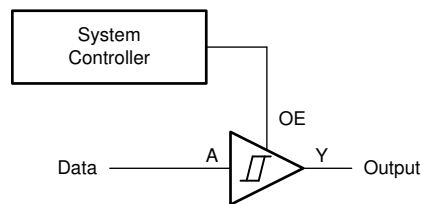


Figure 9. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS126-Q1 plus the maximum supply current, I_{CC} , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [Absolute Maximum Ratings](#).

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\text{max})$ listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t(\text{min})}$ to be considered a logic LOW, and $V_{t(\text{max})}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the [Absolute Maximum Ratings](#).

Typical Application (continued)

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS126-Q1, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS126-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_T(\text{min})$ in the [Electrical Characteristics](#). This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the [Typical Characteristics](#).

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics](#).

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to [Feature Description](#) for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [Layout](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS126-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(\text{max})}) \Omega$. This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

9.2.3 Application Curves

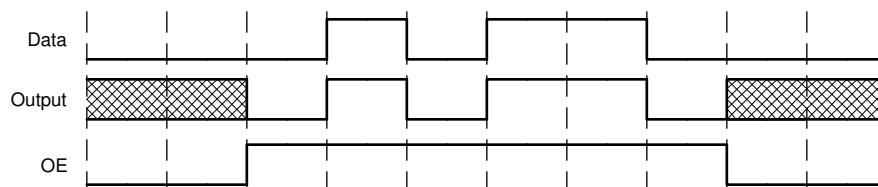


Figure 10. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 11](#).

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

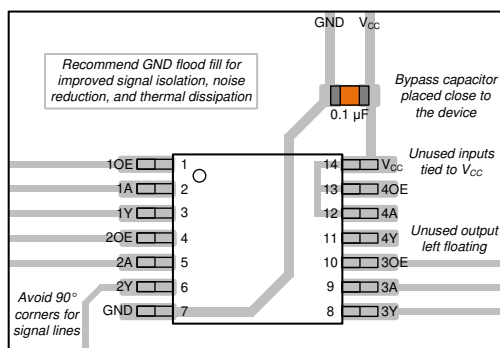


Figure 11. Example layout for the SN74HCS126-Q1

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [Reduce Noise and Save Power with the New HCS Logic Family](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary



[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS126QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS126Q1	
SN74HCS126QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS126Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS126-Q1 :

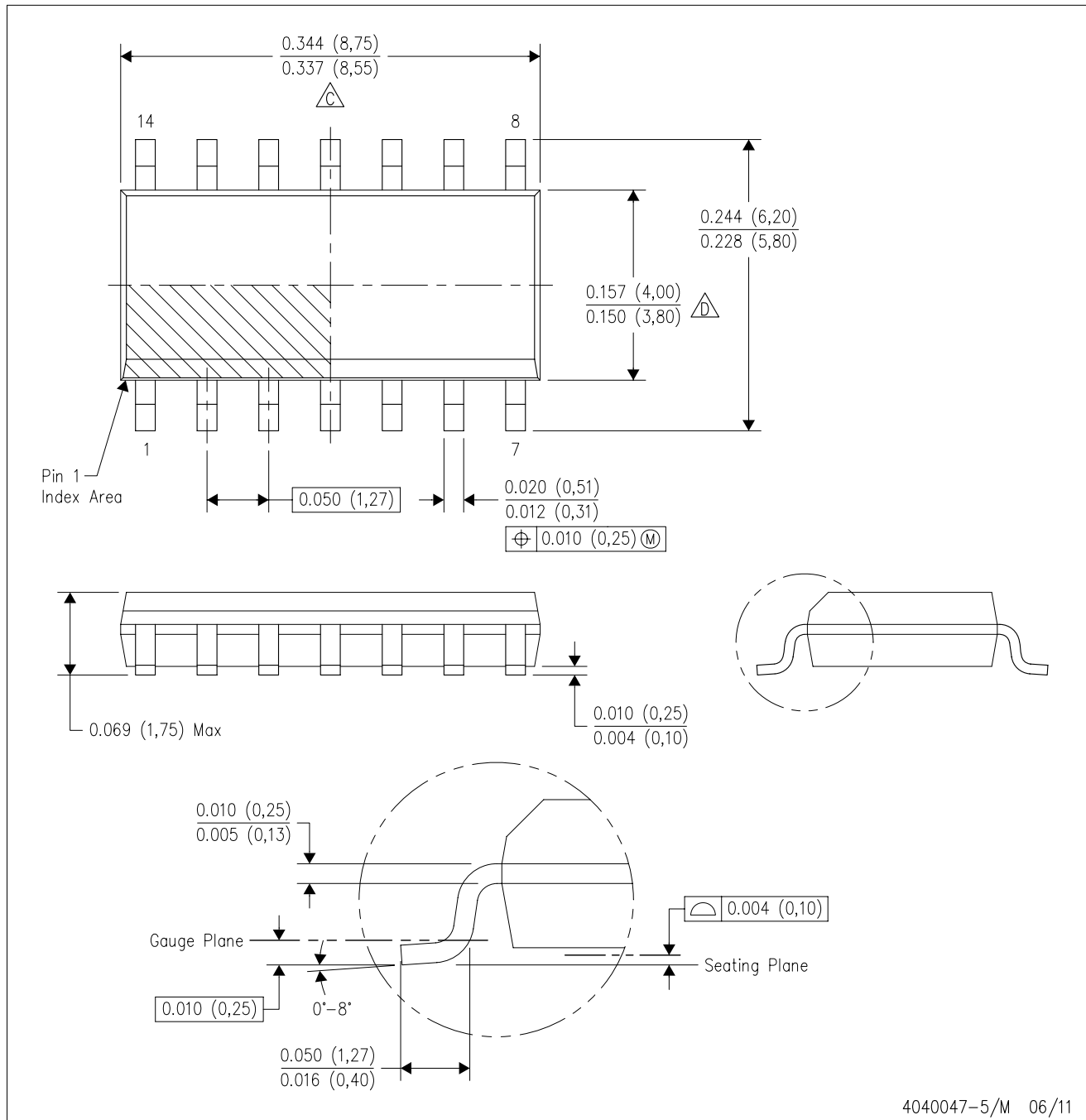
- Catalog: [SN74HCS126](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



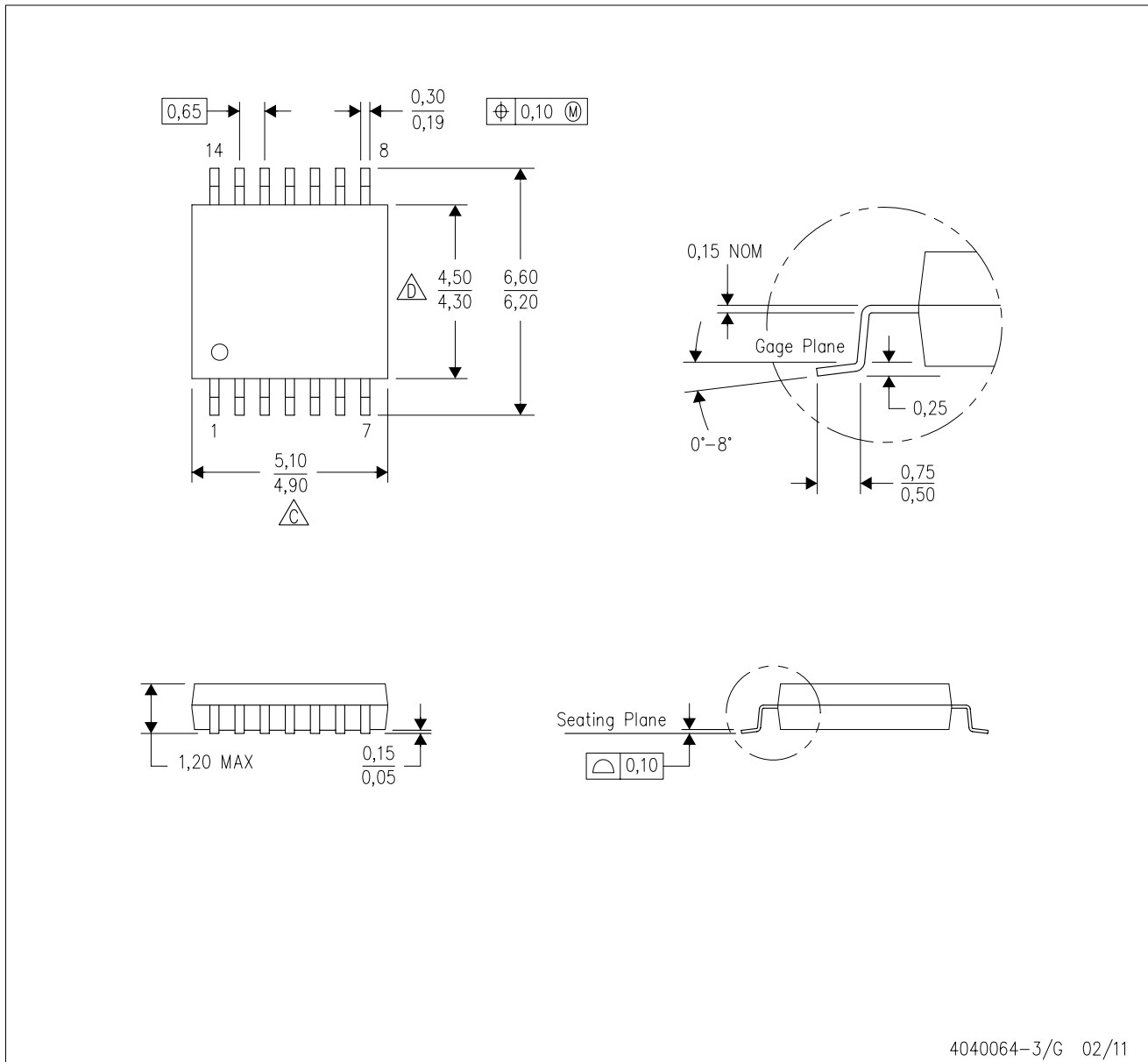
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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