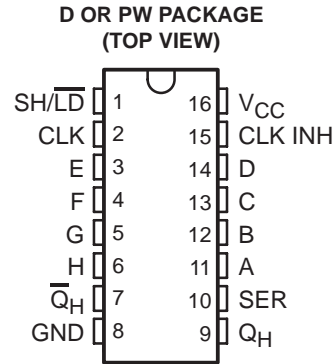


SN74HC165-Q1

8-BIT PARALLEL-LOAD SHIFT REGISTER

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- Qualified for Automotive Applications
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 13$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion



description/ordering information

The SN74HC165 is an 8-bit parallel-load shift register that, when clocked, shift the data toward a serial (QH) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/\overline{LD}) input. The SN74HC165 also features a clock-inhibit (CLK INH) function and a complementary serial (\overline{QH}) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/\overline{LD} is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/\overline{LD} is held high. While SH/\overline{LD} is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

ORDERING INFORMATION†

| T_A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D | Tape and reel | SN74HC165QDRQ1 | HC165Q1 |
| | TSSOP – PW | Tape and reel | SN74HC165QPWRQ1 | HC165Q1 |

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN74HC165-Q1

8-BIT PARALLEL-LOAD SHIFT REGISTER

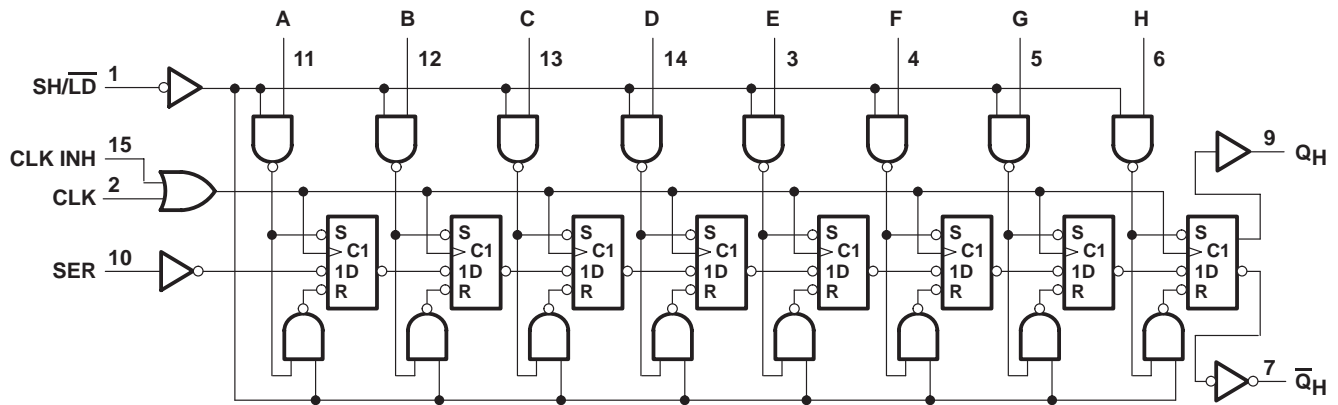
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FUNCTION TABLE

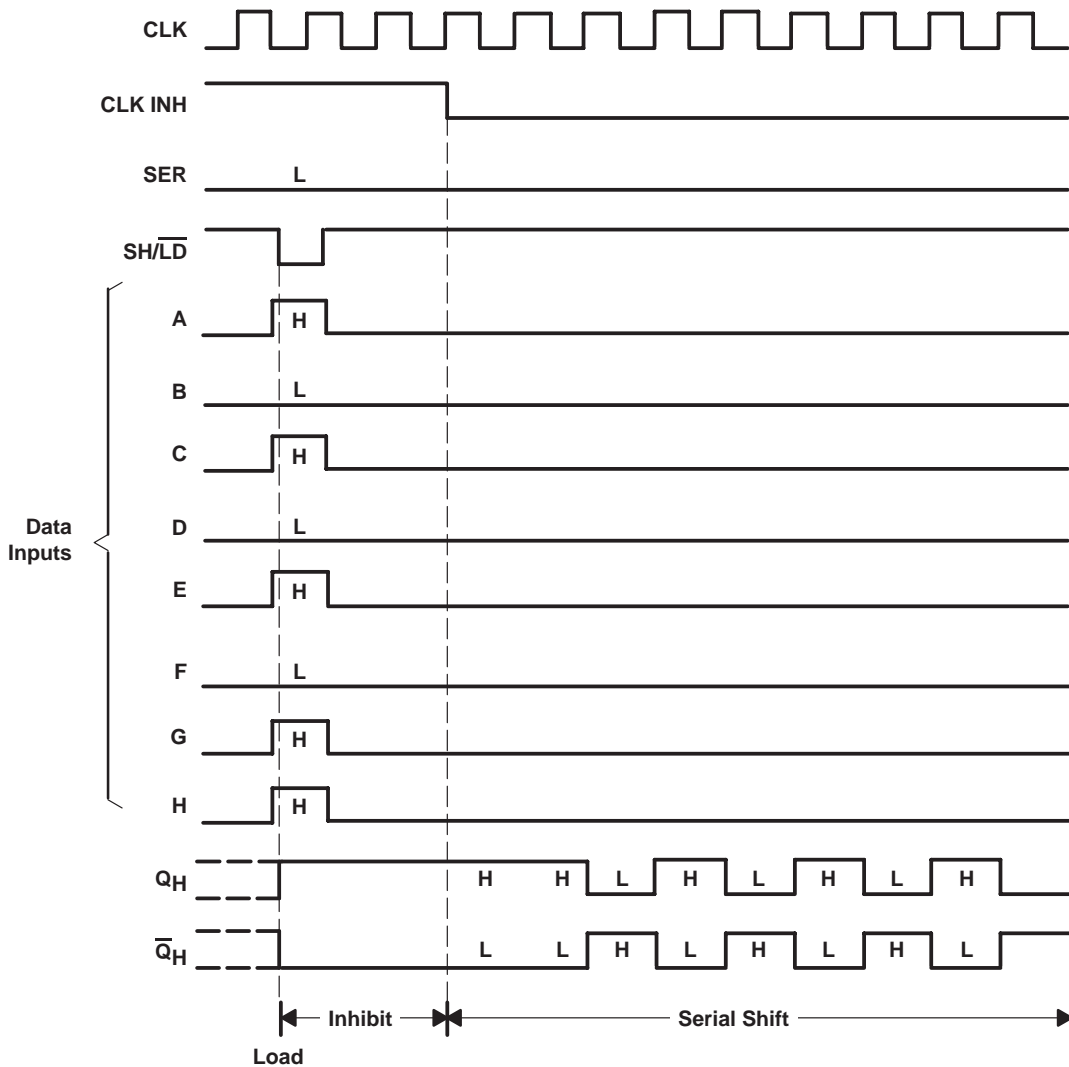
| INPUTS | | | FUNCTION |
|--------|-----|---------|---------------|
| SH/LD | CLK | CLK INH | |
| L | X | X | Parallel load |
| H | H | X | No change |
| H | X | H | No change |
| H | L | ↑ | Shift† |
| H | ↑ | L | Shift† |

† Shift = content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

logic diagram (positive logic)



typical shift, load, and inhibit sequence



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 73°C/W |
| PW package | 108°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|------------------------------|---------------------------------|------------------|------|----------|------|
| V_{CC} | Supply voltage | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | |
| | | $V_{CC} = 6$ V | 4.2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | V |
| $\Delta t/\Delta v^\ddagger$ | Input transition rise/fall time | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | -40 | | 125 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

[‡] If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|---|--------------------------|-----------------------|-------|-------|-----|-----|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | 3.7 | | |
| | | | 6 V | 5.48 | 5.8 | 5.2 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | 0.002 | 0.1 | 0.1 | V | |
| | | | 4.5 V | 0.001 | 0.1 | 0.1 | | |
| | | | 6 V | 0.001 | 0.1 | 0.1 | | |
| | | I _{OL} = 4 mA | 4.5 V | 0.17 | 0.26 | 0.4 | | |
| | | | 6 V | 0.15 | 0.26 | 0.4 | | |
| I _I | V _I = V _{CC} or 0 | 6 V | ±0.1 | ±100 | ±1000 | nA | | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | 8 | 160 | μA | | |
| C _i | | 2 V to 6 V | | 3 | 10 | 10 | pF | |

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8-BIT PARALLEL-LOAD SHIFT REGISTER

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | MIN | MAX | UNIT |
|--------------------|--|-----------------|-----------------------|-----|-----|-----|------|
| | | | MIN | MAX | | | |
| f _{clock} | Clock frequency | 2 V | 6 | | 4.2 | | MHz |
| | | 4.5 V | 31 | | 21 | | |
| | | 6 V | 36 | | 25 | | |
| t _w | SH/ $\overline{\text{LD}}$ low | 2 V | 80 | | 120 | | ns |
| | | 4.5 V | 16 | | 24 | | |
| | | 6 V | 14 | | 20 | | |
| | CLK high or low | 2 V | 80 | | 120 | | |
| | | 4.5 V | 16 | | 24 | | |
| | | 6 V | 14 | | 20 | | |
| t _{su} | SH/ $\overline{\text{LD}}$ high before CLK \uparrow | 2 V | 80 | | 120 | | ns |
| | | 4.5 V | 16 | | 24 | | |
| | | 6 V | 14 | | 20 | | |
| | SER before CLK \uparrow | 2 V | 40 | | 60 | | |
| | | 4.5 V | 8 | | 12 | | |
| | | 6 V | 7 | | 10 | | |
| | CLK INH low before CLK \uparrow | 2 V | 100 | | 150 | | |
| | | 4.5 V | 20 | | 30 | | |
| | | 6 V | 17 | | 25 | | |
| | CLK INH high before CLK \uparrow | 2 V | 40 | | 60 | | |
| | | 4.5 V | 8 | | 12 | | |
| | | 6 V | 7 | | 10 | | |
| | Data before SH/ $\overline{\text{LD}}$ \downarrow | 2 V | 100 | | 150 | | |
| | | 4.5 V | 20 | | 30 | | |
| | | 6 V | 17 | | 26 | | |
| t _h | SER data after CLK \uparrow | 2 V | 5 | | 5 | | ns |
| | | 4.5 V | 5 | | 5 | | |
| | | 6 V | 5 | | 5 | | |
| | PAR data after SH/ $\overline{\text{LD}}$ \downarrow | 2 V | 5 | | 5 | | |
| | | 4.5 V | 5 | | 5 | | |
| | | 6 V | 5 | | 5 | | |



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|---------------------|------------------------------------|-----------------|-----------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| f _{max} | | | 2 V | 6 | 13 | | 4.2 | MHz | |
| | | | 4.5 V | 31 | 50 | | 21 | | |
| | | | 6 V | 36 | 62 | | 25 | | |
| t _{pd} | SH/ \overline{LD} | Q _H or \overline{Q}_H | 2 V | | 80 | 150 | | 225 | ns |
| | | | 4.5 V | | 20 | 30 | | 45 | |
| | | | 6 V | | 16 | 26 | | 38 | |
| | CLK | Q _H or \overline{Q}_H | 2 V | | 75 | 150 | | 225 | |
| | | | 4.5 V | | 15 | 30 | | 45 | |
| | | | 6 V | | 13 | 26 | | 38 | |
| | H | Q _H or \overline{Q}_H | 2 V | | 75 | 150 | | 225 | |
| | | | 4.5 V | | 15 | 30 | | 45 | |
| | | | 6 V | | 13 | 26 | | 38 | |
| t _t | | Any | 2 V | | 38 | 75 | | 110 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | |
| | | | 6 V | | 6 | 13 | | 19 | |

operating characteristics, T_A = 25°C

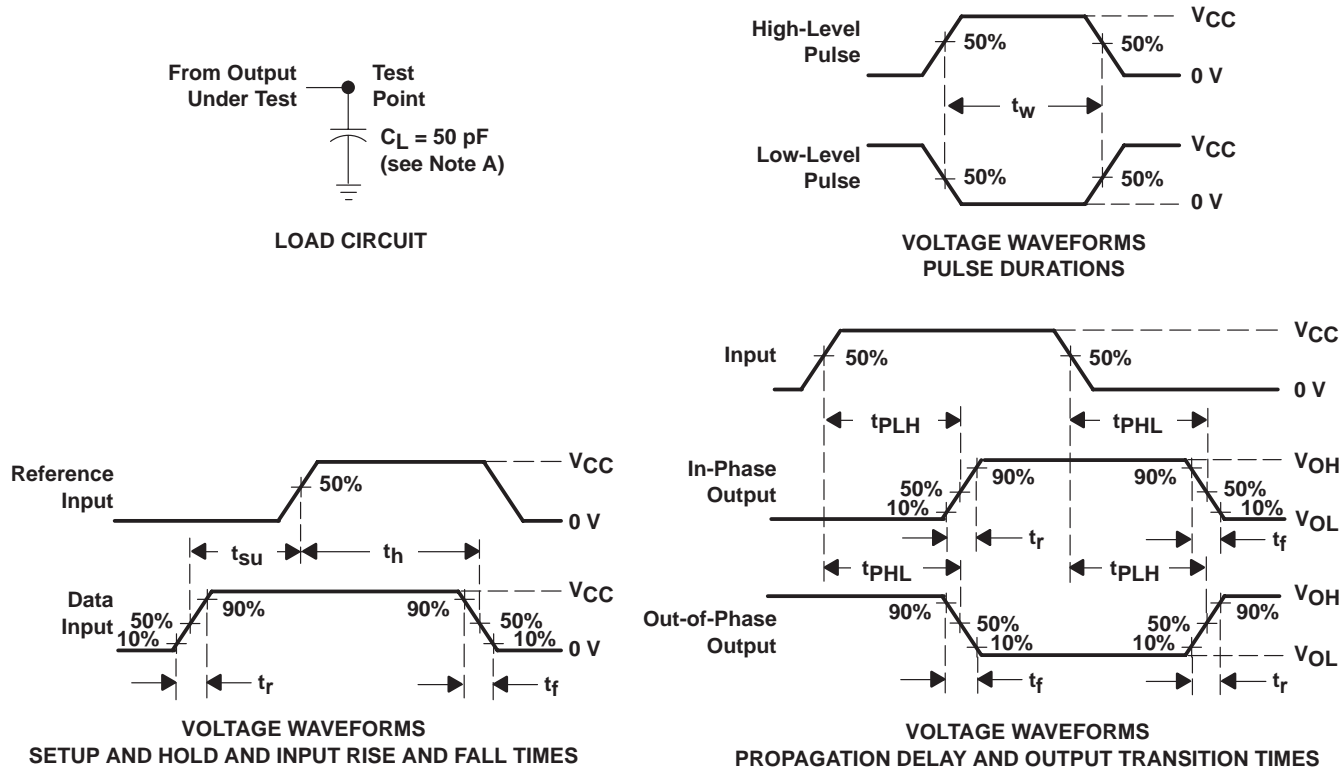
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | No load | 75 | pF |

SN74HC165-Q1

8-BIT PARALLEL-LOAD SHIFT REGISTER

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74HC165QDRQ1 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC165QQ1 | Samples |
| SN74HC165QPWRG4Q1 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC165Q1 | Samples |
| SN74HC165QPWRQ1 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC165Q1 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74HC165-Q1 :

- Catalog: [SN74HC165](#)
- Enhanced Product: [SN74HC165-EP](#)
- Military: [SN54HC165](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC165QPWRG4Q1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC165QPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC165QPWRG4Q1 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74HC165QPWRQ1 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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