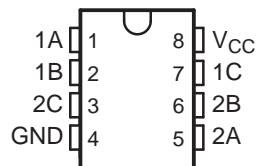


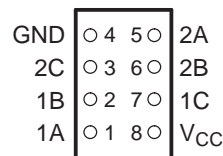
## FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Operates at 0.8 V to 2.7 V
- Sub-1-V Operable
- Max  $t_{pd}$  of 0.5 ns at 1.8 V
- Low Power Consumption, 10  $\mu$ A at 2.7 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE  
(TOP VIEW)



YZP PACKAGE  
(BOTTOM VIEW)



## DESCRIPTION/ORDERING INFORMATION

This dual analog switch is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.1-V to 2.7-V  $V_{CC}$  operation.

The SN74AUC2G66 can handle both analog and digital signals. It permits signals with amplitudes of up to 2.7-V (peak) to be transmitted in either direction.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G66YZPR	__ _U6_
	SSOP – DCT	Reel of 3000	SN74AUC2G66DCTR	U66__ _
	VSSOP – DCU	Reel of 3000	SN74AUC2G66DCUR	U66_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

## FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON



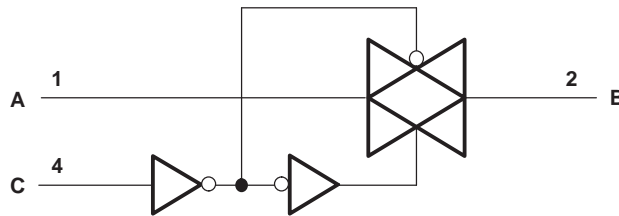
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

# SN74AUC2G66 DUAL BILATERAL ANALOG SWITCH

SCE5507A–NOVEMBER 2003–REVISED JANUARY 2007

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range <sup>(2)</sup>	-0.5	3.6	V
$V_I$	Input voltage range <sup>(2)(3)</sup>	-0.5	3.6	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Control input clamp current	$V_I < 0$		-50 mA
$I_{I/O}$	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		$\pm 50$ mA
$I_T$	On-state switch current	$V_{I/O} = 0$ to $V_{CC}$		$\pm 50$ mA
	Continuous current through $V_{CC}$ or GND			$\pm 100$ mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCT package		220
		DCU package		227
		YZP package		102
$T_{stg}$	Storage temperature range	-65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	0.8	2.7	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V	0	V
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.35 × V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
V <sub>I/O</sub>	I/O port voltage	0	V <sub>CC</sub>	V
V <sub>I</sub>	Control input voltage	0	3.6	V
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 0.8 V to 1.65 V <sup>(2)</sup>	20	ns/V
		V <sub>CC</sub> = 1.65 V to 2.3 V <sup>(3)</sup>	20	
		V <sub>CC</sub> = 2.3 V to 2.7 V <sup>(3)</sup>	20	
T <sub>A</sub>	Operating free-air temperature	−40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) The data was taken at C<sub>L</sub> = 15 pF, R<sub>L</sub> = 2 kΩ (see Figure 1).

(3) The data was taken at C<sub>L</sub> = 30 pF, R<sub>L</sub> = 500 Ω (see Figure 1).

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
r <sub>on</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>C</sub> = V <sub>IH</sub> (see Figure 1 and Figure 2)	I <sub>S</sub> = 4 mA	1.1 V	17	40	Ω
			1.65 V	7	20	
		I <sub>S</sub> = 8 mA	2.3 V	4	15	
r <sub>on(p)</sub>	V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>C</sub> = V <sub>IH</sub> (see Figure 1 and Figure 2)	I <sub>S</sub> = 4 mA	1.1 V	131	180	Ω
			1.65 V	32	80	
		I <sub>S</sub> = 8 mA	2.3 V	15	20	
Δr <sub>on</sub>	V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>C</sub> = V <sub>IH</sub> (see Figure 1 and Figure 2)	I <sub>S</sub> = 4 mA	1.1 V		3	Ω
			1.65 V		1	
		I <sub>S</sub> = 8 mA	2.3 V		1	
I <sub>S(off)</sub>	V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND, or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> , V <sub>C</sub> = V <sub>IL</sub> (see Figure 3)	2.7 V		±1	±0.1 <sup>(2)</sup>	μA
I <sub>S(on)</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>C</sub> = V <sub>IH</sub> , V <sub>O</sub> = Open (see Figure 4)	2.7 V		±1	±0.1 <sup>(2)</sup>	μA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V			±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V			10	μA
C <sub>ic</sub>		2.5 V		2.5		pF
C <sub>io(off)</sub>		2.5 V		3		pF
C <sub>io(on)</sub>		2.5 V		7		pF

(1) t<sub>a</sub> = 25°C

(2) The data was taken at C<sub>L</sub> = 15 pF, R<sub>L</sub> = 2 kΩ (see Figure 1).

# SN74AUC2G66

## DUAL BILATERAL ANALOG SWITCH

SCE5507A–NOVEMBER 2003–REVISED JANUARY 2007

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15$  pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V $\pm 0.1$ V	$V_{CC} = 1.5$ V $\pm 0.1$ V	$V_{CC} = 1.8$ V $\pm 0.15$ V	$V_{CC} = 2.5$ V $\pm 0.2$ V	UNIT
			TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
$t_{pd}^{(1)}$	A or B	B or A	1	0.6	0.5	0.5	0.4	ns
$t_{en}$	C	A or B	5	0.5 3	0.5 2.1	0.5 0.9 1.6	0.5 1.4	ns
$t_{dis}$	C	A or B	5.3	0.5 4	0.5 3	0.5 2.6 3.3	0.5 2.7	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V $\pm 0.15$ V			$V_{CC} = 2.5$ V $\pm 0.2$ V		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{pd}^{(1)}$	A or B	B or A			0.7		0.7	ns
$t_{en}$	C	A or B	0.5	1.6	2.7	0.5	2.3	ns
$t_{dis}$	C	A or B	0.5	2.7	3.4	0.5	2	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

### Analog Switch Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
Frequency response (switch ON)	A or B	B or A	$C_L = 50$ pF, $R_L = 600$ $\Omega$ , $f_{in} =$ sine wave (see Figure 6)	0.8 V	101	MHz
				1.1 V	150	
				1.4 V	175	
				1.65 V	250	
				2.3 V	400	
			$C_L = 5$ pF, $R_L = 50$ $\Omega$ , $f_{in} =$ sine wave (see Figure 6)	0.8 V	450	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	
Crosstalk (between switches)	A or B	B or A	$C_L = 50$ pF, $R_L = 600$ $\Omega$ , $f_{in} = 1$ MHz (sine wave) (see Figure 7)	0.8 V	-60	dB
				1.1 V	-60	
				1.4 V	-60	
				1.65 V	-60	
				2.3 V	-60	
			$C_L = 5$ pF, $R_L = 50$ $\Omega$ , $f_{in} = 1$ MHz (sine wave) (see Figure 7)	0.8 V	-65	
				1.1 V	-65	
				1.4 V	-65	
				1.65 V	-65	
				2.3 V	-65	

### Analog Switch Characteristics (continued)

$T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
Crosstalk (control input to signal output)	C	A or B	$C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ , $f_{in} = 1\text{ MHz}$ (square wave) (see Figure 8)	0.8 V	9	mV
				1.1 V	14	
				1.4 V	15	
				1.65 V	16	
				2.3 V	20	
Feedthrough attenuation (switch OFF)	A or B	B or A	$C_L = 50\text{ pF}$ , $R_L = 600\ \Omega$ , $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9)	0.8 V	-50	dB
				1.1 V	-50	
				1.4 V	-50	
				1.65 V	-50	
				2.3 V	-50	
			$C_L = 5\text{ pF}$ , $R_L = 50\ \Omega$ , $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 9)	0.8 V	-60	
				1.1 V	-60	
				1.4 V	-60	
				1.65 V	-60	
				2.3 V	-60	
Sine-wave distortion	A or B	B or A	$C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ , $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10)	0.8 V	7	%
				1.1 V	0.256	
				1.4 V	0.04	
				1.65 V	0.03	
				2.3 V	0.01	
	A or B	B or A	$C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ , $f_{in} = 10\text{ kHz}$ (sine wave) (see Figure 10)	0.8 V	3.7	
				1.1 V	0.4	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

### Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	2.5	2.5	2.5	2.5	2.5	pF

PARAMETER MEASUREMENT INFORMATION

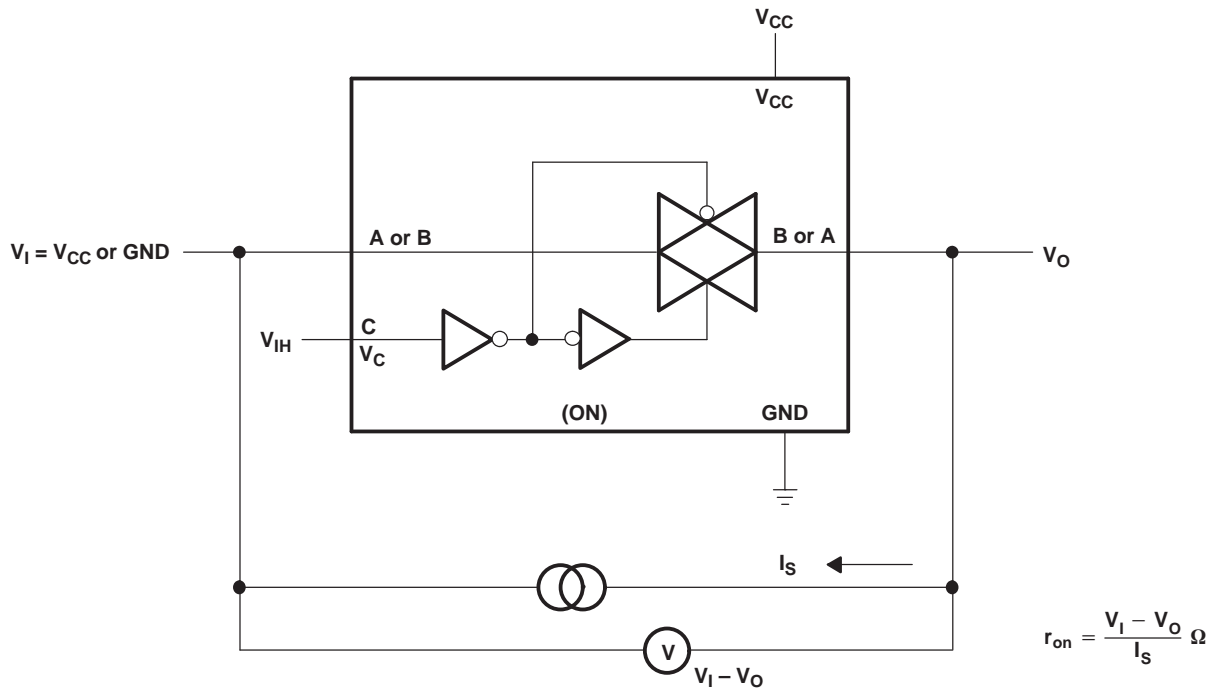


Figure 1. On-State Resistance Test Circuit

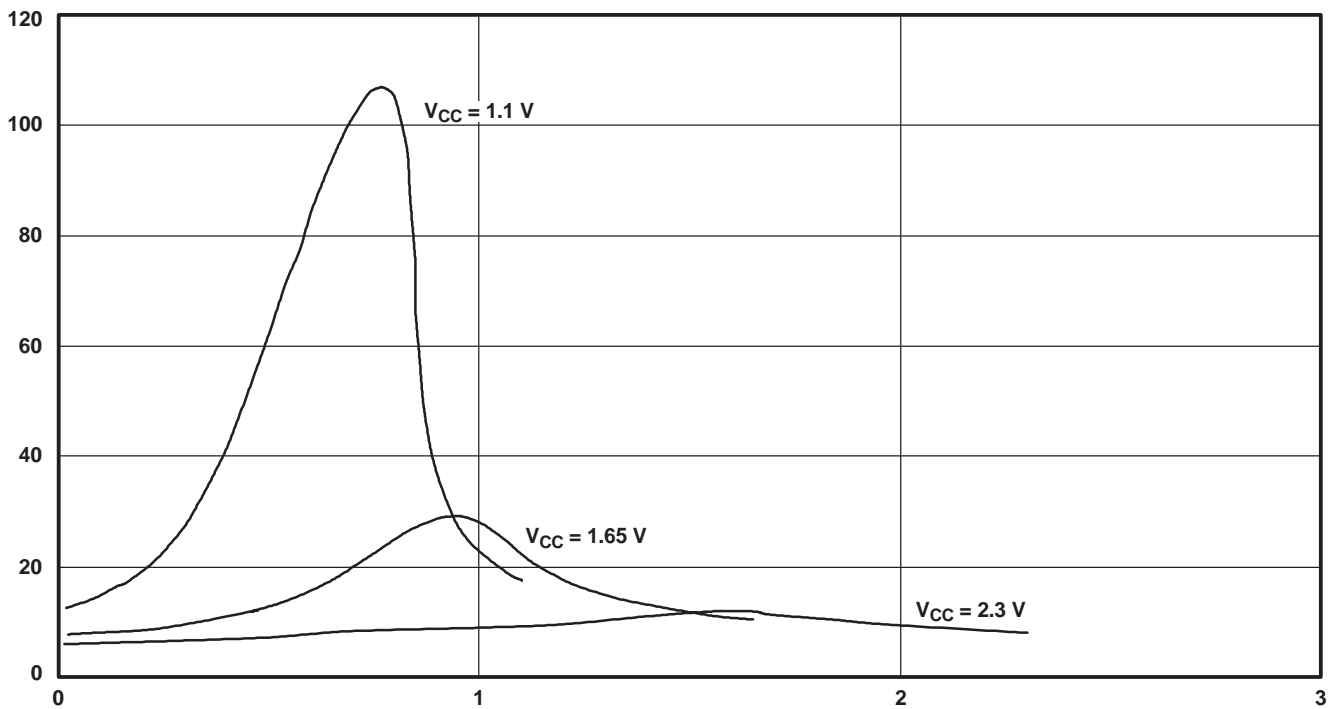
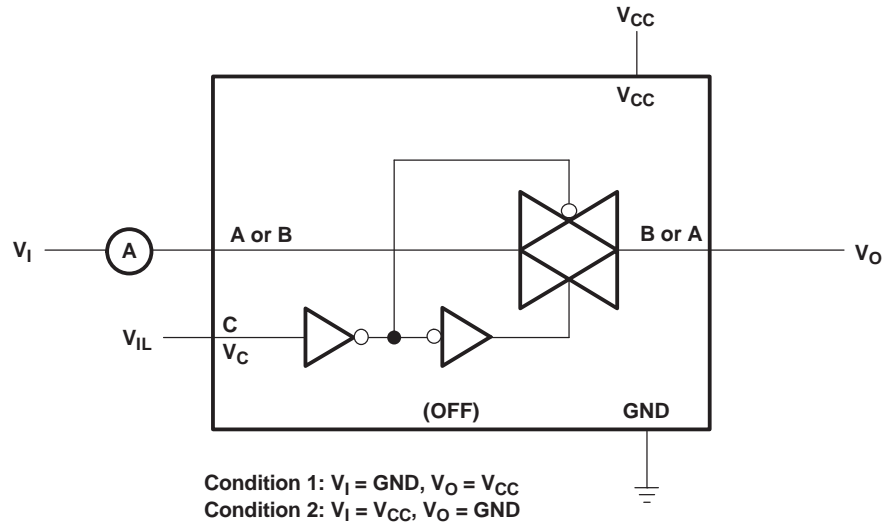
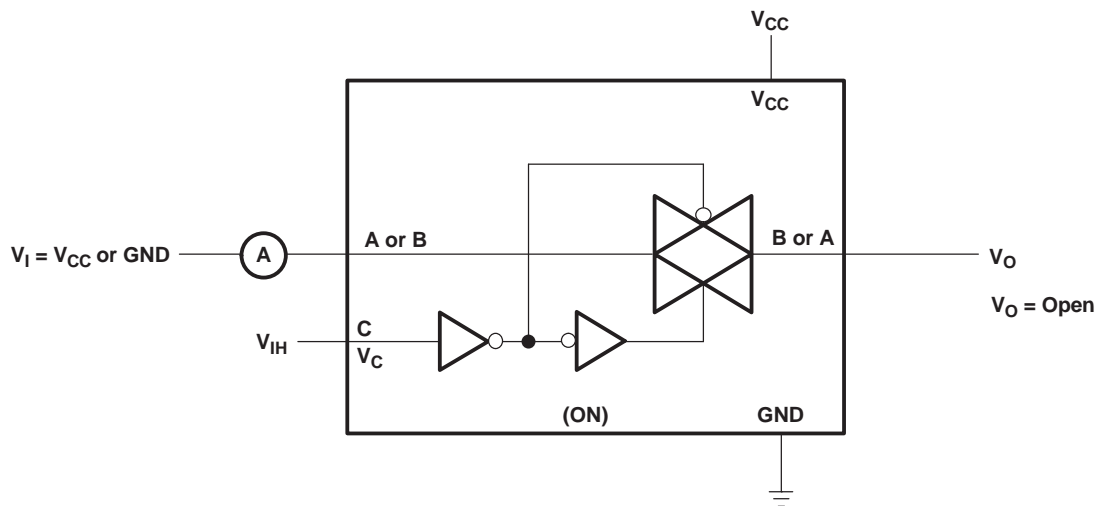


Figure 2. Typical  $r_{on}$  as a Function of Voltage ( $V_I$ ) for  $V_I = 0$  to  $V_{CC}$

**PARAMETER MEASUREMENT INFORMATION**

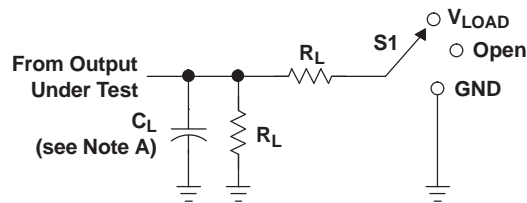


**Figure 3. Off-State Switch Leakage-Current Test Circuit**



**Figure 4. On-State Leakage-Current Test Circuit**

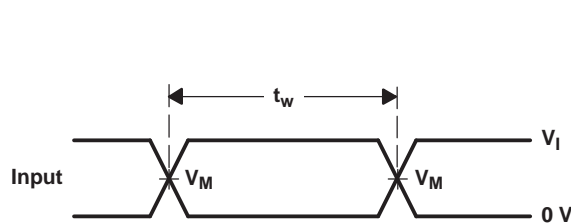
PARAMETER MEASUREMENT INFORMATION



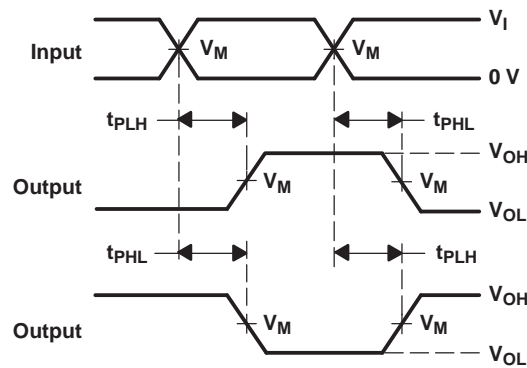
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

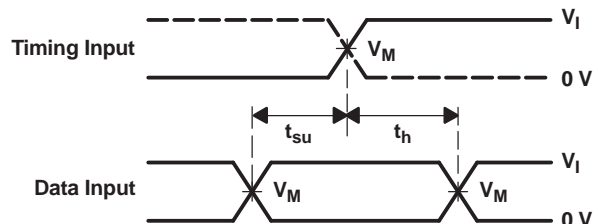
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
0.8 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 k $\Omega$	0.15 V
1.8 V $\pm$ 0.15 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V



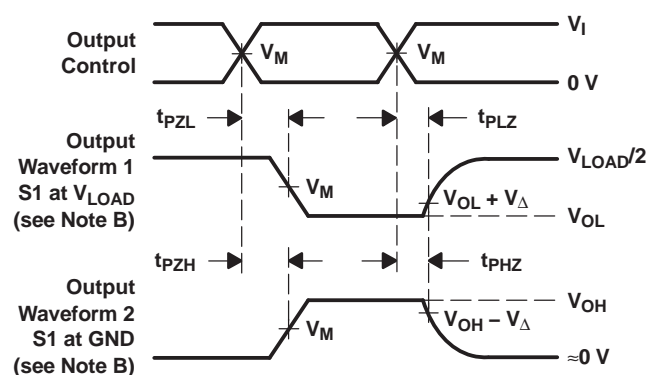
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



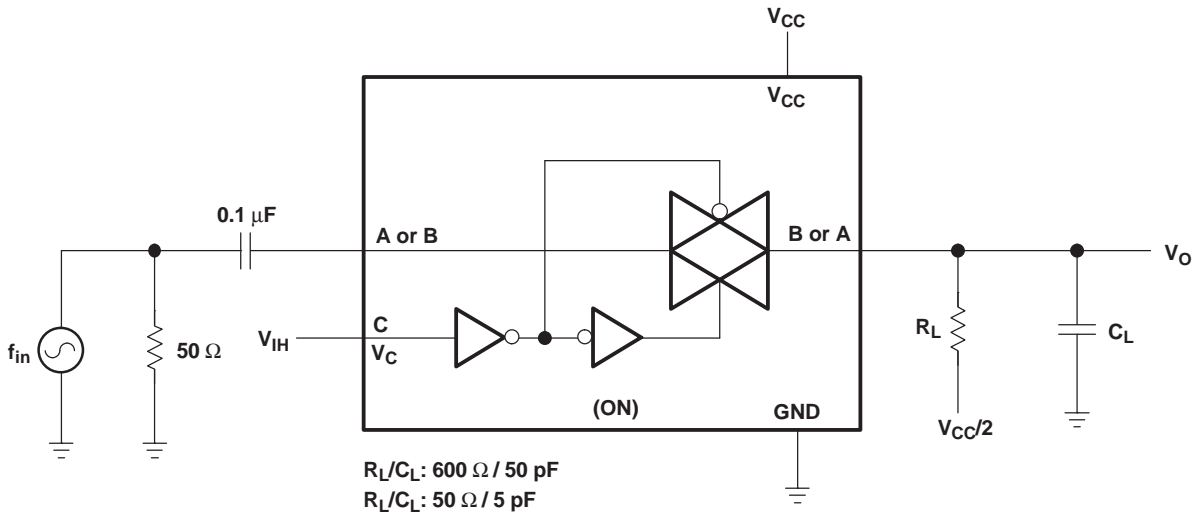
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

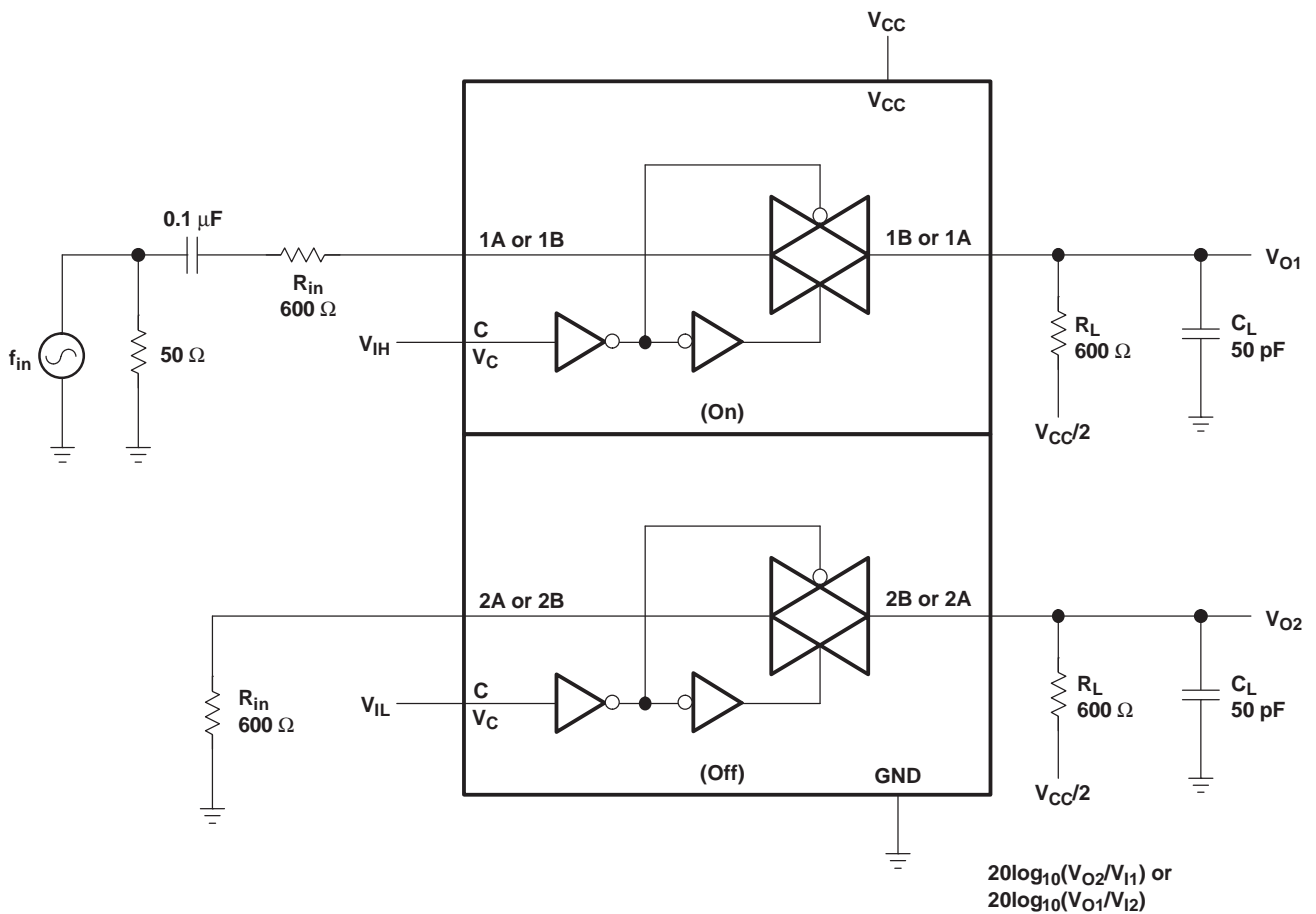
Figure 5. Load Circuit and Voltage Waveforms



**PARAMETER MEASUREMENT INFORMATION**

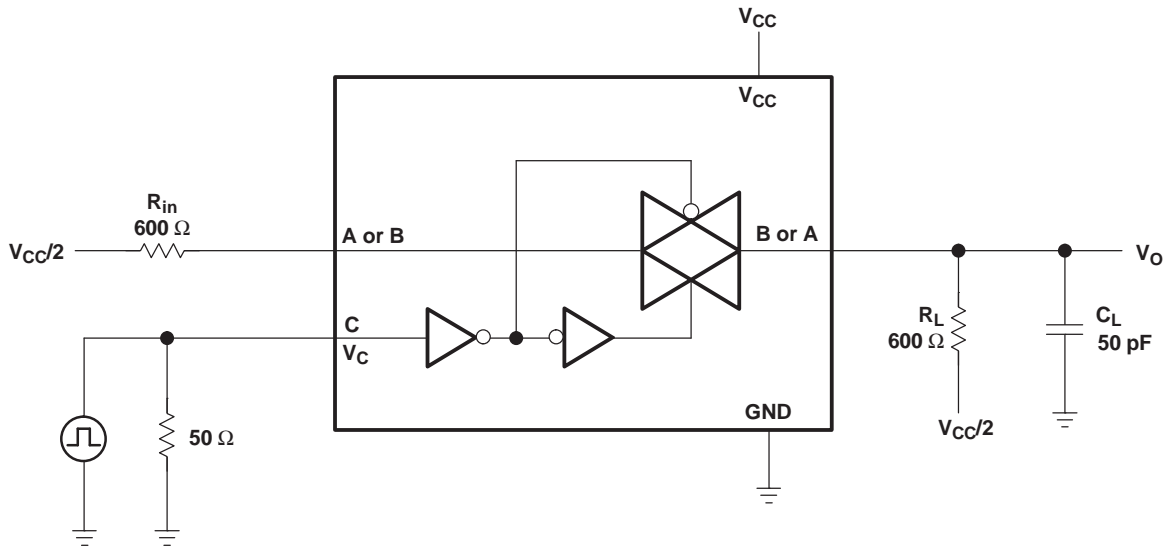


**Figure 6. Frequency Response (Switch ON)**

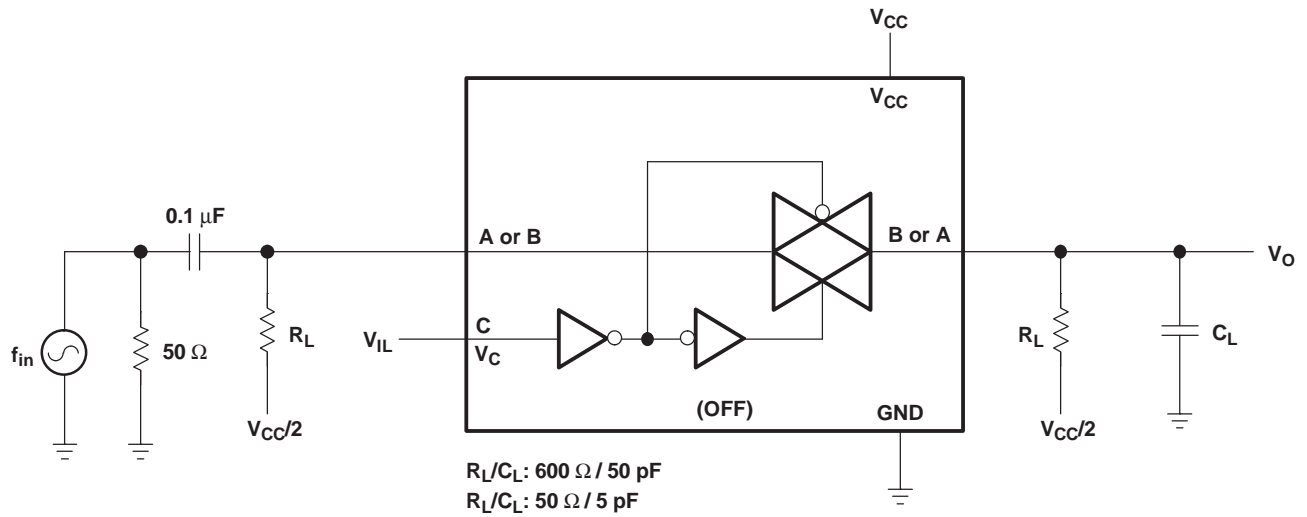


**Figure 7. Crosstalk (Between Switches)**

**PARAMETER MEASUREMENT INFORMATION**

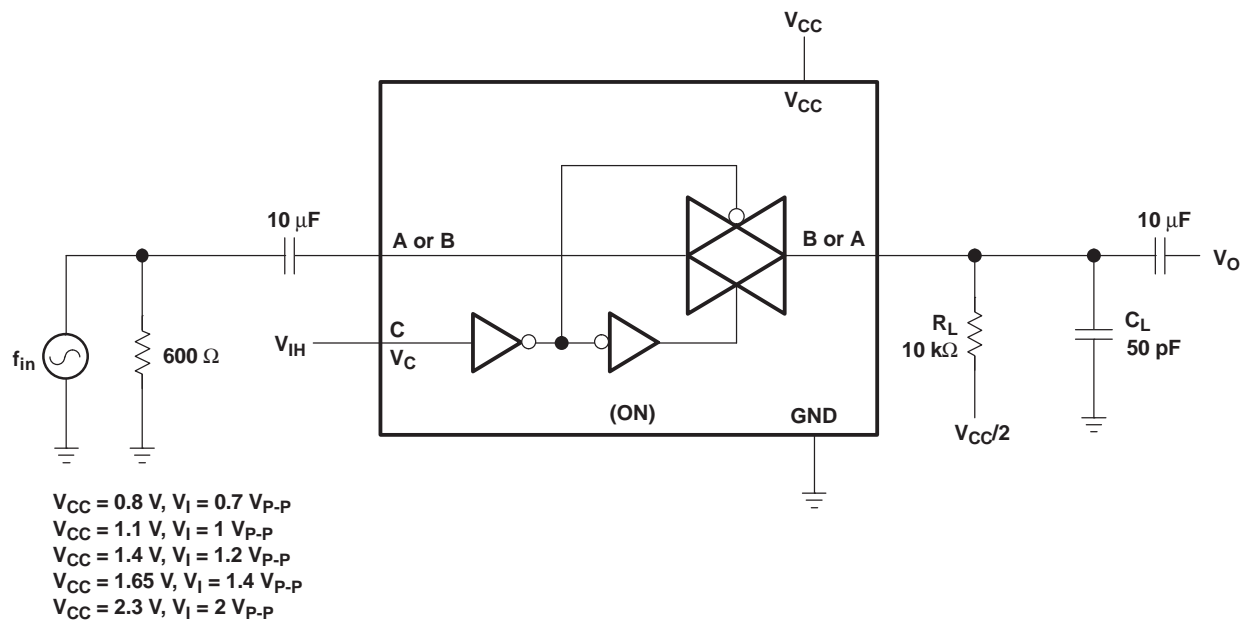


**Figure 8. Crosstalk (Control Input – Switch Output)**



**Figure 9. Feedthrough, Switch Off**

**PARAMETER MEASUREMENT INFORMATION**



**Figure 10. Sine-Wave Distortion**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AUC2G66DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G66DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G66DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G66DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G66DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G66YZPR	ACTIVE	WCSP	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G66DCUR	US8	DCU	8	3000	180.0	9.2	2.25	3.35	1.05	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**

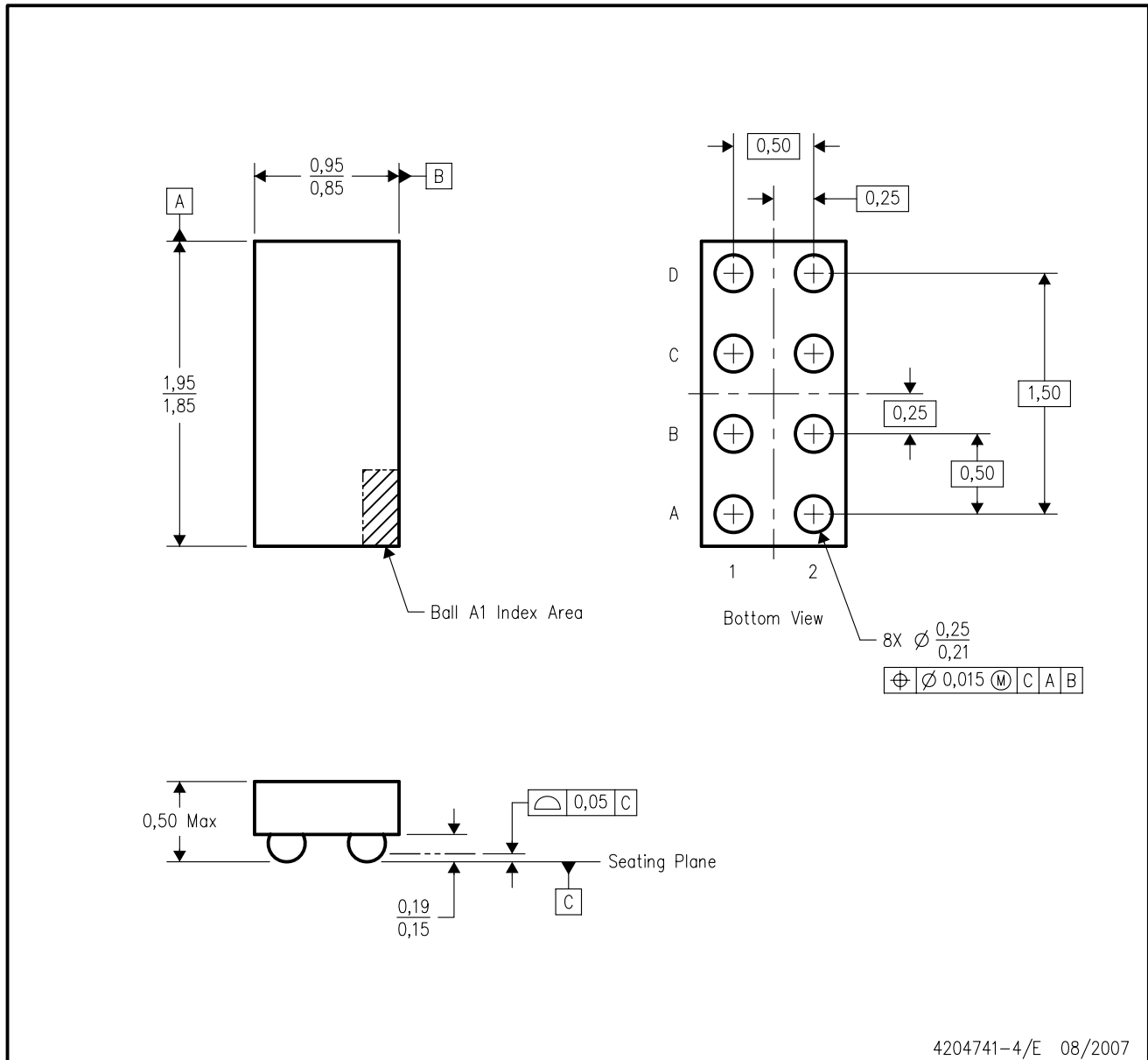


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G66DCUR	US8	DCU	8	3000	202.0	201.0	28.0

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



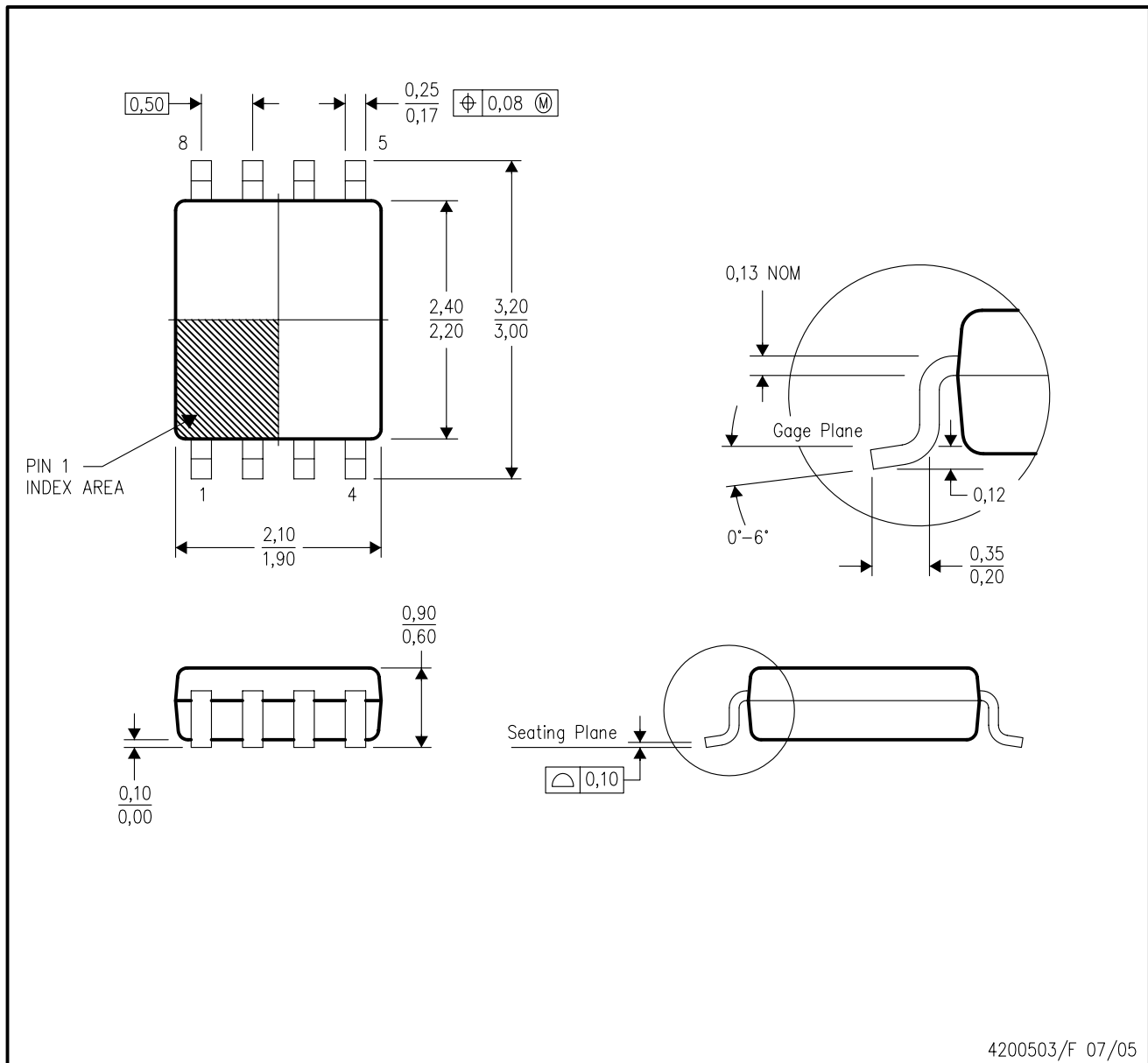
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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# MECHANICAL DATA

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-187 variation CA.



DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion  
 D. Falls within JEDEC MO-187 variation DA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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