

# SN54ACT573, SN74ACT573 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS538D – OCTOBER 1995 – REVISED OCTOBER 2002

- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 9.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible

## description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

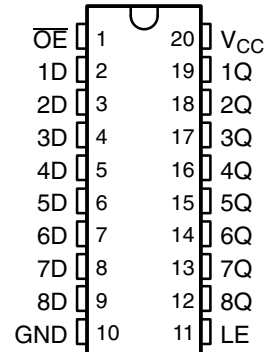
The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

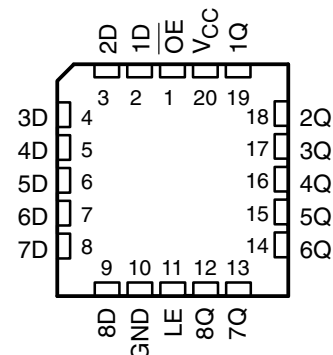
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ACT573 . . . J OR W PACKAGE  
SN74ACT573 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54ACT573 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| $T_A$          | PACKAGE†      |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | PDIP – N      | Tube          | SN74ACT573N           | SN74ACT573N      |
|                | SOIC – DW     | Tube          | SN74ACT573DW          | ACT573           |
|                |               | Tape and reel | SN74ACT573DWR         |                  |
|                | SOP – NS      | Tape and reel | SN74ACT573NSR         | ACT573           |
|                | SSOP – DB     | Tape and reel | SN74ACT573DBR         | AD573            |
| TSSOP – PW     | Tape and reel | SN74ACT573PWR | AD573                 |                  |
| -55°C to 125°C | CDIP – J      | Tube          | SNJ54ACT573J          | SNJ54ACT573J     |
|                | CFP – W       | Tube          | SNJ54ACT573W          | SNJ54ACT573W     |
|                | LCCC – FK     | Tube          | SNJ54ACT573FK         | SNJ54ACT573FK    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

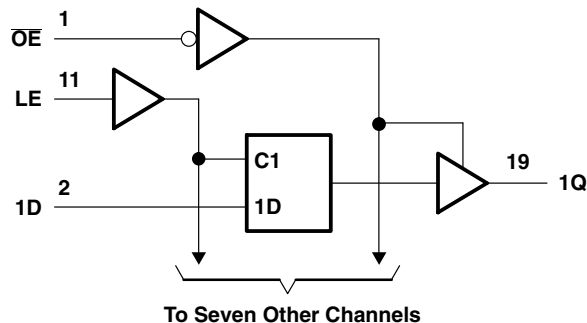
# SN54ACT573, SN74ACT573 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS538D – OCTOBER 1995 – REVISED OCTOBER 2002

FUNCTION TABLE  
(each latch)

| INPUTS          |    |   | OUTPUT |
|-----------------|----|---|--------|
| $\overline{OE}$ | LE | D | Q      |
| L               | H  | H | H      |
| L               | H  | L | L      |
| L               | L  | X | $Q_0$  |
| H               | X  | X | Z      |

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|  |                            |
|--|----------------------------|
| Supply voltage range, $V_{CC}$                                 | -0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                        | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, $V_O$ (see Note 1)                       | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )  | $\pm 20$ mA                |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) | $\pm 20$ mA                |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )     | $\pm 50$ mA                |
| Continuous current through, $V_{CC}$ or GND                    | $\pm 200$ mA               |
| Package thermal impedance, $\theta_{JA}$ (see Note 2):         |                            |
| DB package   | 70°C/W                     |
| DW package   | 58°C/W                     |
| N package  | 69°C/W                     |
| NS package   | 60°C/W                     |
| PW package   | 83°C/W                     |
| Storage temperature range, $T_{stg}$                           | -65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54ACT573, SN74ACT573 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS538D – OCTOBER 1995 – REVISED OCTOBER 2002

## recommended operating conditions (see Note 3)

|                 |                                    | SN54ACT573 |                 | SN74ACT573 |                 | UNIT |
|-----------------|------------------------------------|------------|-----------------|------------|-----------------|------|
|                 |                                    | MIN        | MAX             | MIN        | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     | 4.5        | 5.5             | 4.5        | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | 2          |                 | 2          |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            |            | 0.8             |            | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      | 0          | V <sub>CC</sub> | 0          | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                     | 0          | V <sub>CC</sub> | 0          | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          |            | -24             |            | -24             | mA   |
| I <sub>OL</sub> | Low-level output current           |            | 24              |            | 24              | mA   |
| Δt/Δv           | Input transition rise or fall rate |            | 8               |            | 8               | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     | -55        | 125             | -40        | 85              | °C   |

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                 | TEST CONDITIONS   | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      |       | SN54ACT573 |      | SN74ACT573 |     | UNIT |
|---------------------------|---|-----------------|-----------------------|------|-------|------------|------|------------|-----|------|
|                           |   |                 | MIN                   | TYP  | MAX   | MIN        | MAX  | MIN        | MAX |      |
| V <sub>OH</sub>           | I <sub>OH</sub> = -50 μA                                    | 4.5 V           | 4.4                   | 4.49 |       | 4.4        |      | 4.4        | V   |      |
|                           |   | 5.5 V           | 5.4                   | 5.49 |       | 5.4        |      | 5.4        |     |      |
|                           | I <sub>OH</sub> = -24 mA                                    | 4.5 V           | 3.86                  |      |       | 3.7        |      | 3.76       |     |      |
|                           |   | 5.5 V           | 4.86                  |      |       | 4.7        |      | 4.76       |     |      |
|                           | I <sub>OH</sub> = -50 mA†                                   | 5.5 V           |                       |      |       | 3.85       |      |            |     |      |
| I <sub>OH</sub> = -75 mA† | 5.5 V   |                 |                       |      |       |            | 3.85 |            |     |      |
| V <sub>OL</sub>           | I <sub>OL</sub> = 50 μA                                     | 4.5 V           |                       |      | 0.1   |            | 0.1  | 0.1        | V   |      |
|                           |   | 5.5 V           |                       |      | 0.1   |            | 0.1  | 0.1        |     |      |
|                           | I <sub>OL</sub> = 24 mA                                     | 4.5 V           |                       |      | 0.36  |            | 0.44 | 0.44       |     |      |
|                           |   | 5.5 V           |                       |      | 0.36  |            | 0.44 | 0.44       |     |      |
|                           | I <sub>OL</sub> = 50 mA†                                    | 5.5 V           |                       |      |       | 1.65       |      |            |     |      |
| I <sub>OL</sub> = 75 mA†  | 5.5 V   |                 |                       |      |       |            | 1.65 |            |     |      |
| I <sub>OZ</sub>           | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |      | ±0.25 |            | ±5   | ±2.5       | μA  |      |
| I <sub>I</sub>            | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |      | ±0.1  |            | ±1   | ±1         | μA  |      |
| I <sub>CC</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |      | 4     |            | 80   | 40         | μA  |      |
| ΔI <sub>CC</sub> ‡        | One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>  | 5.5 V           |                       | 0.6  |       |            | 1.5  | 1.5        | mA  |      |
| C <sub>i</sub>            | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 5    |       |            |      |            | pF  |      |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

|                 |                             | T <sub>A</sub> = 25°C |     | SN54ACT573 |     | SN74ACT573 |     | UNIT |
|-----------------|-----------------------------|-----------------------|-----|------------|-----|------------|-----|------|
|                 |                             | MIN                   | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>w</sub>  | Pulse duration, LE high     | 3.5                   |     | 5          |     | 4          |     | ns   |
| t <sub>su</sub> | Setup time, data before LE↓ | 3                     |     | 4.5        |     | 3.5        |     | ns   |
| t <sub>h</sub>  | Hold time, data after LE↓   | 0                     |     | 1          |     | 0          |     | ns   |



**SN54ACT573, SN74ACT573**  
**OCTAL D-TYPE TRANSPARENT LATCHES**  
**WITH 3-STATE OUTPUTS**

SCAS538D – OCTOBER 1995 – REVISED OCTOBER 2002

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

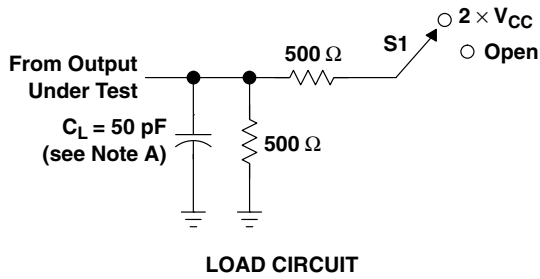
| PARAMETER | FROM (INPUT)           | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ |     |      | SN54ACT573 |      | SN74ACT573 |      | UNIT |
|-----------|------------------------|-------------|--------------------------|-----|------|------------|------|------------|------|------|
|           |                        |             | MIN                      | TYP | MAX  | MIN        | MAX  | MIN        | MAX  |      |
| $t_{PLH}$ | D                      | Q           | 2.5                      | 6   | 10.5 | 1.5        | 13.5 | 2          | 12   | ns   |
| $t_{PHL}$ |                        |             | 2.5                      | 6   | 10.5 | 1.5        | 13.5 | 2          | 12   |      |
| $t_{PLH}$ | LE                     | Q           | 3                        | 6   | 10.5 | 1.5        | 13   | 2.5        | 12   | ns   |
| $t_{PHL}$ |                        |             | 2.5                      | 5.5 | 9.5  | 1.5        | 12   | 2          | 10.5 |      |
| $t_{PZH}$ | OE                     | Q           | 2                        | 5.5 | 10   | 1.5        | 11.5 | 1.5        | 11   | ns   |
| $t_{PZL}$ |                        |             | 1.5                      | 5.5 | 9.5  | 1.5        | 11   | 1.5        | 10.5 |      |
| $t_{PHZ}$ | $\overline{\text{OE}}$ | Q           | 2.5                      | 6.5 | 11   | 1.5        | 13.5 | 1.5        | 12.5 | ns   |
| $t_{PLZ}$ |                        |             | 1.5                      | 5   | 8.5  | 1.5        | 10.5 | 1          | 9.5  |      |

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

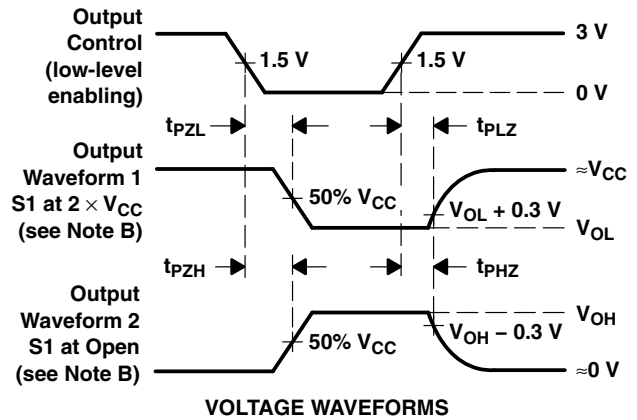
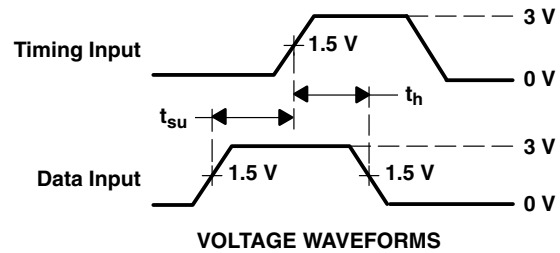
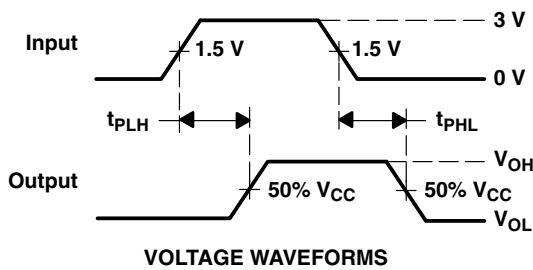
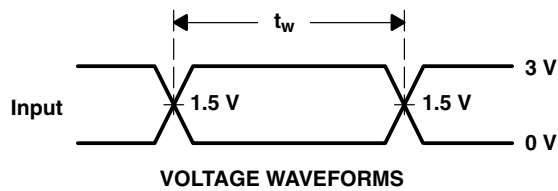
| PARAMETER                              | TEST CONDITIONS                           | TYP | UNIT |
|--|---|-----|------|
| $C_{pd}$ Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 25  | pF   |



PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open              |







- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                 | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-87664012A   | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>87664012A<br>SNJ54ACT<br>573FK | <a href="#">Samples</a> |
| 5962-8766401RA   | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-8766401RA<br>SNJ54ACT573J          | <a href="#">Samples</a> |
| 5962-8766401SA   | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-8766401SA<br>SNJ54ACT573W          | <a href="#">Samples</a> |
| SN74ACT573DBLE   | OBSOLETE      | SSOP         | DB                 | 20   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |   |                         |
| SN74ACT573DBR    | ACTIVE        | SSOP         | DB                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AD573                                   | <a href="#">Samples</a> |
| SN74ACT573DW     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ACT573                                  | <a href="#">Samples</a> |
| SN74ACT573DWG4   | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ACT573                                  | <a href="#">Samples</a> |
| SN74ACT573DWR    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ACT573                                  | <a href="#">Samples</a> |
| SN74ACT573DWRG4  | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ACT573                                  | <a href="#">Samples</a> |
| SN74ACT573N      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | SN74ACT573N                             | <a href="#">Samples</a> |
| SN74ACT573NE4    | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | SN74ACT573N                             | <a href="#">Samples</a> |
| SN74ACT573NSR    | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ACT573                                  | <a href="#">Samples</a> |
| SN74ACT573NSRE4  | ACTIVE        | SO           | NS                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ACT573                                  | <a href="#">Samples</a> |
| SN74ACT573PW     | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AD573                                   | <a href="#">Samples</a> |
| SN74ACT573PWG4   | ACTIVE        | TSSOP        | PW                 | 20   | 70             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AD573                                   | <a href="#">Samples</a> |
| SN74ACT573PWLE   | OBSOLETE      | TSSOP        | PW                 | 20   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |   |                         |
| SN74ACT573PWR    | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AD573                                   | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                 | Samples   |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|---|
| SN74ACT573PWRE4  | ACTIVE        | TSSOP        | PW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AD573                                   |  |
| SNJ54ACT573FK    | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>87664012A<br>SNJ54ACT<br>573FK |  |
| SNJ54ACT573J     | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-8766401RA<br>SNJ54ACT573J          |  |
| SNJ54ACT573W     | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-8766401SA<br>SNJ54ACT573W          |  |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ACT573, SN74ACT573 :**

- Catalog: [SN74ACT573](#)
- Military: [SN54ACT573](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

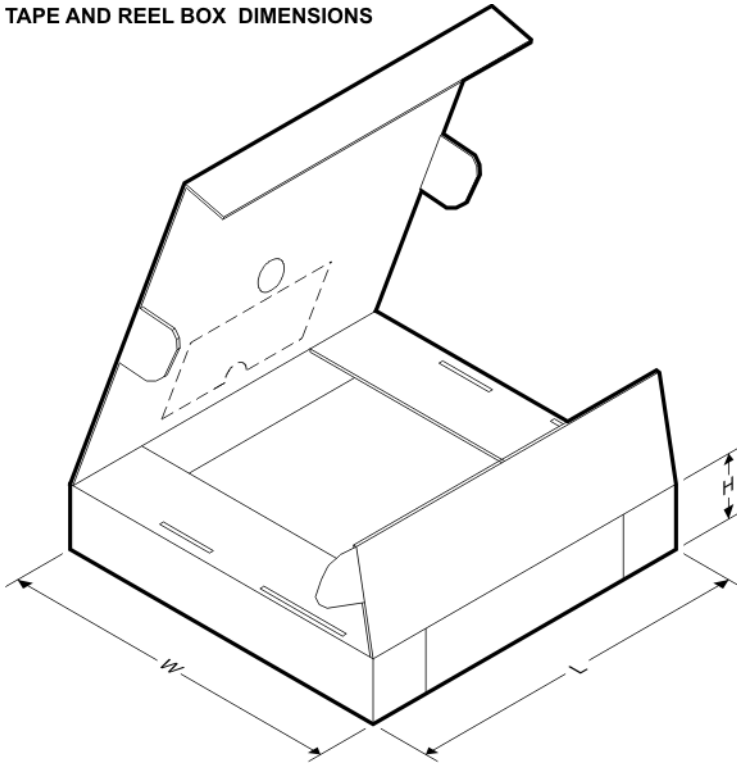


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT573DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ACT573DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ACT573NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 9.0     | 13.0    | 2.4     | 4.0     | 24.0   | Q1            |
| SN74ACT573PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


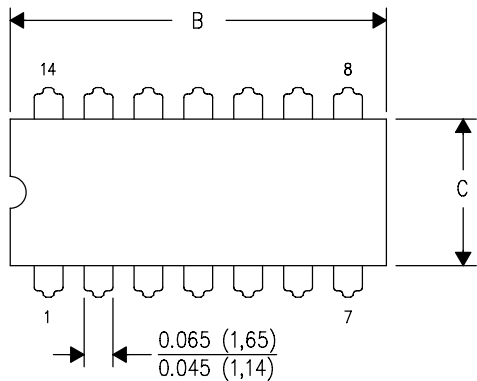
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT573DBR | SSOP         | DB              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74ACT573DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74ACT573NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74ACT573PWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |

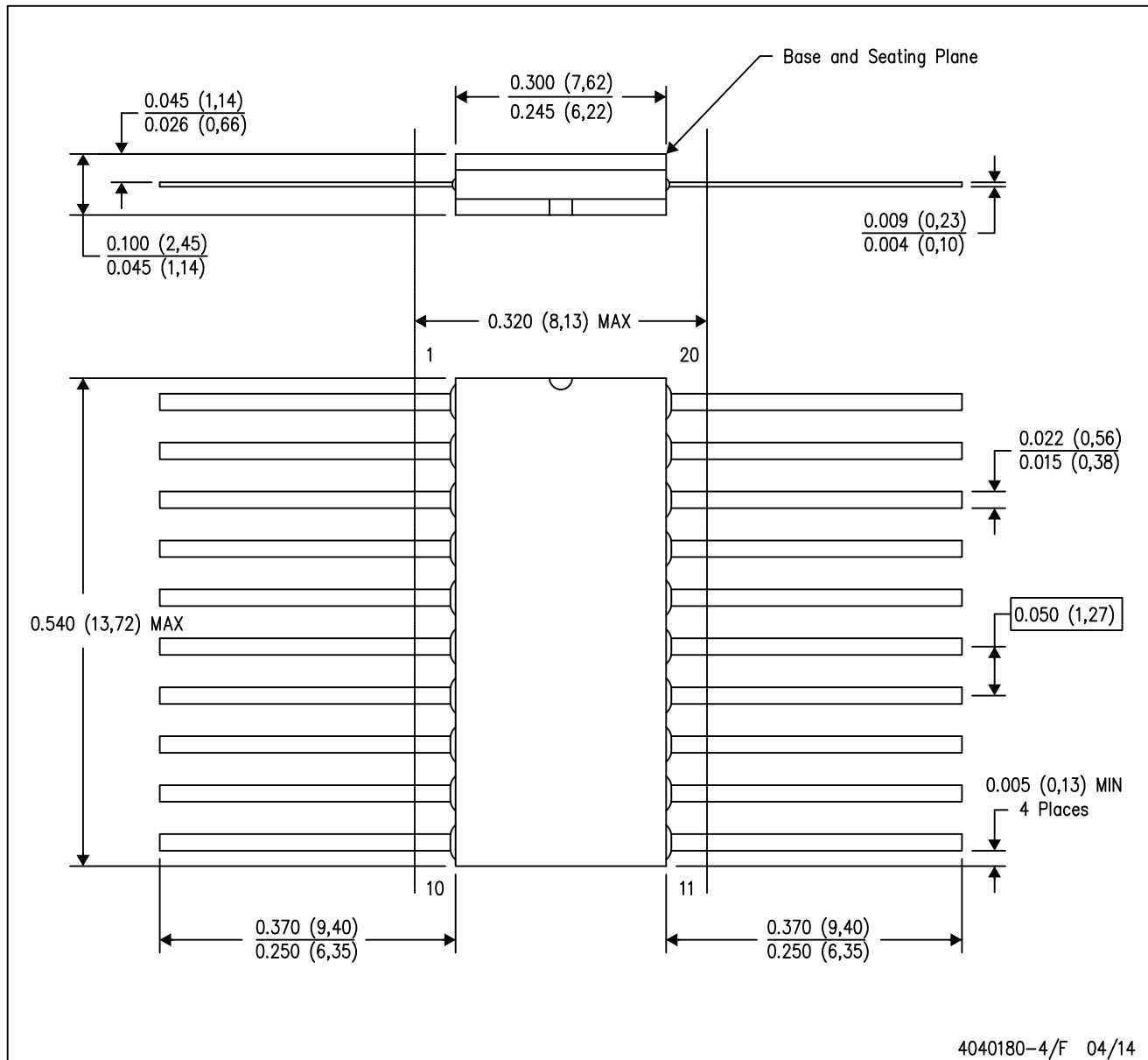


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

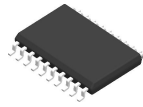
PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

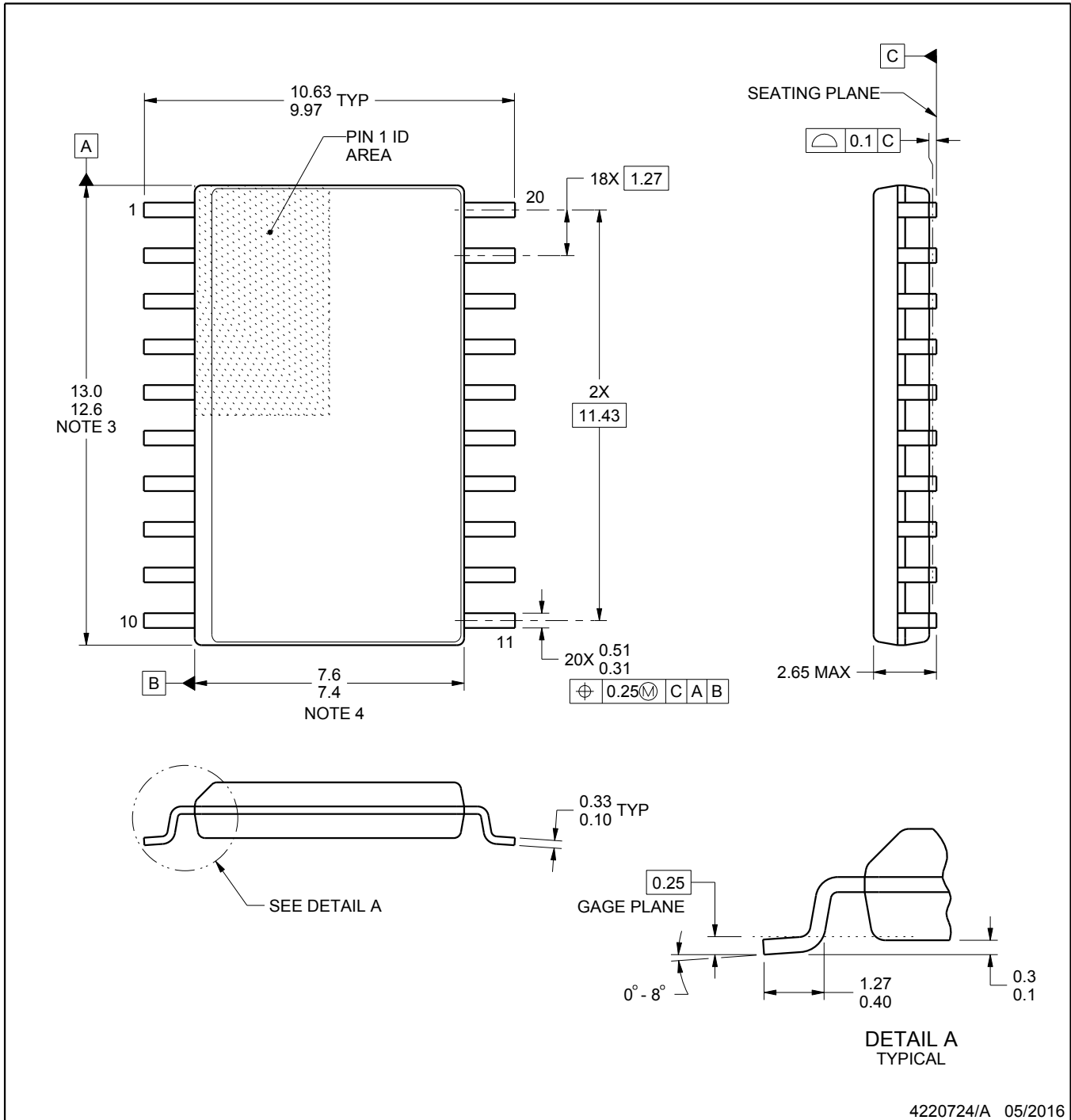
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

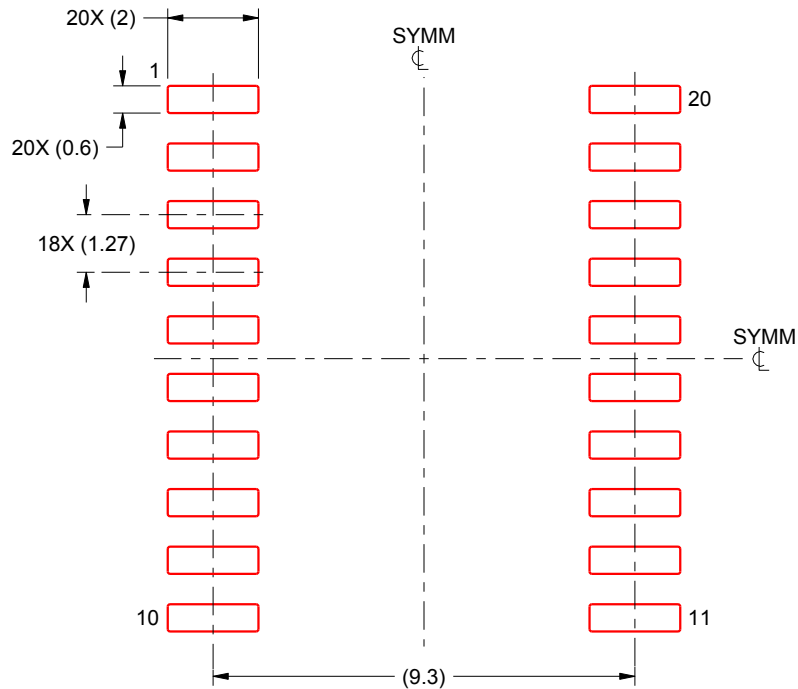


# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

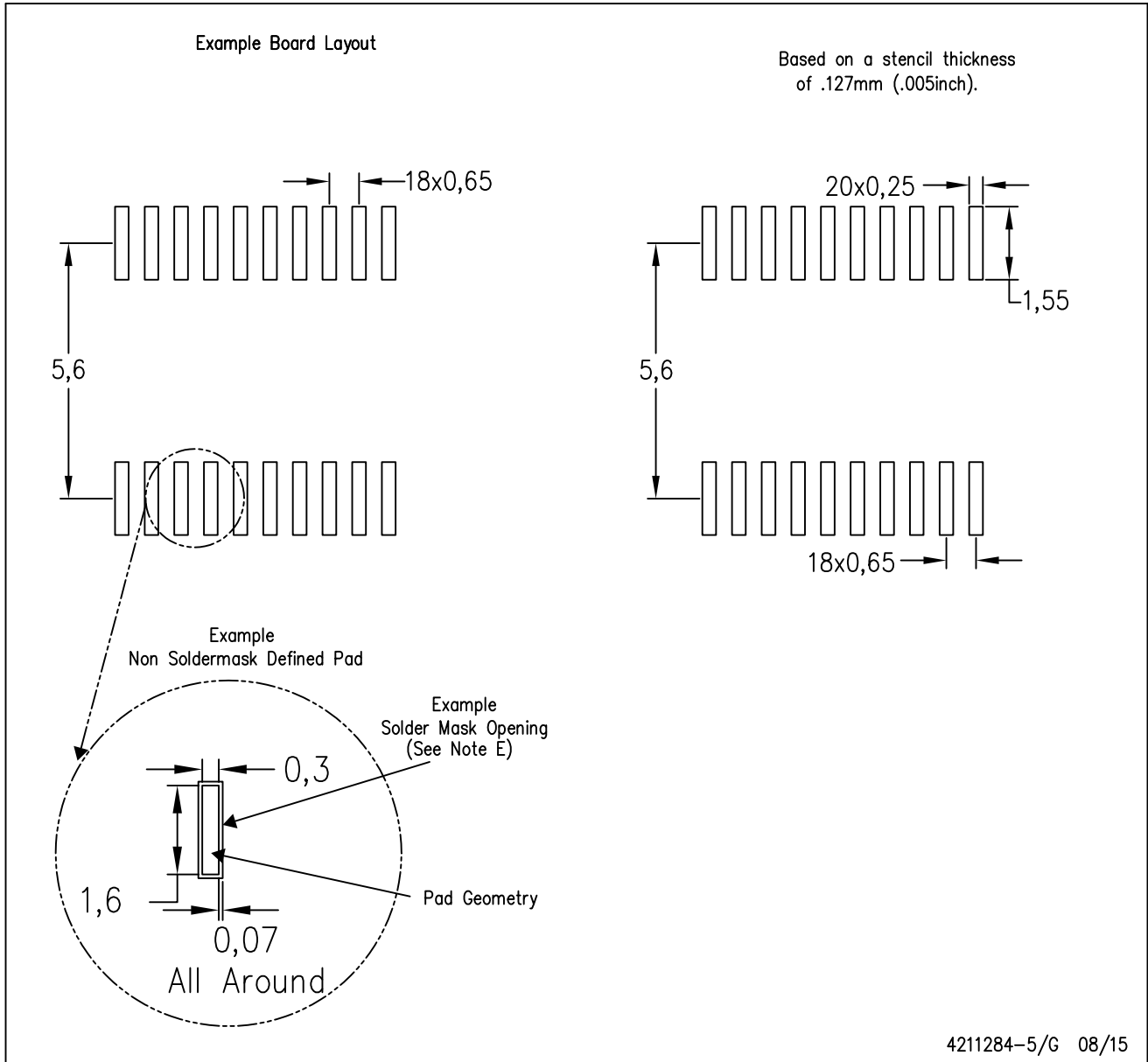
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)