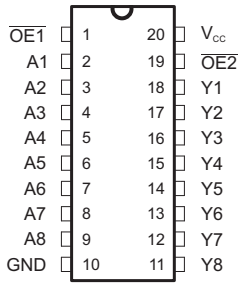
# SN54ABT541, SN74ABT541B OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS093L – DECEMBER 1993 – REVISED DECEMBER 2006

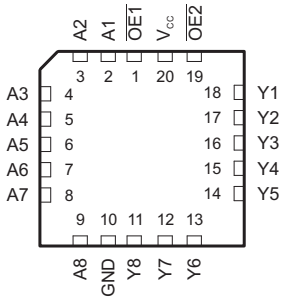
## FEATURES

- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V at $V_{CC}$ = 5 V, $T_A$ = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (J) DIPs**

**SN54ABT541...J OR W PACKAGE**
**SN74ABT541B...DB, DW, N, OR PW PACKAGE**
**(TOP VIEW)**




**SN54ABT541...FK PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

The SN54ABT541 and SN74ABT541B octal buffers and line drivers are ideal for driving bus lines or buffering memory address registers. The devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Reel of 1000 | SN74ABT541BN | SN74ABT541BN |
| | SOIC – DW | Tube of 25 | SN74ABT541BDW | ABT541B |
| | | Reel of 2000 | SN74ABT541BDWR | |
| | SSOP – DB | Reel of 2000 | SN74ABT541BDBR | AB541B |
| | | | SN74ABT541BDBRG4 | |
| | TSSOP – PW | Reel of 1050 | SN74ABT541BPW | AB541B |
| | | Reel of 2000 | SN74ABT541BPWR | |
| –55°C to 125°C | CDIP – J | Reel of 1000 | SNJ54ABT541J | SNJ54ABT541J |
| | CFP – W | Reel of 510 | SNJ54ABT541W | SNJ54ABT541W |
| | LCCC – FK | Reel of 2200 | SNJ54ABT541FK | SNJ54ABT541FK |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

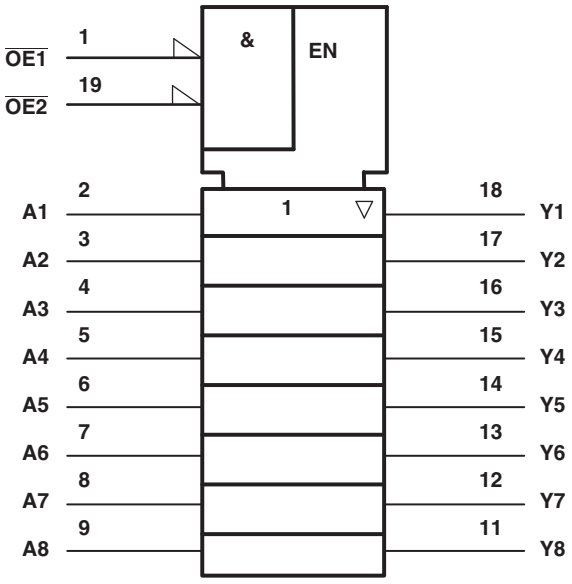
When VCC is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT541B is characterized for operation from –40°C to 85°C.

### FUNCTION TABLE

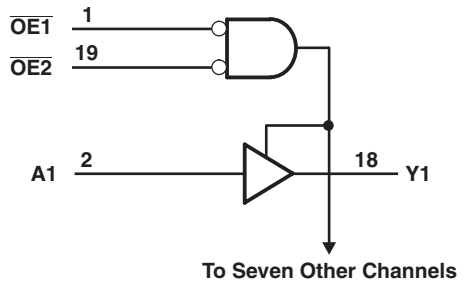
| INPUTS | | | OUTPUTS |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

### LOGIC SYMBOL(1)




(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### LOGIC DIAGRAM (POSITIVE LOGIC)



## Absolute Maximum Ratings(1)

over recommended operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high or power-off state | | –0.5 | 5.5 | V |
| $I_O$ | Current into any output in the low state | SN54ABT541 | | 96 | mA |
| | | SN74ABT541B | | 128 | |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –18 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $\theta_{JA}$ | Package thermal impedance(3) | DB package | | 115 | °C/W |
| | | DW package | | 97 | |
| | | N package | | 67 | |
| | | PW package | | 128 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## Recommended Operating Conditions(1)

over recommended operating free-air temperature range (unless otherwise noted)

| | | SN54ABT541 | | SN74ABT541B | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | | 0.8 | V |
| $I_{OH}$ | High-level output current | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 5 | | 5 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | | 200 | | µs/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $T_A$ = 25°C | | | SN54ABT51 | | SN74ABT541B | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP(1) | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | –1.2 | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC}$ = 5 V, | $I_{OH}$ = –3 mA | 3 | | | 3 | | 3 | | |
| | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –24 mA | 2 | | | 2 | | | | |
| | | $I_{OH}$ = –32 mA | 2(2) | | | | | 2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | | 0.55 | | 0.55 | | | VV |
| | | $I_{OL}$ = 64 mA | | | 0.55(2) | | | | 0.55 | |
| $V_{hys}$ | | | | 100 | | | | | | mV |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | µA |
| $I_{OZPU}$ | $V_{CC}$ = 0 to 2.1 V, $V_O$ = 0.5 V to 2.7 V, $\overline{OE}$ = X | | | | ±50(3) | | ±50(3) | | ±50 | µA |
| $I_{OZPD}$ | $V_{CC}$ = 2.1 V to 0, $V_O$ = 0.5 V to 2.7 V, $\overline{OE}$ = X | | | | ±50(3) | | ±50(3) | | ±50 | µA |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 10 | | 10 | | 10 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | | –10 | | –10 | | –10 | µA |
| $I_{off}$ | $V_{CC}$ = 0 V, | $V_I$ or $V_O$≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | $V_{CC}$ = 5.5 V, $V_O$ = 5.5 V, | Outputs high | | | 50 | | | | 50 | µA |
| $I_O$ | $V_{CC}$ = 5.5 V(4), | $V_O$ = 2.5 V | –50 | –140 | –180 | –50 | –180 | –50 | –180 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V, $I_O$ = 0 V, $V_I$ = $V_{CC}$ or GND | Outputs high | | 5 | 250 | | 250 | | 250 | µA |
| | | Outputs low | | 22 | 30 | | 30 | | 30 | mA |
| | | Outputs disabled | | 1 | 250 | | 250 | | 250 | µA |
| $\Delta I_{CC}$ | $V_{CC}$ = 5.5 V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND(5) | Outputs enabled | | | 1.5 | | 1.5 | | 1.5 | mA |
| | | Outputs disabled | | | 50 | | 50 | | 50 | µA |
| | | Control Inputs | | | 1.5 | | 1.2 | | 1.5 | mA |
| $C_i$ | $V_I$ = 2.5 V or 0.5 V | | | 3 | | | | | | pF |
| $C_o$ | $V_O$ = 2.5 V or 0.5 V | | | 6 | | | | | | pF |

(1) All typical values are at $V_{CC}$ = 5 V.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(4) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
(5) This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## Switching Characteristics, SN54ABT541

over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | VCC = 5 V, TA = 25°C | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1 | 2.6 | 4.1 | 1 | 4.6 | ns |
| $t_{PHL}$ | | | 1 | 2.9 | 4.2 | 1 | 4.7 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 1.1 | 3.1 | 4.8 | 1.1 | 5.4 | ns |
| $t_{PZL}$ | | | 2.1 | 4.4 | 5.9 | 2.1 | 7 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 2.1 | 5.1 | 6.6 | 2.1 | 7.5 | ns |
| $t_{PLZ}$ | | | 1.7 | 4.7 | 6.2 | 1.7 | 6.7 | |

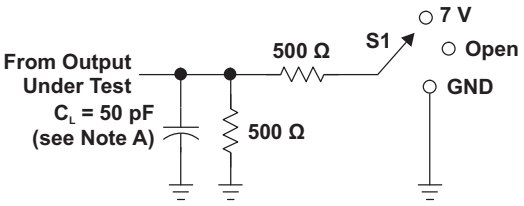
## Switching Characteristics, SN74ABT541B

over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | VCC = 5 V, TA = 25°C | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1 | 2 | 3.2 | 1 | 3.9 | ns |
| $t_{PHL}$ | | | 1 | 2.6 | 3.5 | 1 | 3.9 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 2 | 3.5 | 4.5 | 2 | 4 | ns |
| $t_{PZL}$ | | | 1.9 | 4 | 5.1 | 1.9 | 5.9 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 2.2 | 4.4 | 5.4 | 2.2 | 5.8 | ns |
| $t_{PLZ}$ | | | 1.5 | 3 | 4 | 1.5 | 4.4 | |
| $t_{sk(o)}$ (1) | | | | | 0.5 | | 0.5 | ns |

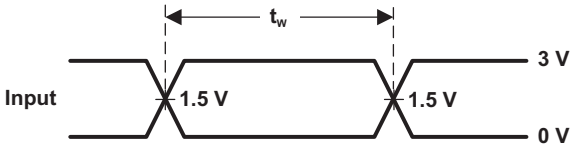
(1) Skew between any two outputs of the same package switching in the same direction.

## PARAMETER MEASURMENT INFORMATION

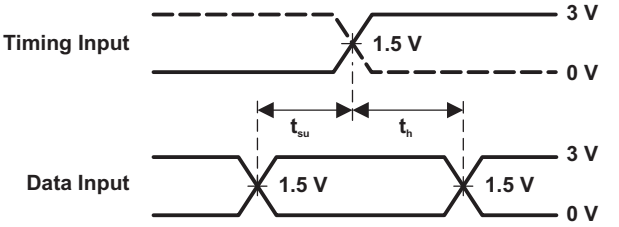



LOAD CIRCUIT

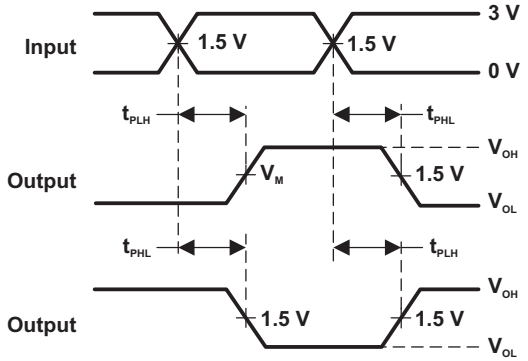
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |



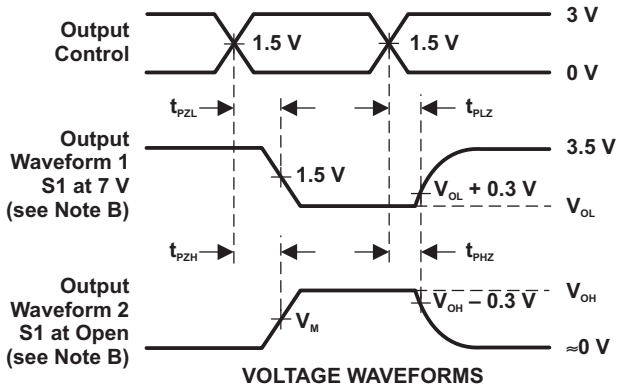

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_o$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 5962-9471801Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9471801QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-9471801QSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74ABT541BDBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74ABT541BDBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BDWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT541BNE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT541BNSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BNSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BNSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BPWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BPWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BPWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI |
| SN74ABT541BPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BPWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT541BPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54ABT541FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ABT541J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54ABT541W | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type |

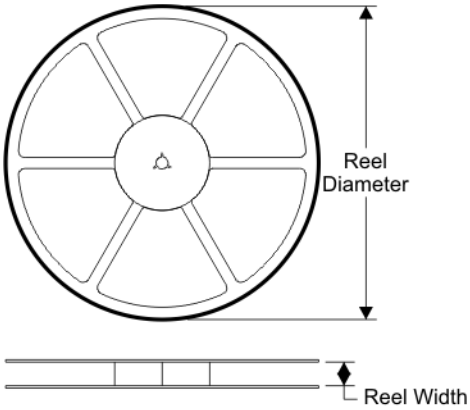
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

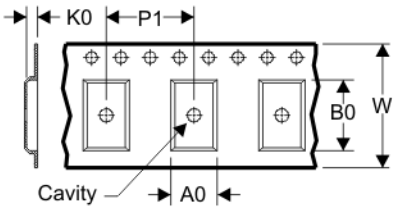
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL BOX INFORMATION

**REEL DIMENSIONS**

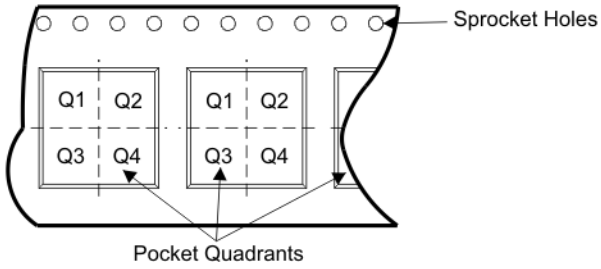



**TAPE DIMENSIONS**



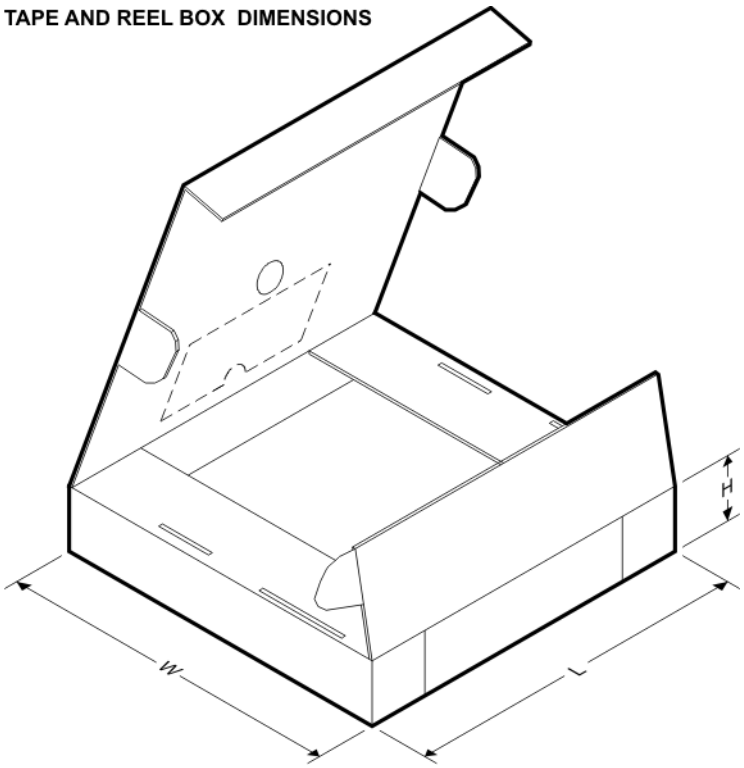

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ABT541BDBR | DB | 20 | SITE 41 | 330 | 16 | 8.2 | 7.5 | 2.5 | 12 | 16 | Q1 |
| SN74ABT541BDWR | DW | 20 | SITE 41 | 330 | 24 | 10.8 | 13.0 | 2.7 | 12 | 24 | Q1 |
| SN74ABT541BPWR | PW | 20 | SITE 41 | 330 | 16 | 6.95 | 7.1 | 1.6 | 8 | 16 | Q1 |

TAPE AND REEL BOX DIMENSIONS

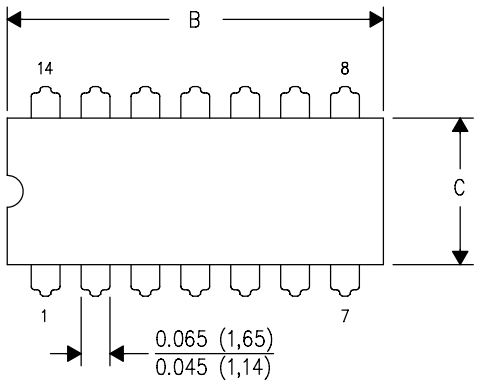



| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| SN74ABT541BDBR | DB | 20 | SITE 41 | 346.0 | 346.0 | 33.0 |
| SN74ABT541BDWR | DW | 20 | SITE 41 | 346.0 | 346.0 | 41.0 |
| SN74ABT541BPWR | PW | 20 | SITE 41 | 346.0 | 346.0 | 33.0 |

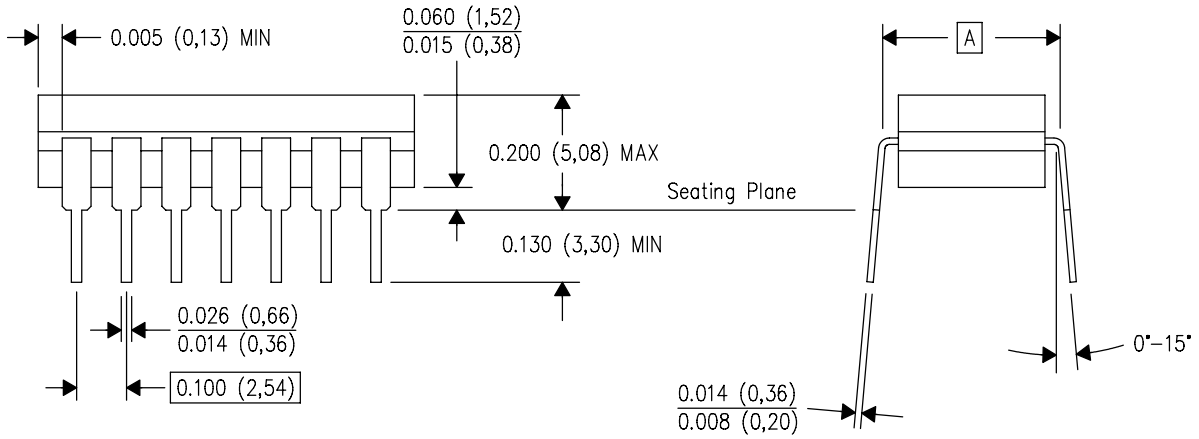
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



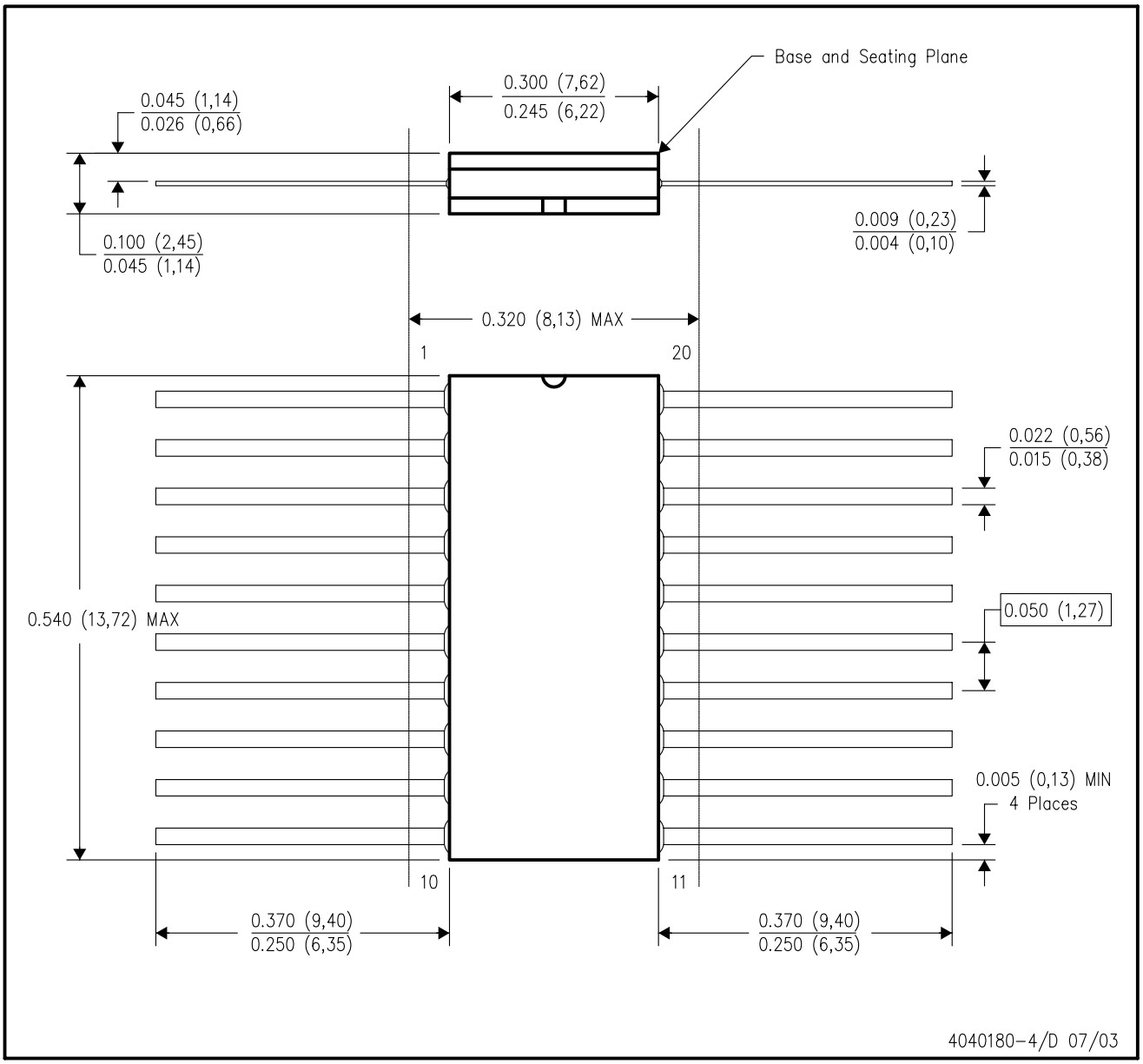

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

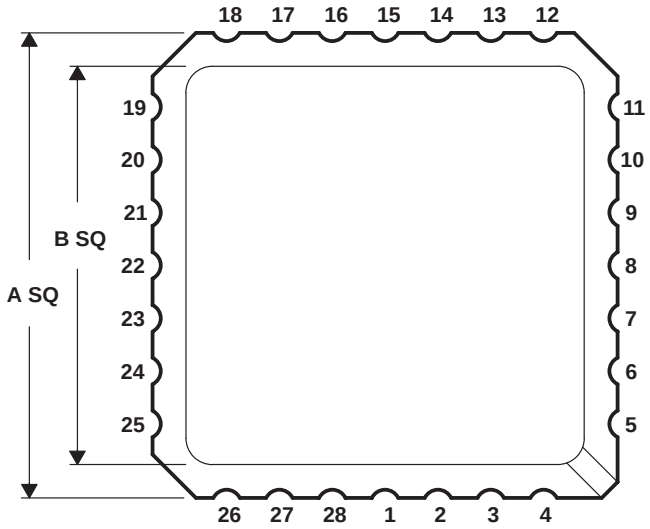
## W (R–GDFP–F20) CERAMIC DUAL FLATPACK



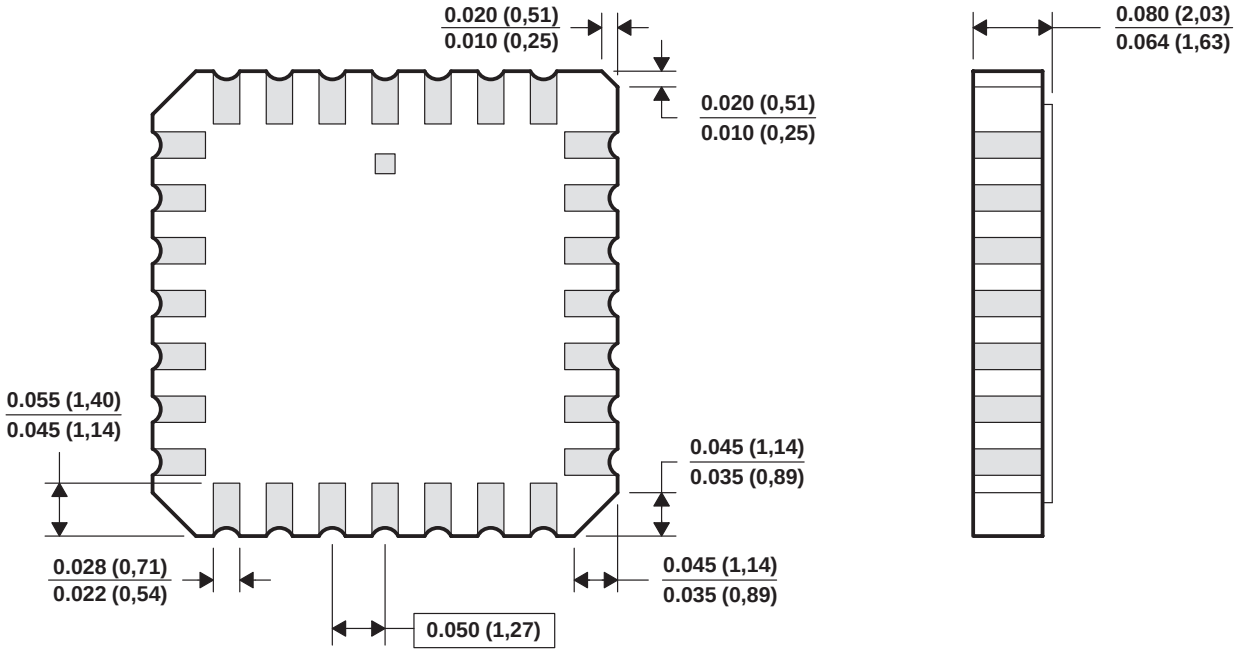

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



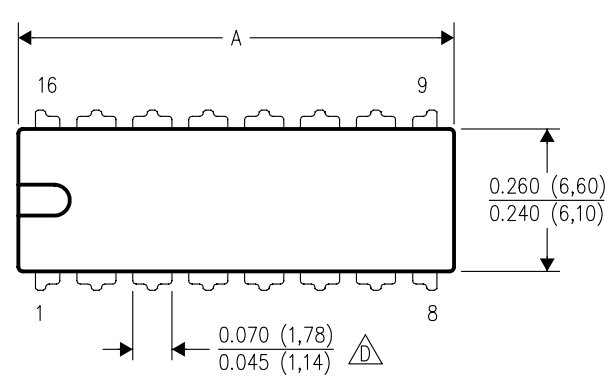

**4040140/D 10/96**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

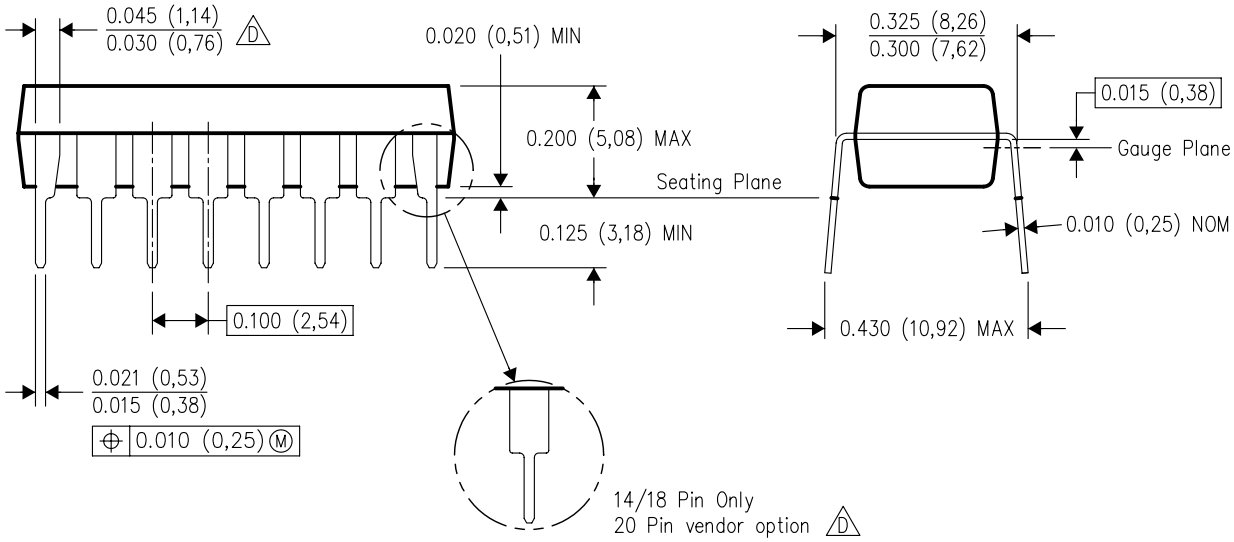
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



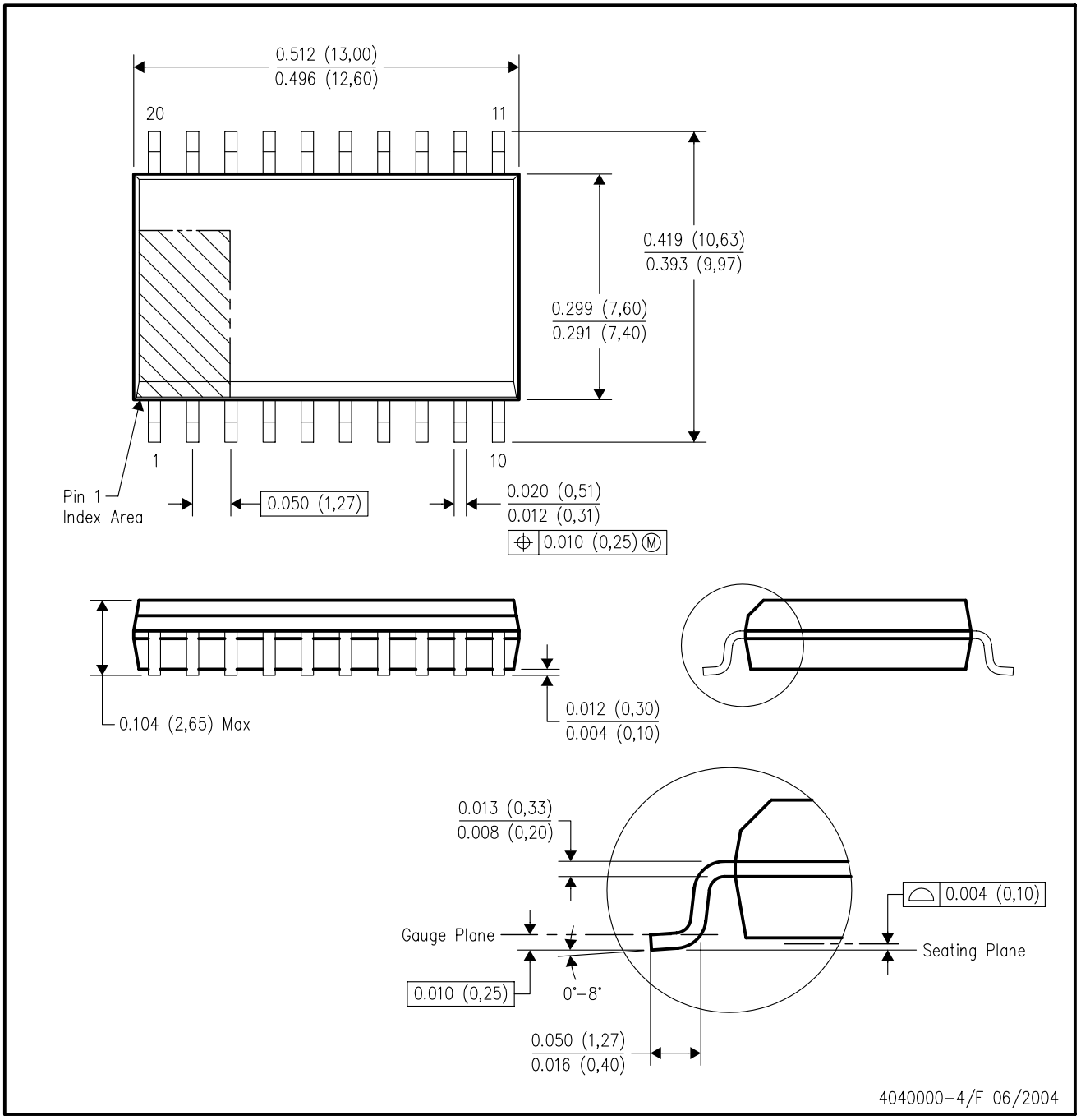

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

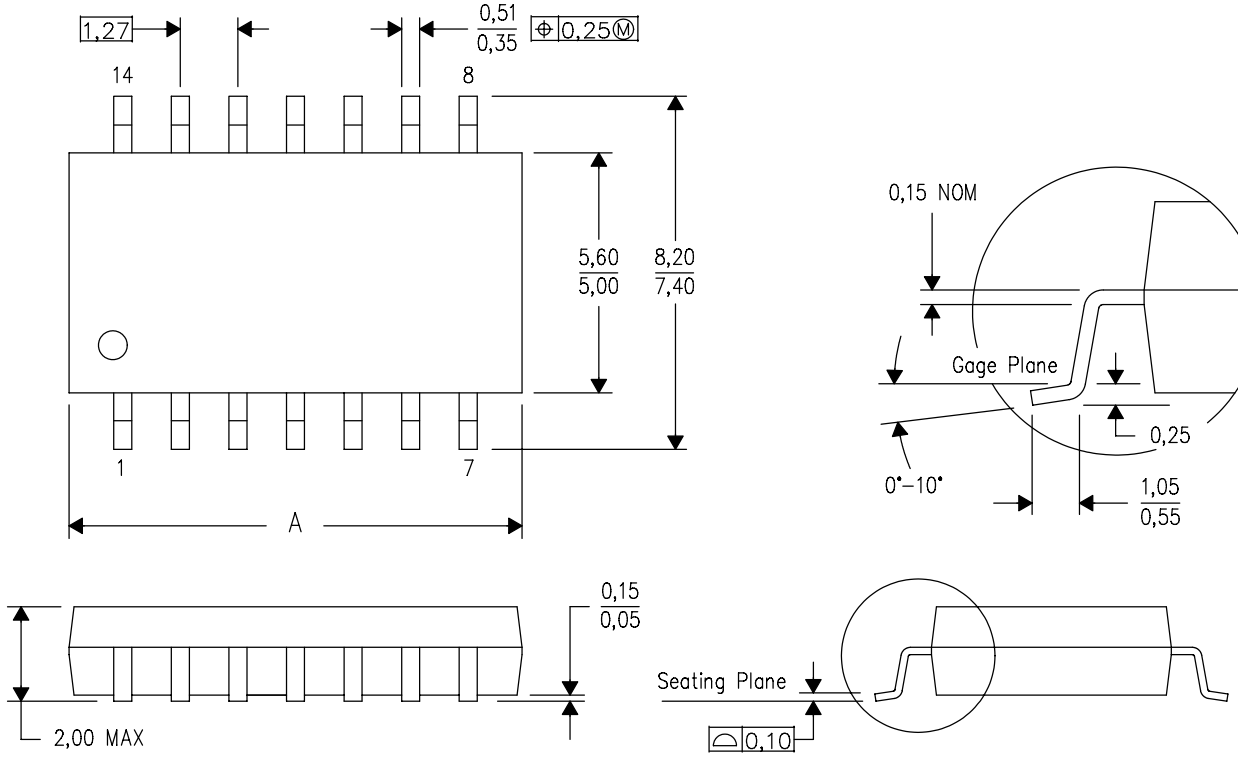



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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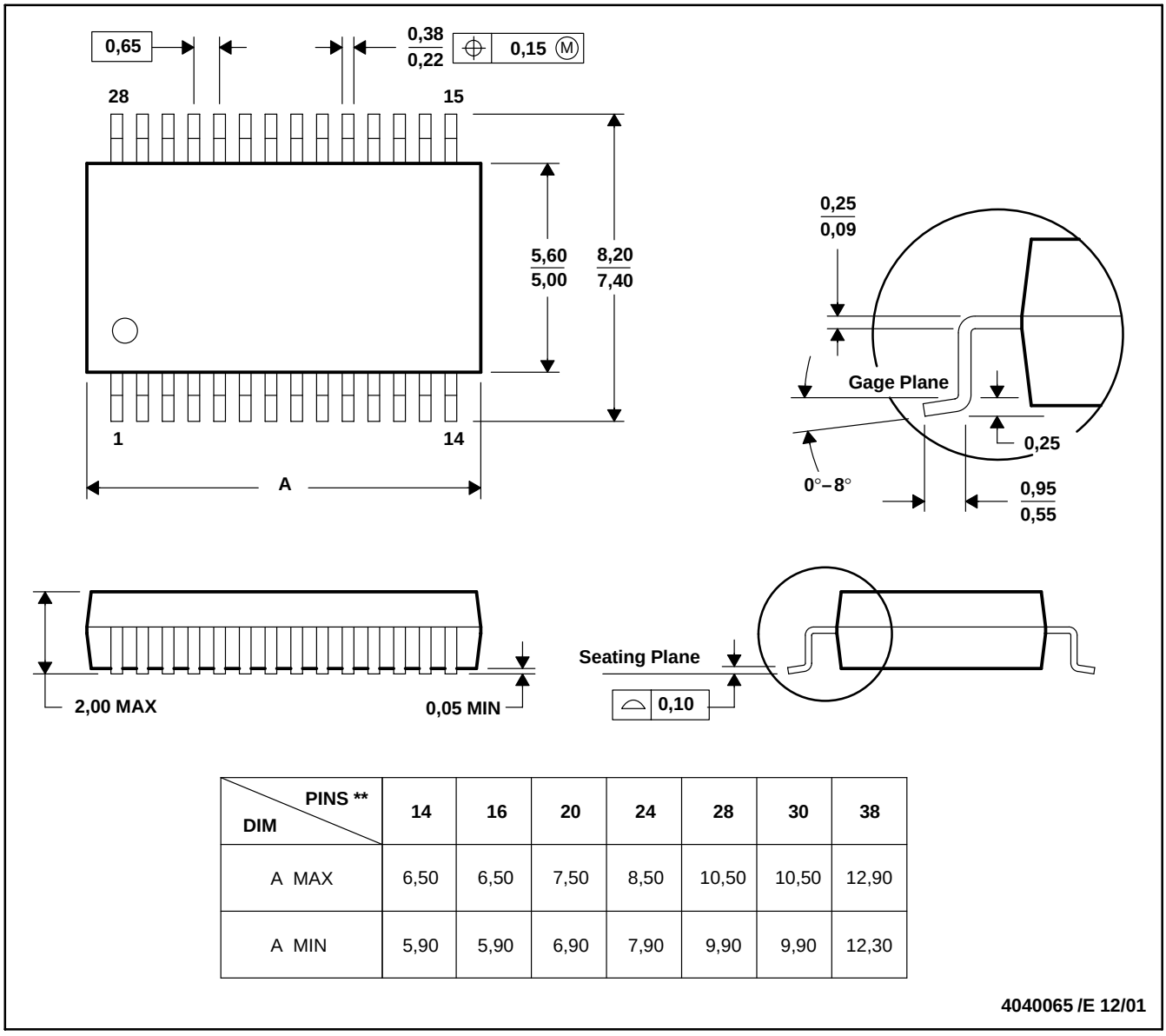
**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



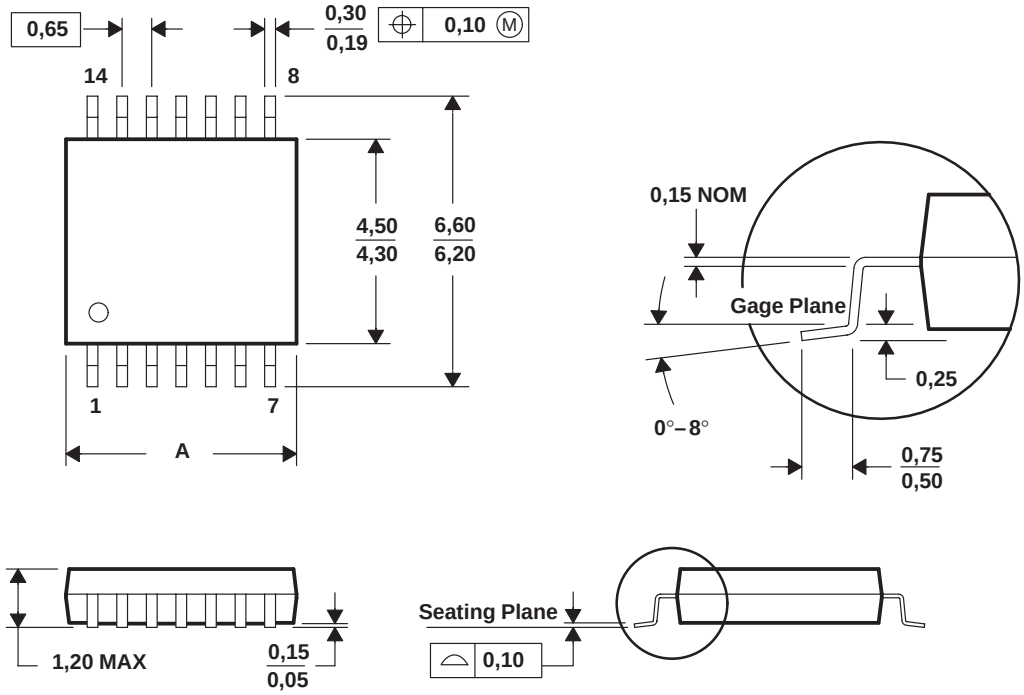

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153