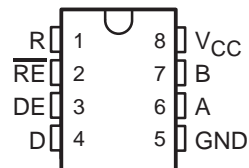


- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27
- Recommended for PROFIBUS Applications
- Operates at Data Rates up to 35 MBaud
- Operating Temperature Range . . .  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirement . . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design
- Package Options Include Plastic Small-Outline (D) Package and (P) DIPs

**D† OR P PACKAGE  
(TOP VIEW)**



† The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN65ALS1176DR).

## description

The SN65ALS1176 differential bus transceiver is designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS1176 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS1176 is characterized for operation from  $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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## Function Tables

### DRIVERS

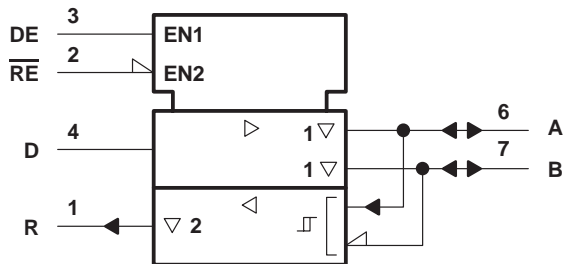
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

### RECEIVER

DIFFERENTIAL INPUTS A-B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Inputs open	L	H

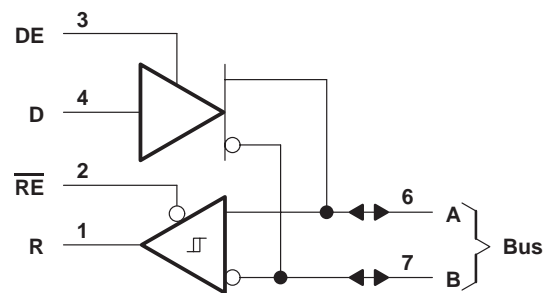
H = high level, L = low level, X = irrelevant,  
? = Indeterminate, Z = high impedance (off)

### logic symbol†

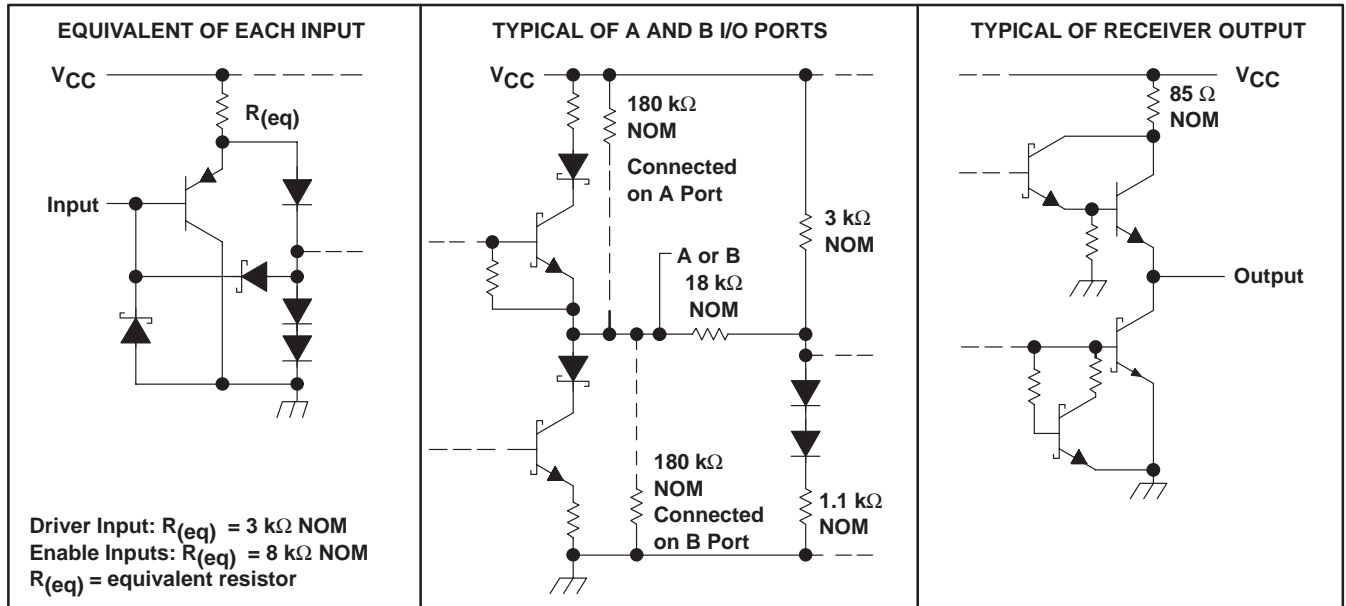


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	-7 V to 12 V
Enable input voltage, $V_I$	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	97°C/W
P package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$				12	V
				-7	
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $V_{ID}$ (see Note 3)				±12	V
High-level output current, $I_{OH}$	Driver			-60	mA
	Receiver			-400	μA
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	
Operating free-air temperature, $T_A$		-25		85	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

# SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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## DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION†	MIN	TYP‡	MAX	UNIT
V <sub>IK</sub> Input clamp voltage	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>O</sub> Output voltage	I <sub>O</sub> = 0	0		6	V
V <sub>OD1</sub>   Differential output voltage	I <sub>O</sub> = 0	1.5		6	V
V <sub>OD2</sub>   Differential output voltage	R <sub>L</sub> = 100 Ω, See Figure 1	1/2V <sub>OD1</sub> or 2§			V
	R <sub>L</sub> = 54 Ω, See Figure 1	2.1	2.5	5	V
V <sub>OD3</sub> Differential output voltage	V <sub>test</sub> = -7 V to 12 V, See Figure 2	1.5		5	V
Δ V <sub>OD</sub>   Change in magnitude of differential output voltage¶				±0.2	V
V <sub>OC</sub> Common-mode output voltage	R <sub>L</sub> = 54 Ω or 100 Ω, See Figure 1			3 -1	V
Δ V <sub>OC</sub>   Change in magnitude of common-mode output voltage¶				±0.2	V
I <sub>O</sub> Output current	Outputs disabled, See Note 4	V <sub>O</sub> = 12 V		1	mA
		V <sub>O</sub> = -7 V		-0.8	
I <sub>IH</sub> High-level input current	V <sub>I</sub> = 2.4 V			20	μA
I <sub>IL</sub> Low-level input current	V <sub>I</sub> = 0.4 V			-400	μA
I <sub>OS</sub> Short-circuit output current#	V <sub>O</sub> = -4 V			-250	mA
	V <sub>O</sub> = 0			-150	
	V <sub>O</sub> = V <sub>CC</sub>			250	
	V <sub>O</sub> = 8 V			250	
I <sub>CC</sub> Supply current	No load	Outputs enabled	23	30	mA
		Outputs disabled	19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

§ The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.

¶ Δ|V<sub>OD</sub>| and Δ|V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from one logic state to the other.

# Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.



**switching characteristics over recommended ranges of supply voltage and operating free-air temperature range**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_d(\text{OD})$	Differential output delay time	$R_L = 54 \Omega$ , See Figure 3	$C_L = 50 \text{ pF}$ ,			15	ns
$t_{sk(p)}$	Pulse skew‡				0	2	ns
$t_t(\text{OD})$	Differential output transition time				8		ns
$t_{PZH}$	Output enable time to high level	$R_L = 110 \Omega$ , See Figure 4	$C_L = 50 \text{ pF}$ ,			80	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110 \Omega$ , See Figure 5	$C_L = 50 \text{ pF}$ ,			30	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110 \Omega$ , See Figure 4	$C_L = 50 \text{ pF}$ ,			50	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110 \Omega$ , See Figure 5	$C_L = 50 \text{ pF}$ ,			30	ns

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Pulse skew is defined as the  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.

**SYMBOL EQUIVALENTS**

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$V_O$	$V_{Oa}, V_{Ob}$	$V_{Oa}, V_{Ob}$
$ V_{OD1} $	$V_O$	$V_O$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	None	$V_t$ (test termination measurement 2)
$\Delta  V_{OD} $	$  V_t  -  \bar{V}_t  $	$  V_t  -  \bar{V}_t  $
$V_{OC}$	$ V_{os} $	$ V_{os} $
$\Delta  V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
$I_{OS}$	$ I_{sa} ,  I_{sb} $	None
$I_O$	$ I_{xa} ,  I_{xb} $	$I_{ia}, I_{ib}$

# SN65ALS1176

## DIFFERENTIAL BUS TRANSCEIVER

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### RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = 2.7 V, I <sub>O</sub> = -0.4 mA			0.2	V
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.5 V, I <sub>O</sub> = 8 mA	-0.2‡			V
V <sub>hys</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )			60		mV
V <sub>IK</sub>	Enable-input clamp voltage	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV, See Figure 6 I <sub>OH</sub> = -400 μA,		2.7		V
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -200 mV, See Figure 6 I <sub>OL</sub> = 8 mA,			0.45	V
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V			±20	μA
V <sub>I</sub>	Line input current	Other input = 0 V, See Note 5			1	mA
					-0.8	
I <sub>IH</sub>	High-level-enable input current	V <sub>IH</sub> = 2.7 V			20	μA
I <sub>IL</sub>	Low-level-enable input current	V <sub>IL</sub> = 0.4 V			-100	μA
r <sub>I</sub>	Input resistance		12	20		kΩ
I <sub>OS</sub>	Short-circuit output current	V <sub>ID</sub> = 200 mV, V <sub>O</sub> = 0	-15		-85	mA
I <sub>CC</sub>	Supply current	No load		23	30	mA
				19	26	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>pd</sub>	Propagation time	V <sub>ID</sub> = -1.5 V to 1.5 V, C <sub>L</sub> = 15 pF, See Figure 7			25	ns
t <sub>sk(p)</sub>	Pulse skew§			0	2	ns
t <sub>pZH</sub>	Output enable time to high level	C <sub>L</sub> = 15 pF, See Figure 8		11	18	ns
t <sub>pZL</sub>	Output enable time to low level			11	18	ns
t <sub>PHZ</sub>	Output disable time from high level				50	ns
t <sub>PLZ</sub>	Output disable time from low level				30	ns

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Pulse skew is defined as the |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.



PARAMETER MEASUREMENT INFORMATION

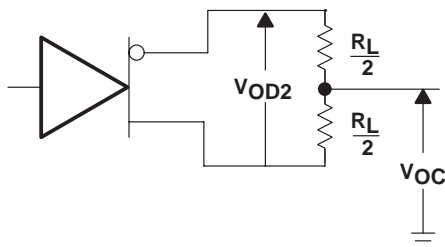


Figure 1. Driver  $V_{OD2}$  and  $V_{OC}$  Test Circuit

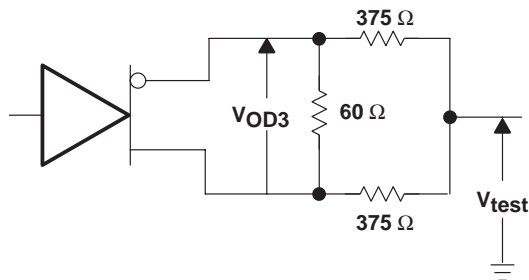
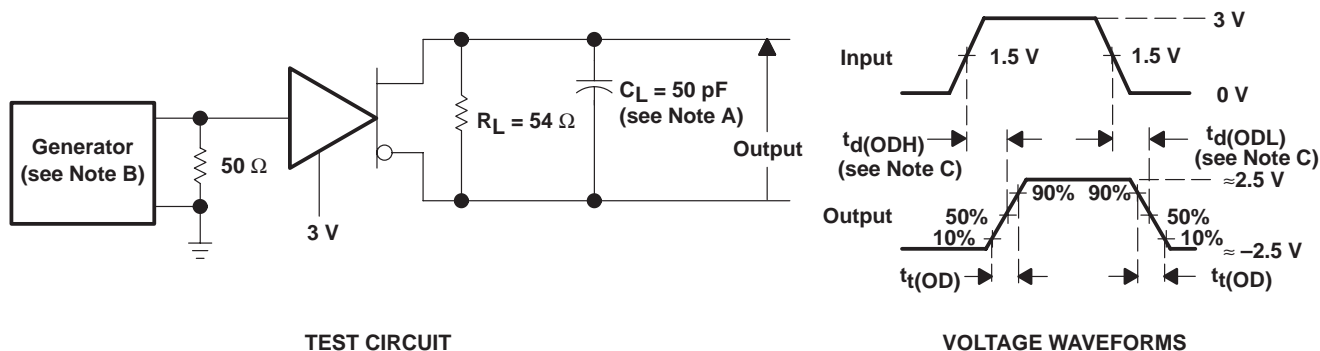


Figure 2. Driver  $V_{OD3}$  Test Circuit



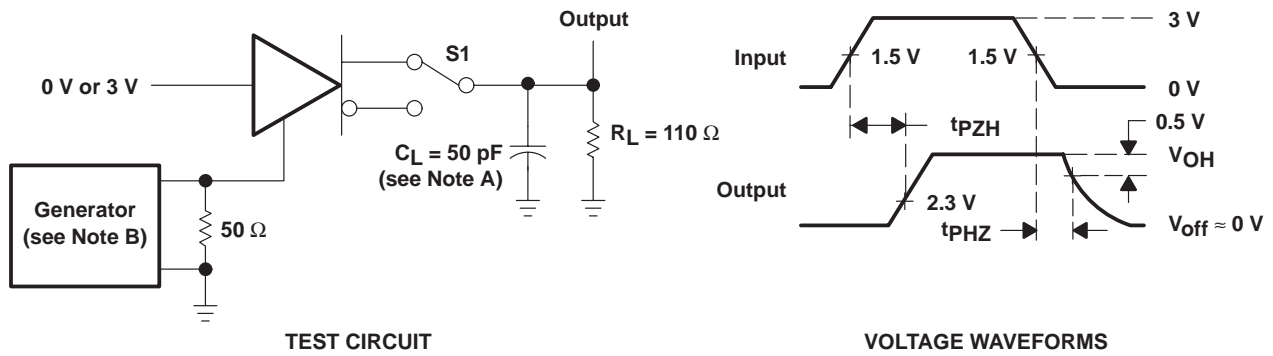
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 C.  $t_d(OD) = t_d(ODH)$  or  $t_d(ODL)$

Figure 3. Driver Differential-Output Delay and Transition Times

# SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

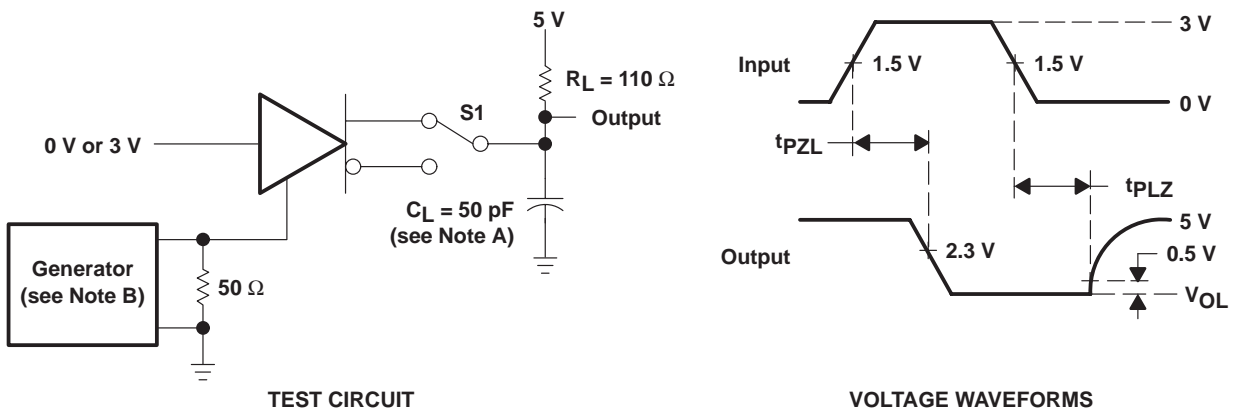
SLLS295A – APRIL 1998 – REVISED DECEMBER 1999

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

Figure 4. Driver Enable and Disable Times



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .

Figure 5. Driver Enable and Disable Times



PARAMETER MEASUREMENT INFORMATION

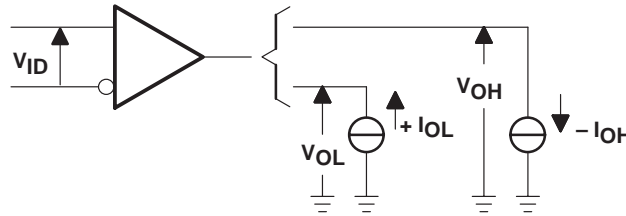
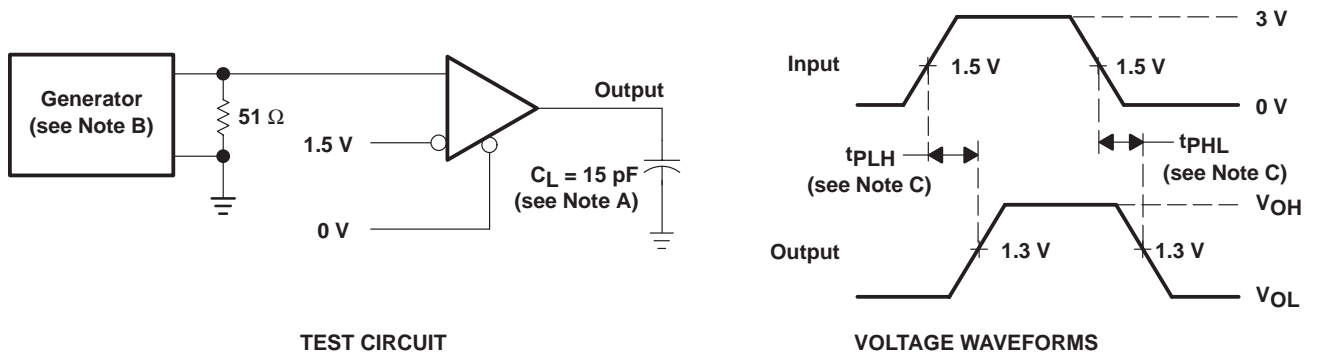


Figure 6. Receiver  $V_{OH}$  and  $V_{OL}$  Test Circuit



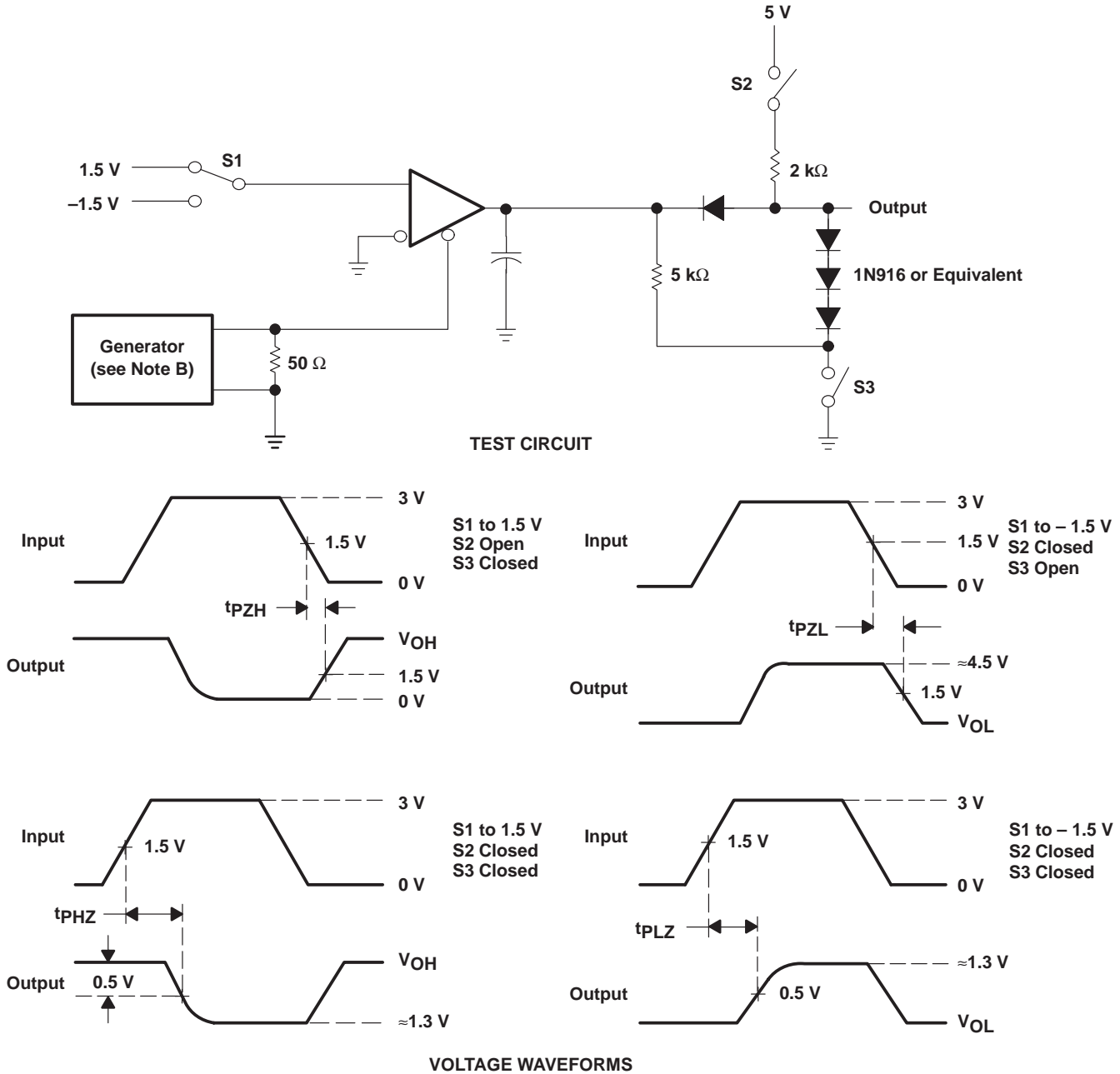
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 C.  $t_{pd} = t_{PLH}$  or  $t_{PHL}$

Figure 7. Receiver Propagation-Delay Times

# SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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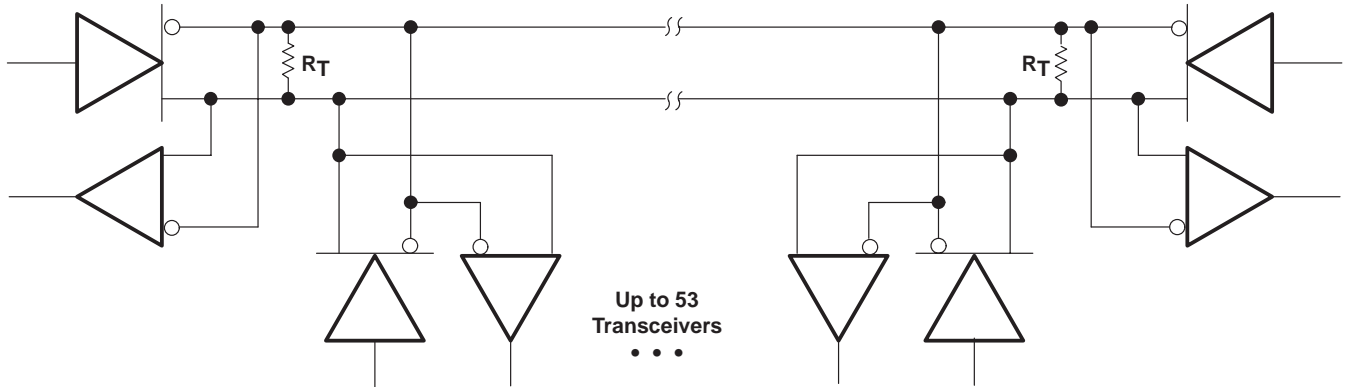
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .

Figure 8. Receiver Output Enable and Disable Times

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 9. Typical Application Circuit

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN65ALS1176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN65ALS1176DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN65ALS1176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
SN65ALS1176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN65ALS1176DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN65ALS1176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

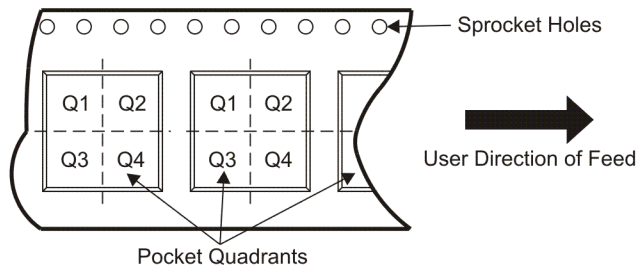
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS1176DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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