

Low Jitter and Power Clock Generator with SSCG

| Key Features | Description |
|--|---|
| <ul style="list-style-type: none"> • Low power dissipation <ul style="list-style-type: none"> - 13.5mA-typ CL=15pF - 18.0mA-max CL=15pF • 3.3V +/-10% power supply range • 27.000MHz crystal or clock input • 27.000MHz REFCLK • 100MHz SSCLK with SSEL0/1 spread options • Low CCJ Jitter • Low LT Jitter • Internal Voltage Regulators • 45% to 55% Output Duty Cycle • On-chip Crystal Oscillator • -10 to +85 Temperature Range • 10-pin 3x3x0.75 mm TDFN package | <p>The SL16010DC is a low power dissipation spread spectrum clock generator using SLI proprietary low jitter PLL. The SL16010DC provides two output clocks. REFCLK (Pin-9) which is a buffered output of the 27.000MHz input crystal and SSCLK (Pin-5) which is synthesized as 100.000MHz nominal by an internal PLL using the 27.00MHz external input crystal or clock.</p> <p>In addition, SSEL0 (Pin-7) and SSEL1 (Pin-3) spread percent selection control inputs enable users to select from 0.0% (no spread) to -3.0% down spread at 100.000MHz SSCLK output to reduce and optimize system EMI levels.</p> <p>The SL16010DC operates in an extended temperature range of -10 to +85°C.</p> |
| <p>Application</p> <ul style="list-style-type: none"> • Video Cards • NB and DT PCs • HDTV and DVD-RW • Routers, Switches and Servers • Data Communications • Embedded Digital Applications | <p>Contact SLI for other programmable frequencies, Spread Spectrum Clock (SSC) options, as well as 2.5V+/-10 and 1.8V+/-5% power supply options.</p> <p>Benefits</p> <ul style="list-style-type: none"> • EMI Reduction • Improved Jitter • Low Power Dissipation • Eliminates external Xtals or XOs |

Block Diagram

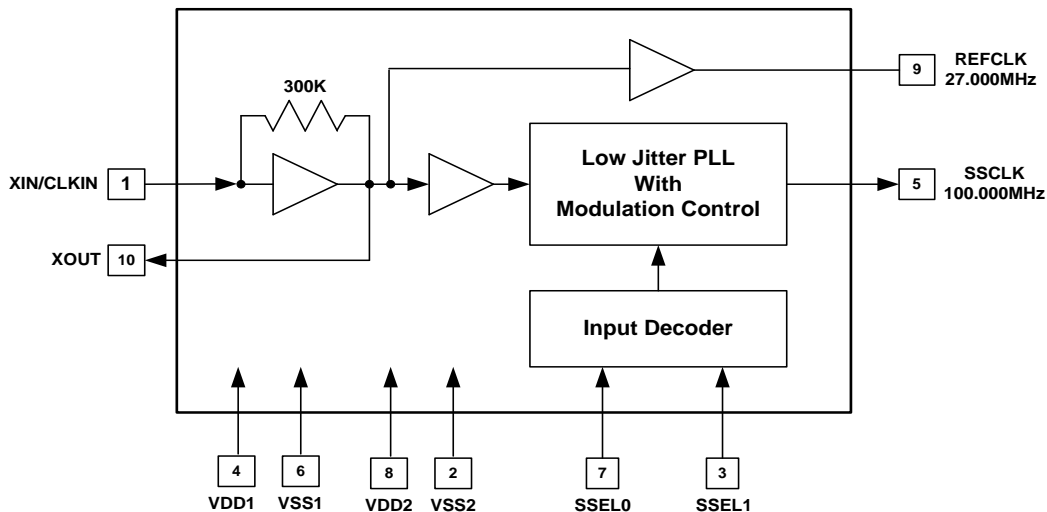


Figure 1. Block Diagram

Pin Configuration

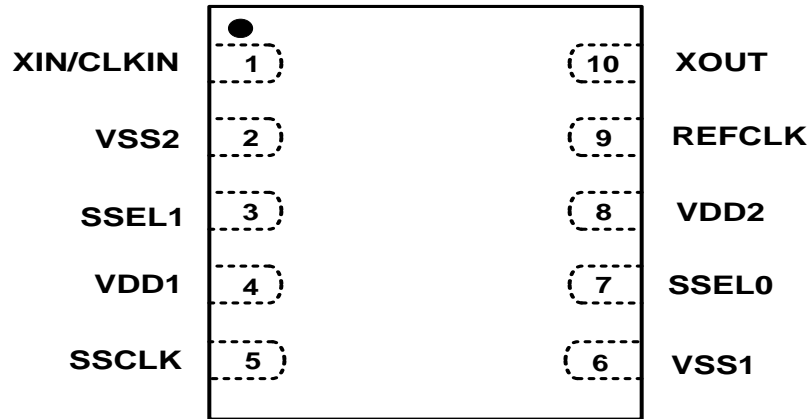


Figure 2. 10-Pin TDFN (3x3x0.75 mm)

Table 1. Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|-----------|----------|---|
| 1 | XIN/CLKIN | Input | External crystal or clock input. Capacitance at this pin is 4 pF-typ. |
| 2 | VSS2 | Power | Power supply ground for 27.000MHz REFCLK output. |
| 3 | SSEL1 | Input | SSEL1 spread percent selection pin. Refer to Table 5 for available spread options using SSEL1 pin. Three state, Low (L), Middle (M) and High (H) digital input logic levels. This pin has 150kΩ-typ input pull down resistor. |
| 4 | VDD1 | Power | Positive power supply for 100.000MHz SSCLK output. 3.3V +/-10%. |
| 5 | SSCLK | Output | SSCLK clock output. 100.000MHz nominal. Refer to Table 5 for available spread % options by using SSEL0 and SSEL1 control pins. |
| 6 | VSS1 | Power | Power supply ground for 100.000MHz SSCLK output. |
| 7 | SSEL0 | Input | SSEL spread percent selection pin. Refer to Table 5 for available spread options using SSEL0 pin. Three state, Low (L), Middle (M) and High (H) digital input logic levels. This pin has 150kΩ-typ input pull down resistor. |
| 8 | VDD2 | Power | Positive power supply for 27.000MHz REFCLK output. 3.3V +/-10%. |
| 9 | REFCLK | Output | REFCLK clock output. 27.000MHz nominal. |
| 10 | XOUT | Output | Crystal output. Capacitance at this pin 4 pF-typ. If clock input is used, leave this pin not connected (N/C). |

Table 2. Absolute Maximum Ratings

| Description | Condition | Min | Max | Unit |
|----------------------------------|--------------------------------|--------|---------|------|
| Supply voltage, VDD | | -0.5 | 4.2 | V |
| All Inputs and Outputs | | -0.5 | VDD+0.5 | V |
| Ambient Operating Temperature | In operation, extended C grade | -10 | 85 | °C |
| Storage Temperature | No power is applied | -65 | 150 | °C |
| Junction Temperature | In operation, power is applied | - | 125 | °C |
| Soldering Temperature | | - | 260 | °C |
| ESD Rating (Human Body Model) | JEDEC22-A114D | -4,000 | 4,000 | V |
| ESD Rating (Charge Device Model) | JEDEC22-C101C | -1,500 | 1,500 | V |
| ESD Rating (Machine Model) | JEDEC22-A115D | -200 | 200 | V |

Table 3. DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -10 to +85Deg C

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------|--------|--|---------|------|--------|------|
| Operating Voltage | VDD1/2 | VDD1=VDD2=3.3V +/-10% | 2.97 | 3.3 | 3.63 | V |
| Input Low Voltage | VINL | SSEL0 and SSEL1 | 0 | - | 0.2 | V |
| Input Middle Voltage | VINM | SSEL0 and SSEL1 | 0.4VDD | - | 0.6VDD | |
| Input High Voltage | VINH | SSEL0 and SSEL1 | 0.9VDD | - | VDD | V |
| Input High Voltage | VINH1 | CMOS Level, Pin-1 If input is clock | 0.7VDD | - | VDD | V |
| Input Low Voltage | VINL1 | CMOS Level, Pin-1 If input is clock | 0 | - | 0.3VDD | V |
| Output Low Voltage | VOL | IOL=15mA, Pins 5 and 9 | - | - | 0.4 | V |
| Output High Voltage | VOH | IOH=-15mA , Pins 5 and 9 | VDD-0.4 | - | - | V |
| Power Supply Current | IDD | SSEL=1, M or 0, CL=15pF, VDD=3.63V and T=85°C | - | 13.5 | 18.0 | mA |
| Input Capacitance | CIN1 | XIN and XOUT, Pins 1 and 10 | - | 4 | - | pF |
| Input Capacitance | CIN2 | SSEL0/1, Pins 7 and 3 | - | 3 | 5 | pF |
| Load Capacitance | CL | SSCLK and REFCLK, Pins 5 and 9 | - | - | 15 | pF |
| Pull Down Resistor | RPD | | 100 | 150 | 250 | kΩ |

Table 4. AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD= 3.3V+/-10%, CL=15pF and Ambient Temperature range -10 to +85 Deg C

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------------|--------|--|-----|--------|-----|------|
| Frequency Range | FR-1 | Input crystal or clock range, +/-10 ppm crystal accuracy if a crystal is used | - | 27.000 | - | MHz |

| | | | | | | |
|-------------------------------------|--------|--|-----|---------|-------|------|
| Frequency Range | FR-2 | REFCLK, Pin 9 | - | 27.000 | - | MHz |
| Frequency Range | FR-3 | SSCLK, Pin 5 | - | 100.000 | - | MHz |
| Frequency Accuracy | FACC1 | REFCLK, Pin 9 | -30 | +/-0 | 30 | ppm |
| Frequency Accuracy | FACC2 | SSCLK, Pin 5, SSEL0/1=0 | -30 | +/-0 | 30 | ppm |
| Rise and Fall Time | TR/F-1 | REFCLK, Pin 9, CL=5pF, measured from 20% to 80% of VDD | - | 1.0 | 1.5 | ns |
| Rise and Fall Time | TR/F-2 | REFCLK, Pin 9, CL=15pF, measured from 20% to 80% of VDD | - | 1.5 | 2.0 | ns |
| Rise and Fall Time | TR/F-3 | SSCLK, Pin 5, CL=5pF, measured from 20% to 80% of VDD | - | 0.75 | 1.0 | ns |
| Rise and Fall Time | TR/F-4 | SSCLK, Pin 5, CL=15pF, measured from 20% to 80% of VDD | - | 1.5 | 1.75 | ns |
| Output Duty Cycle | DC | SSCLK and REFCLK, Pins 5 and 9, measured at VDD/2, CL=15pF | 45 | 50 | 55 | % |
| Cycle-to-Cycle Jitter | CCJ | SSCLK/REFCLK, Pins 5 and 9 | - | 125 | 200 | ps |
| Long Term Jitter | LTJ | REFCLK, Pins 9, 10,000 cycles | - | 130 | 300 | ps |
| Power-up Time (VDD) | tPU1 | Time from 0.9VDD to valid frequency at output Pins 5 and 9 | - | 2.0 | 5.0 | ms |
| Spread Percent Change Settling Time | tSS% | Time from SSEL0/1 change to stable SSCLK with spread % | - | - | 1.0 | ms |
| Modulation Frequency | MF | SSCLK, 100MHz nominal, Pin 5 | 31 | 32 | 33 | kHz |
| Modulation Type and Slew Rate | FMTSR | SSCLK, Pin 5, Triangular Modulation Profile | - | - | 0.125 | %/μs |

Table 5. SSEL1 and SSEL0 versus Spread % Selection at SSCLK

| SSEL1 (Pin 3) | SSEL0 (Pin 7) | Spread Percent (%) SSCLK (Pin 5) |
|----------------|----------------|-------------------------------------|
| Low (VSS) | Low (VSS) | Spread Off (No Spread) |
| Low (VSS) | Middle (VDD/2) | -0.50% |
| Low (VSS) | High (VDD) | -2.5% |
| Middle (VDD/2) | Low (VSS) | -0.25% |
| Middle (VDD/2) | Middle (VDD/2) | -0.75% |
| Middle (VDD/2) | High (VDD) | -1.0% |
| High (VDD) | Low (VSS) | -1.5% |
| High (VDD) | Middle (VDD/2) | -2.0% |
| High (VDD) | High (VDD) | -3.0% |

Note: Middle (VDD/2) state requires 5kΩ/5kΩ external resistors as shown in Figure 3, page 5.

Table 6. Recommended Crystal Specifications

| Description | Min | Typ | Max | Unit |
|---|-----|--------|-----|----------|
| Nominal Frequency (Fundamental Crystal) | - | 27.000 | - | MHz |
| Crystal Accuracy | - | +/-10 | - | ppm |
| Load Capacitance | 8 | 12 | 18 | pF |
| Shunt Capacitance | - | - | 7.0 | pF |
| Equivalent Series Resistance (ESR) | - | - | 30 | Ω |
| Drive Level | - | - | 1.0 | mW |

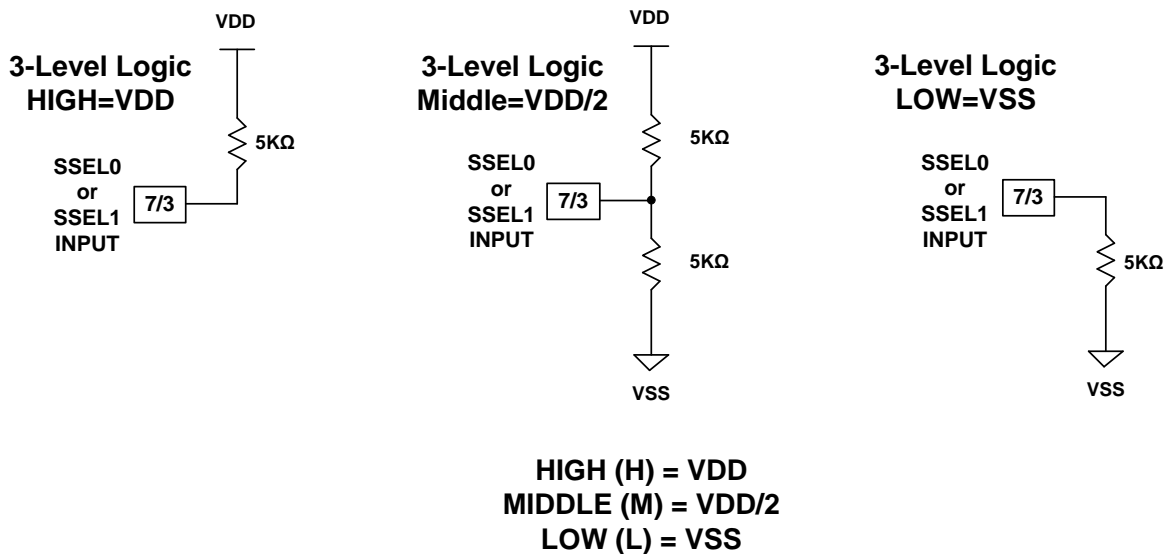


Figure 3. FSEL0 and FSEL1 Spread % Selection Logic

Note: SSEL0 and SSEL1 pins use 3-Level L(LOW) = VSS, M(MIDDLE)=VDD/2 and H(HIGH) = VDD 3-Level logic to provide 9 spread % values at SSCLK (pin 5) as given in Table 5. Use 5k Ω /5k Ω external resistor divider at SSEL0 and SSEL1 pins from VDD to VSS to obtain VDD/2 for M=VDD/2 Logic level as shown above in Figure 3.

External Components and Design Considerations

Typical Application Circuit

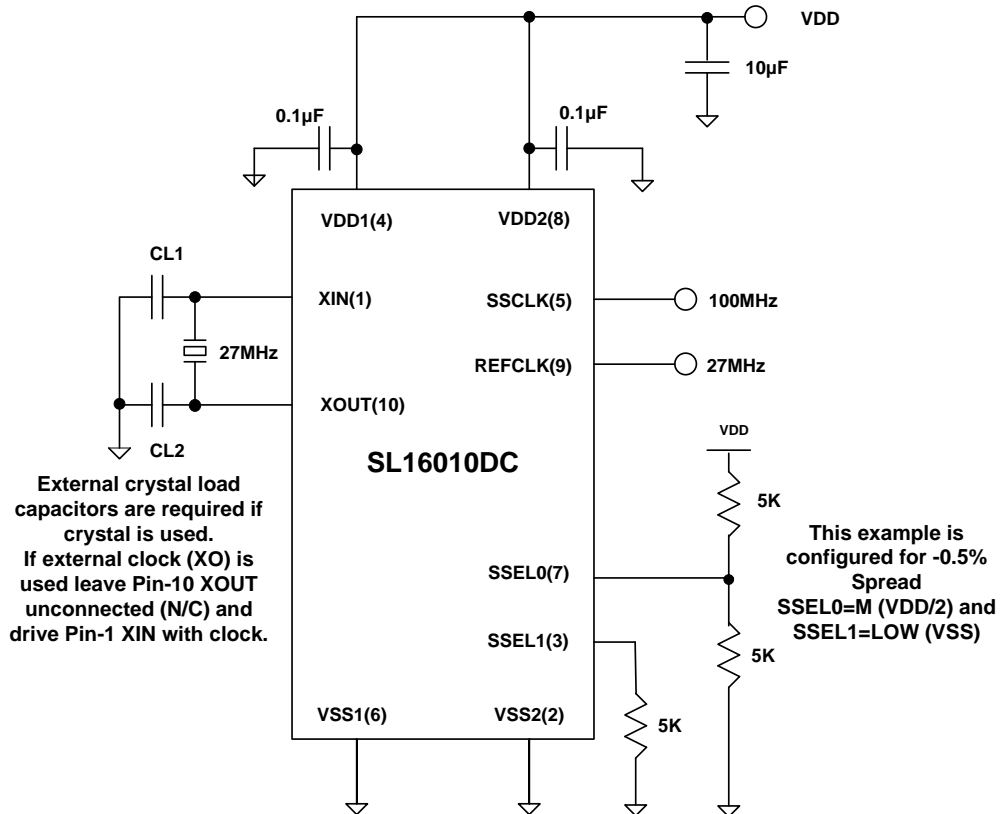


Figure 4. Typical Application Schematic

Comments and Recommendations

Crystal and Crystal Load: Only use a parallel resonant fundamental AT cut crystal. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm) make sure that external crystal load capacitor is matched to crystal load specification. To determine the value of CL1 and CL2, use the following formula;

$$C1 = C2 = 2CL - (Cpin + Cp)$$

Where: CL is load capacitance stated by crystal manufacturer

Cpin is the SL16010 pin capacitance (4pF)

Cp is the parasitic capacitance of the PCB traces.

EXAMPLE; if a crystal with CL=12pF specification is used and Cp=1pF (parasitic PCB capacitance on PCB), 19 or 20pF external capacitors from pins XIN (pin-1) and XOUT (Pin-10) to VSS are required since CXIN=CXOUT=4pF for the SL16010DC product. Users must verify Cp value.

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD1/2 pins and VSS1/2 pin. Place the capacitor on the component side of the PCB as close to the VDD1/2 pins as possible. The PCB trace to the VDD1/2 pins and to the VSS via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD1/2 pins. In addition, a 10uf capacitor should be placed between VDD and VSS.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (REFCLK and SSCLK) and the load if PCB trace is over 1 ½ inch. The nominal impedance of the outputs is about 24 Ω. Use 22 Ω resistors in series with the outputs to terminate 50Ω trace impedance and place 22 Ω resistors as close to the clock outputs as possible.

Package Outline and Package Dimensions
10-Pin TDFN Package (3x3x0.75 mm)

Dimensions are in mm

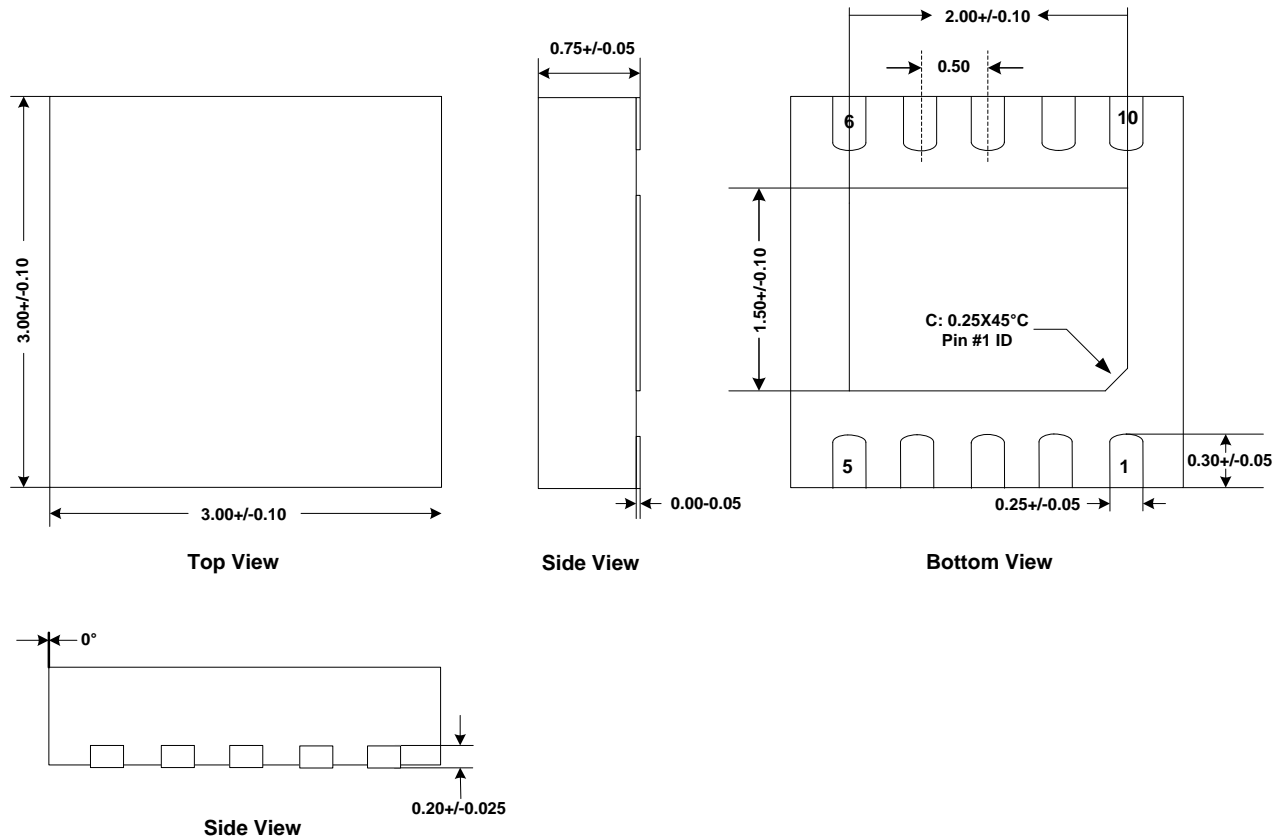


Table 7. Thermal Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|----------------|-------------------------|-----|-----|-----|--------------------|
| Thermal Resistance Junction to Ambient | θ_{JA1} | Still air | - | 75 | - | $^\circ\text{C/W}$ |
| | θ_{JA2} | 1m/s air flow | - | 70 | - | $^\circ\text{C/W}$ |
| | θ_{JA3} | 3m/s air flow | - | 55 | - | $^\circ\text{C/W}$ |
| Thermal Resistance Junction to Case | θ_{JC} | Independent of air flow | - | 25 | - | $^\circ\text{C/W}$ |

Table 8. Ordering Information

| Ordering Number | Marking | Shipping Package | Package | Temperature |
|-----------------|-----------|------------------|-------------|-------------|
| SL16010DC | SL16010DC | Tube | 10-pin TDFN | -10 to 85°C |
| SL16010DCT | SL16010DC | Tape and Reel | 10-pin TDFN | -10 to 85°C |

Note:

1. SL16010DC is RoHS compliant and Halogen Free.

Product Revisions History

| Revision | Date | Originator | Description |
|----------|------------|------------|--|
| Rev 0.5 | 12/12/2009 | C. Ozdalga | Original. |
| Rev 1.0 | 1/30/2009 | C. Ozdalga | Reduce IDD-max to 18 mA from 28 mA. Change C _{xin} /C _{xot} from 4 pF to 6 pF. Change R/R divider from 10Ω/10kΩ to 5kΩ/5kΩ. Add Pull-down resistors definition for SSEL0/1 pins on Pin Description Table. Improve Typical Application Circuit. Remove LTJ for SSCLK until new specification is obtained from customer. |
| Rev 1.0 | 2/23/2009 | C. Ozdalga | Change 13.5mA-max to 15mA-typ (Key Features – Page-1) |
| Rev 2.0 | 2/30/2009 | C. Ozdalga | Final production version revision number change to Rev 2.0. |
| Rev 2.1 | 4/14/2009 | C. Ozdalga | Correct Page 7 package pin number typing error. |
| Rev 2.2 | 4/22/2009 | C. Ozdalga | Page 3 CIN1, CXI/CXOUT pin capacitance changed to 4pF-typ from 6pF-typ. |
| Rev 2.3 | 9/1/2009 | C. Ozdalga | Replace “floating” with “VDD/2” in table 5 on page 4 and add note under the same table 5 for clarification. Redo Figure 3 to clarify 3-Level Logic and add 5KΩ resistor from SSEL1 to VSS in Figure 4 on page 6. Change Table 1 to Table 5 on pin description table page 2 for SSEL1 and SSEL0 rows. |
| Rev 2.4 | 9/3/2009 | C. Ozdalga | Replace “floating” with “VDD/2” in table 5 on page 4 under SSEL1. |
| Rev 2.5 | 6/4/2010 | C. Ozdalga | Add clock input specifications. SL16010DC can be driven by an external crystal or clock. |
| Rev 2.6 | 8/1/2010 | C. Ozdalga | Add Halogen Free, page 8. |

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