Si3404 Data Sheet

Fully-Integrated IEEE 802.3 Type 1-Compliant POE PD Interface and High-Efficiency Switching Regulator with Compact Footprint

The Si3404 integrates the power management and control functions required in a Power-over-Ethernet (PoE) powered device (PD) application. These devices convert the high voltage supplied over the 10/100/1000BASE-T Ethernet connection to a regulated, low-voltage output supply. The optimized architecture of this device minimizes the solution footprint and external BOM cost and enables the use of low-cost external components while maintaining high performance. The Si3404 integrates a transient surge suppressor. The switching power FET and associated functions are also integrated. The integrated, current mode controlled switching regulator supports isolated or non-isolated flyback and buck converter topologies. The switching frequency for the regulator is tunable with a simple external resistor value to help avoid unwanted harmonics for better emissions control.

This device fully supports the IEEE 802.3at specification for Type 1, single-event classification. Standard external resistors provide the proper IEEE 802.3 signatures for the detection function and programming of the classification mode, and internal startup circuits ensure well-controlled soft-start initial operation of both the hotswap switch and the voltage regulator.

The Si3404 is available in a low-profile, 20-pin, 4 x 4 mm QFN package.

KEY FEATURES

- Type 1 (PoE) power
- IEEE 802.3at Type 1 compliance
- Current mode dc-dc converter
- Tunable switching frequency
- Transformer bias winding support
- Auxiliary adapter capability
- Integrated hotswap FET and switching FET
- 120 V Absolute Max voltage performance
- Extended –40 to +85 °C temperature
- Compact ROHS-compliant 4 mm x 4 mm QFN Package

APPLICATIONS

- Voice over IP telephones
- Wireless access points
- Security and surveillance IP cameras
- Point-of-sale terminals
- Internet appliances
- Network devices

1. Ordering Guide

Table 1.1. Si3404 Ordering Guide

Ordering Part Number	Package	Temperature Range (Ambient)	Applications
Si3404-A-GM	4 x 4 mm 20-QFN Pb-free, RoHS-compliant	–40 to 85 °C Extended	All Purposes

Table of Contents

2. System Overview

The following Block Diagrams will give the designer a sense for the internal arrangement of functional blocks, plus their relationships to external pins. The Block Diagrams are followed by a description of the features of these integrated circuits.

2.1 Block Diagram

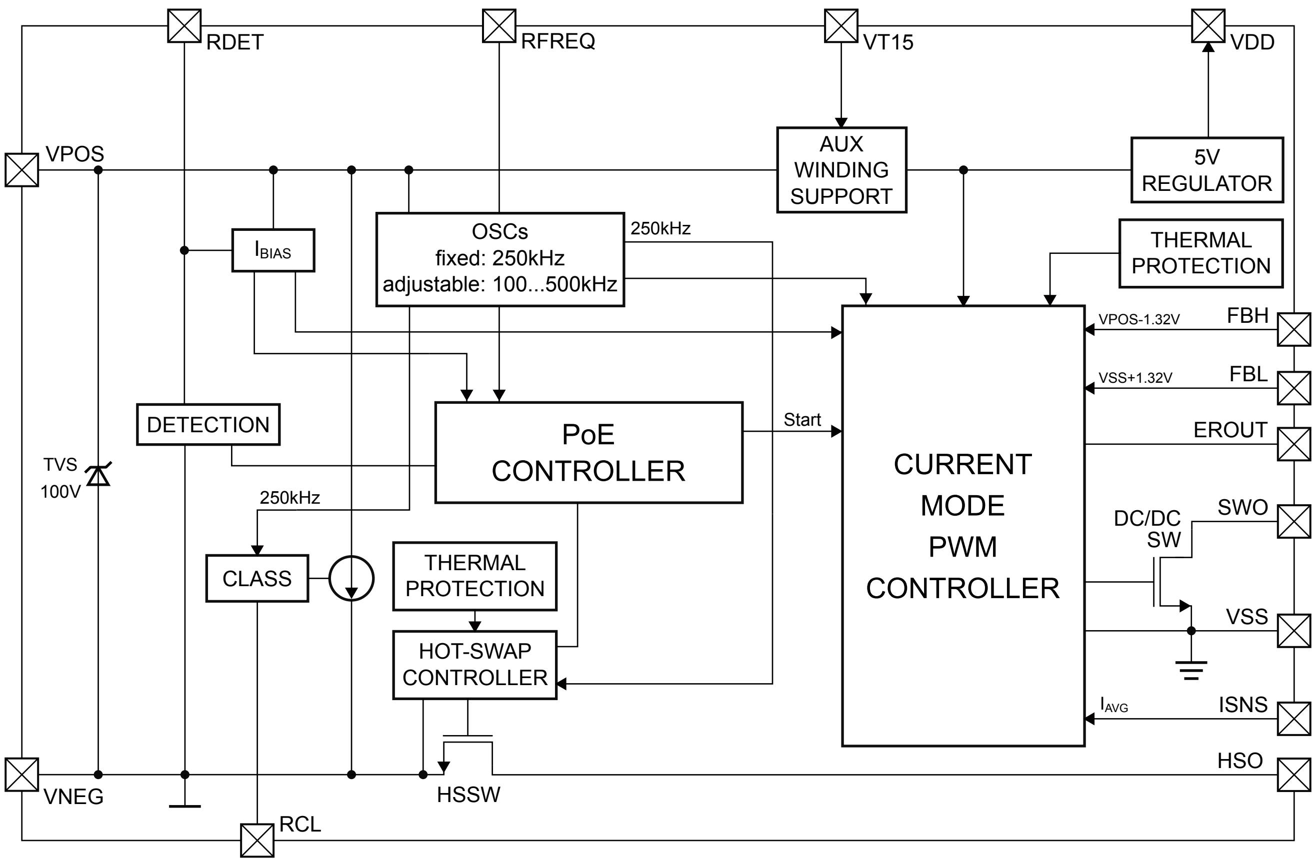


Figure 2.1. Si3404 Block Diagram

2.2 Power over Ethernet (PoE) Line-Side Interface

The PoE line interface consists of external diode bridges, internal surge protection, and protocol interface support for detection and classification.

The chip features active protection against surge transients and accidentally applied telephony voltages.

2.2.1 Surge Protection

The surge protection circuit is activated if the VPOS-VNEG voltage exceeds V_{PROT} *and* the hotswap switch is off (dc-dc is not powered). If the hotswap switch is on, the surge power is sunk in the dc-dc's input capacitance.

The internal surge protection can be overridden with an external TVS if higher than specified surge conditions need be tolerated. The external surge device must be connected in parallel to the internal one; therefore, the designer must ensure that the external surge protection will activate prior to the internal surge protection.

2.2.2 Telephony Protection

The Si3404 provides protection against telephony ringing voltage. The telephony ringing is much longer than the surge pulse but it has less energy, therefore, the Si3404 has a switch parallel with the supply (between VPOS and VNEG). When the protection circuit is activated, it turns ON the protection switch; the ringing energy then dissipates on this switch and ringing generator resistance (> 400 Ω).

2.2.3 Detection and Classification

When the Si3404 is connected via Ethernet cable to a PSE-enabled Ethernet switch, it has to provide a characteristic resistance (~25 kΩ) to the PSE in a given voltage range (2.7–10.1 V). This is called detection. After the PSE detects the PD, the PSE increases the voltage above the classification threshold 14.5 V. Then, the PD provides the classification current to inform the PSE about its required power class (Class 1, 2, 3, or 4). Type 1 PSEs cannot provide enough power for a Class 4 PD. Type 2 PSEs have additional voltage steps before switching on the PD. After an initial classification voltage pulse, the Type 2 PSE reduces the voltage below the mark threshold level (10 V) then raises it up again to the Class event range. Last, before switching ON the dc-dc, it reduces the voltage again.

The Si3404 is a Type 1 PD. The following figure represents the typical turning ON procedure of the PD, which includes detection, classification and PD turn ON.

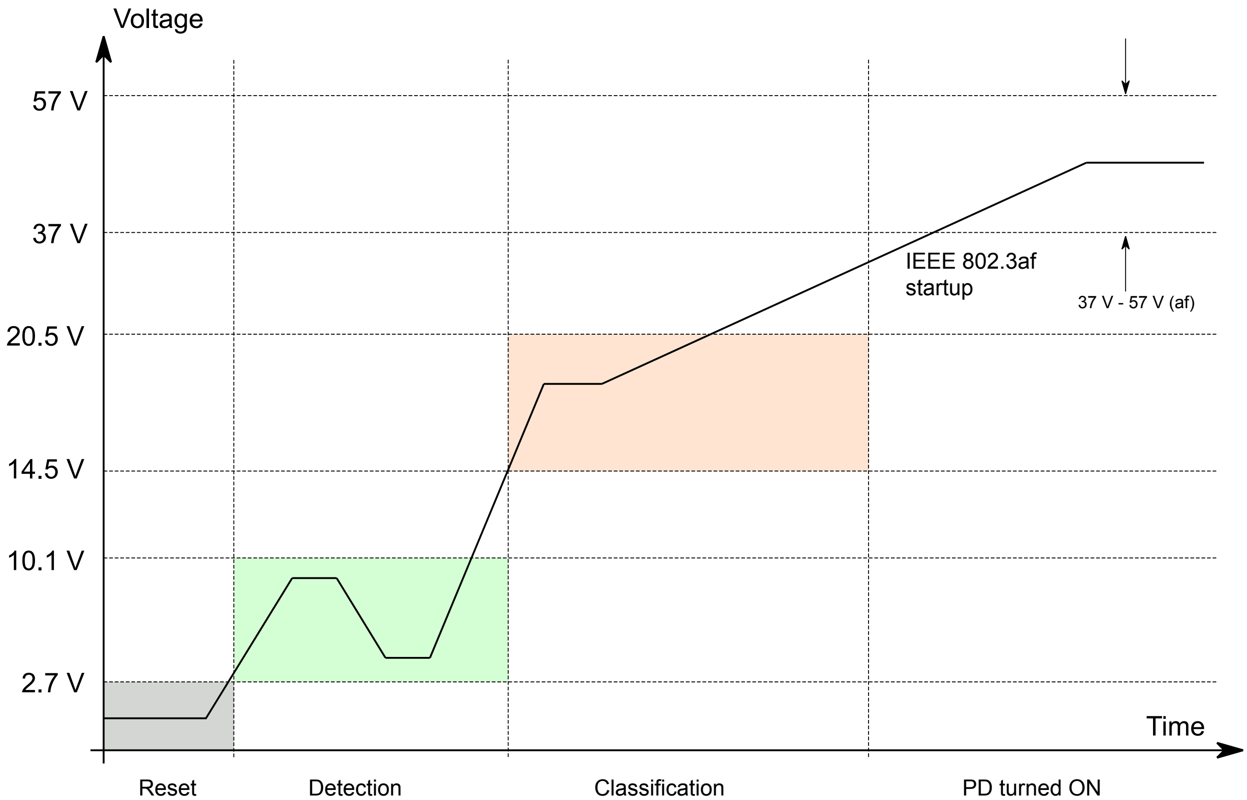


Figure 2.2. Powered Device Voltages

2.3 Hotswap Switch

The hotswap switch is a high voltage switch which separates the PoE inerface from the dc-dc converter domain. The internal hotswap switch (HSSW) is turned on (conducting) when the PoE interface voltage goes above V_{UVLO_R}. It provides limited inrush current until the dc-dc side capacitor is charged. The hotswap switch turns off (open) if voltage on the HSSW switch is greater than V_{HSSW_OFF}.

In overload, the hotswap switch goes into current-limiting mode with a current limit of I_{OVL}. It will turn back ON after $T_{WAITHSSW}$ elapses and the dc-dc input capacitor is recharged, meaning the HSO-VNEG voltage is less than V_{HSSW_ON}.

2.4 HSSW State Machine

The HSSW operates as simple 4-state state machine:

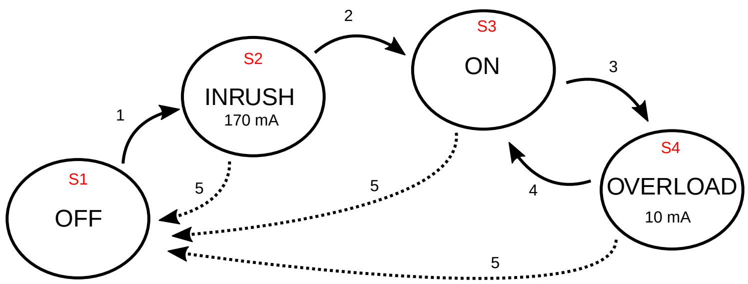


Figure 2.3. Hotswap Switch 4-State Machine

Transitions

1. UVLO released.
2. Input capacitor charged; PWM starts with Soft-Start protection.
3. Overcurrent detected; going to Overload state.
4. Overcurrent not present; going back to ON state.
5. Turning OFF the PD.

OFF State

HSSW turn-on is controlled by UVLO, the undervoltage lockout feature. When UVLO is engaged, the HSSW is OFF. In this state, the HSSW is in idle mode, VNEG and HSO pins are disconnected. In normal operation, a complete detect/classification procedure precedes the HSSW turn-on, and the control of this sequence is implemented in the state machine logic of the chip.

INRUSH State

After the controller enables the HSSW, the block starts operation in the INRUSH state. In this state the switch itself is not directly turned on, but operating in a closed-loop current limit mode to avoid high current peaks during the charging of the input capacitor of the dc-dc converter.

If the V_{HSSW} voltage drops below 380 mV (meaning the bypass cap is 99% charged), the HSSW will change state to ON.

ON State

In ON state, the HSSW switch is completely turned on. The HSSW circuit continuously monitors V_{HSSW}. HSSW will change to OVERLOAD state if V_{HSSW} voltage increases over 3.5 V.

OVERLOAD State

In OVERLOAD state the HSSW operates in closed-loop low current limit mode. If the V_{HSSW} voltage drops below 380 mV again, and the HSSW has been in the OVERLOAD state for at least $T_{WAITHSSW}$, the HSSW will change back to the ON state.

2.5 DC-DC Converter

The dc-dc converter is current-controlled for easier compensation and more robust protection of circuit magnetics. The controller has the following features:

- High- and low-side error amplifier (supports Buck and Flyback topologies).
- <1 Ω internal switching FET
- Overcurrent detection
- Cycle skipping at low current and short circuit conditions

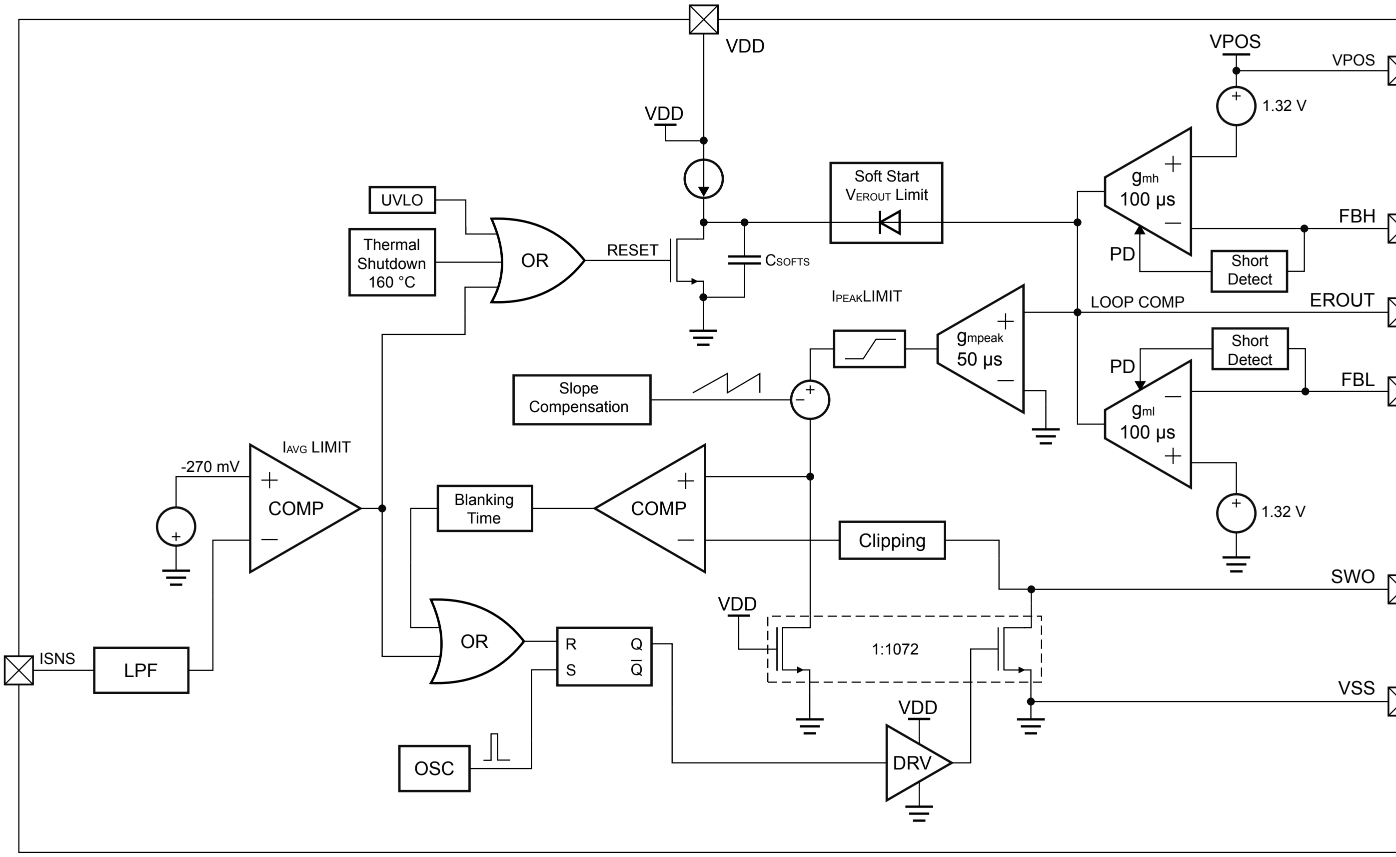


Figure 2.4. Si3404 DC-DC Converter Block Diagram

Feedback to the dc-dc converter can be provided in three ways:

- High side, referenced to VPOS, connected to FBH pin (Buck converter)
- Low side, referenced to VSS, connected to FBL pin (nonisolated Flyback)
- Directly to EROUT pin by a voltage to current converter (isolated Flyback)

The EROUT pin provides current output (if FBL or FBH is used) and voltage input. Also, the loop compensation impedance is connected to EROUT. The active voltage range is V_{EROUT}, which is proportional to the converter peak current.

The converter startup is not configurable; soft start is accomplished by internal circuitry. Soft start time is $T_{SOFTSTART}$. The intelligent soft start circuit dynamically adjusts the soft start time depending on the connected load.

2.5.1 Average Current Sensing, Overcurrent, Low-Current Detection, and Output Short Protection

The application average current is sensed by an external resistor (R_{SENSE}) connected between VSS and ISNS. Overcurrent is detected and triggered when the voltage on the sense resistor exceeds V_{ISNS_OVC}. Sizing the resistor allows the designer to set the overcurrent limit according to application needs. When overcurrent is triggered, the dc-dc controller goes into reset until the overcurrent resolves. When the overcurrent is no longer present, the controller starts up again with softstart.

The Si3404 integrates an output short protection. If the output is shorted for more than 1 ms, the controller will detect a high EROUT signal for more than 1 ms, which will reset the dc-dc controller. A new startup cycle with soft-start turn ON will follow.

2.6 Tunable Oscillator

The dc-dc frequency can be fixed to 250 kHz or tunable by an external resistor.

The tuning resistor must be connected between the R_{FREQ} pin and VPOS. If R_{FREQ} is shorted to VPOS, the fixed frequency oscillator will provide the clock, F_{OSCINT}, to the dc-dc converter; otherwise, the resistor will determine the frequency as shown in the curve below.

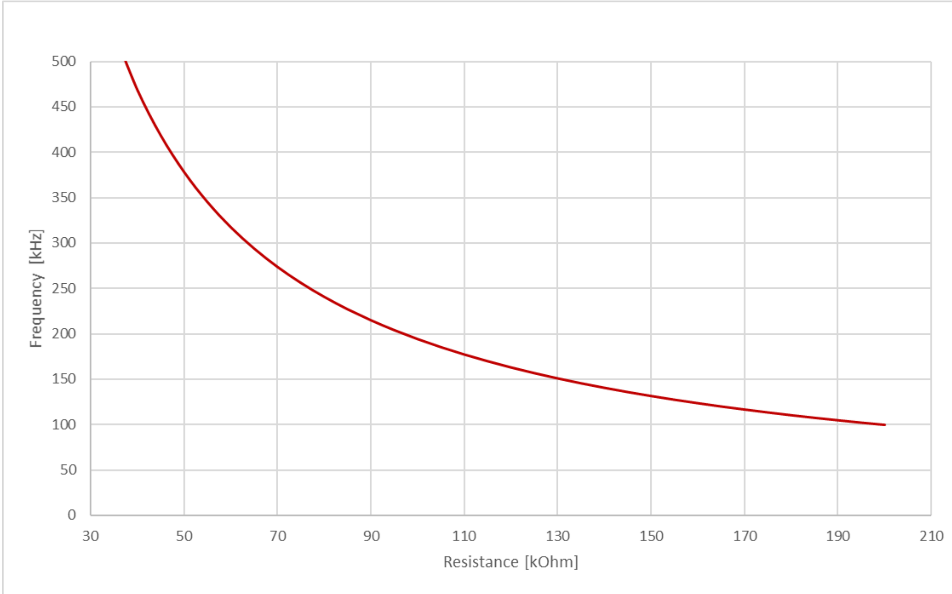


Figure 2.5. R_{FREQ} Frequency Selector Diagram

2.7 Regulators

The chip provides a 5 V output to power LEDs or optocouplers. This is a closed-loop regulator, which ensures accurate output voltage. The 5 V regulator is supplied by an internal 11 V open loop regulator. The 11 V regulator is supplied by a coarse regulator, which is also open-loop. With the Si3404, the VT15 pin can be used to supply this regulator from an optional auxiliary transformer bias winding. The advantage of doing so is additional power saving. The application must be designed to ensure that the absolute maximum rating voltage for the VT15 pin is not exceeded.

2.8 External Wall Adapter Support

The Si3404 allows the use of a range of external wall adapters as a primary or secondary supply. For details on adapter connection, please refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller In Isolated and Non-Isolated Designs".

3. Application Examples

The following diagrams demonstrate the ease of use and straightforward BOM of the Si3404 Powered Device IC. Detailed reference designs are available in Evaluation KIT User Guides. Also refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller In Isolated and Non-Isolated Designs".

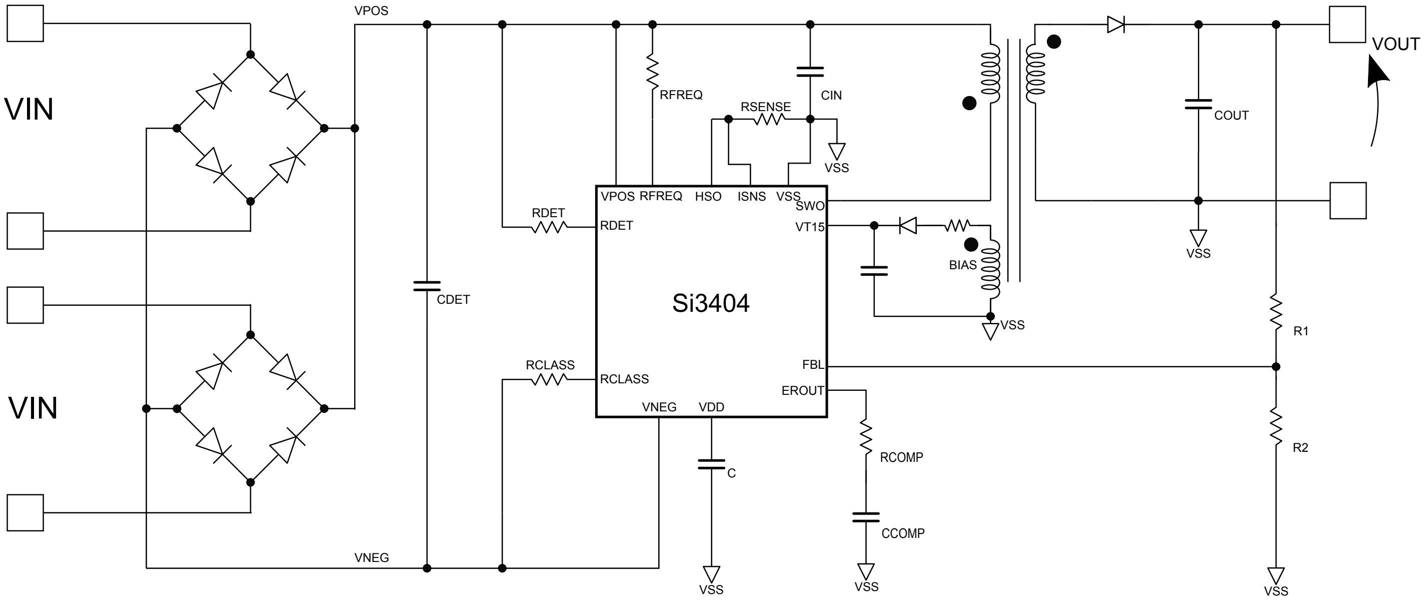


Figure 3.1. Si3404 Non-ISO Flyback Application Diagram

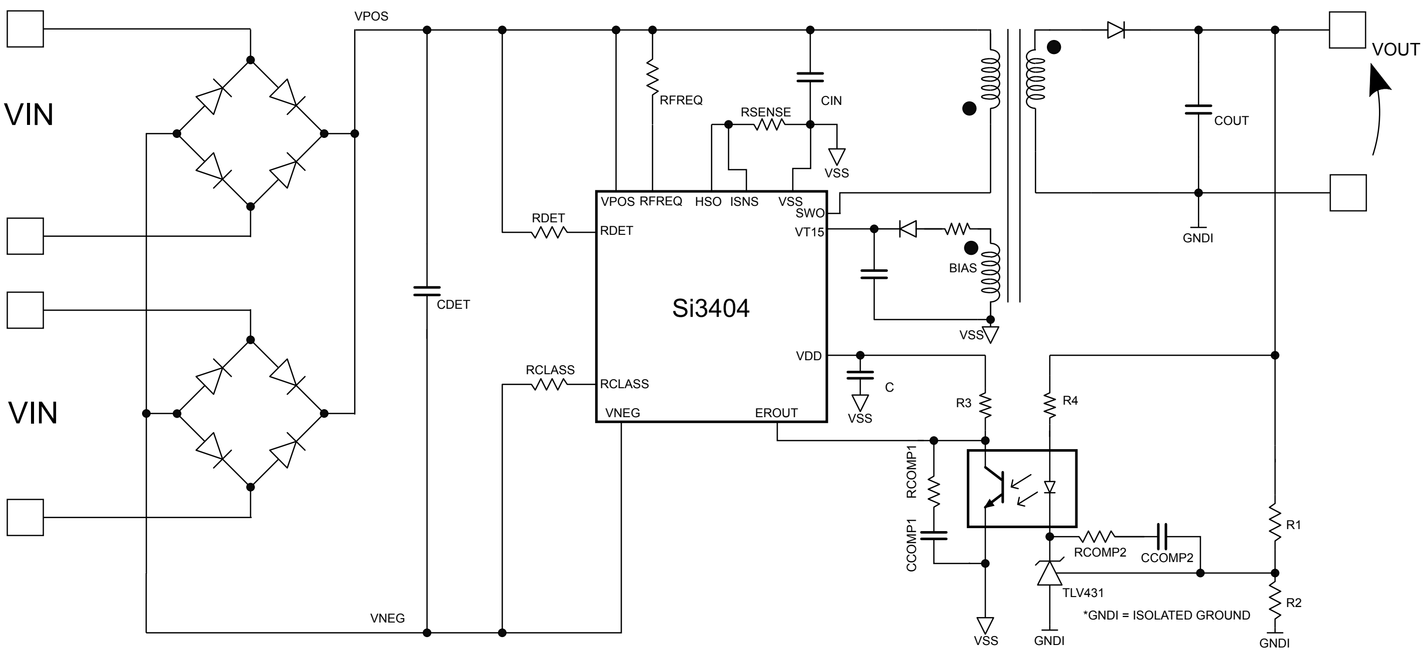


Figure 3.2. Si3404 Isolated Flyback Application Diagram

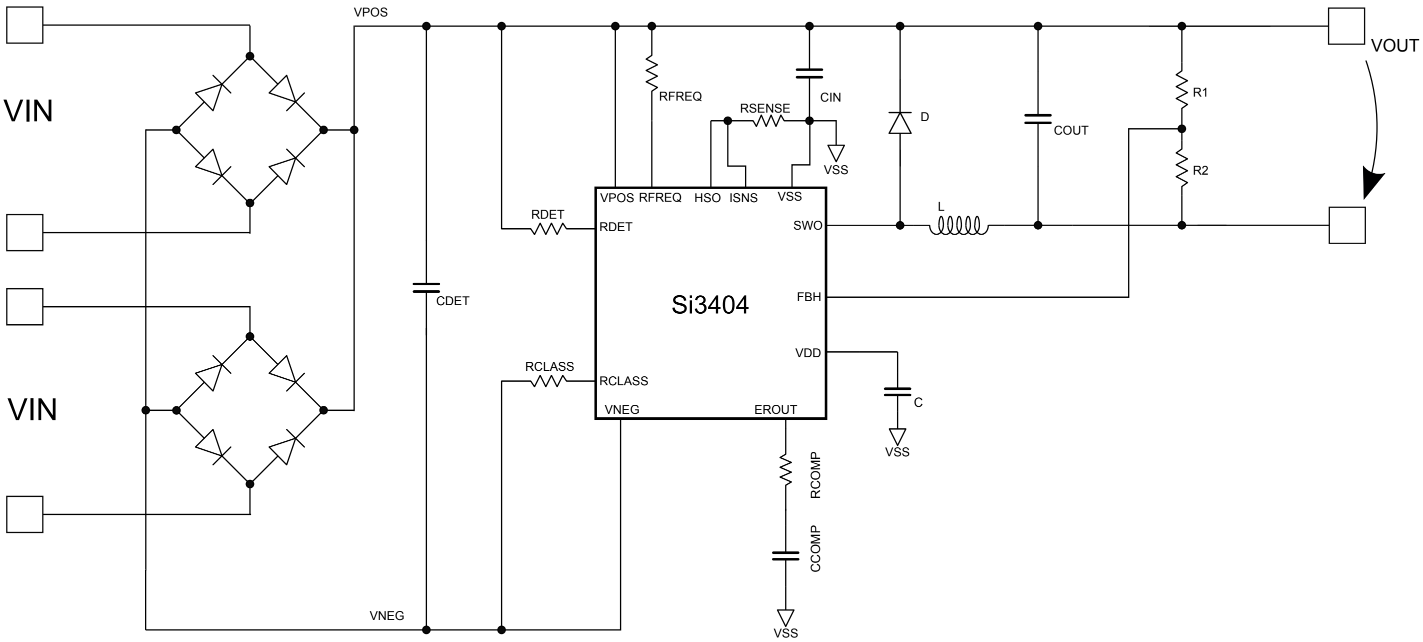


Figure 3.3. Si3404 Buck Application Diagram

4. Electrical Specifications

Table 4.1. Absolute Maximum Ratings[1]

Type	Description	Min	Max	Units
Voltage	VNEG-VSS, VPOS- VNEG, HSO[2], RDET[3]	–0.7	100	V
	SWO-VSS	–0.7	120	V
	ISNS	–1	1	V
	Low Voltage pins: FBH[3], EROUT, FBL, RCL[2], RFREQ[3]	–0.7	6	V
	Mid Voltage pins: VT15	–0.7	18	V
Peak Current	VPOS[4]	–5	5	A
Temperature	Storage Temperature	–65	150	°C
	Ambient Operating Temperature	–40	85	

Note:

1. Unless otherwise noted, all voltages referenced to VSS. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Voltage referenced to VNEG.
3. Voltage referenced to VPOS.
4. Si340x provides internal protection from certain transient surge voltages on these pins. For more information, refer to "AN1130: Using the Si3406/Si34061/Si34062 PoE+ and Si3404 PoE PD Controller in Isolated and Non-Isolated Designs".

Table 4.2. Recommended Operating Conditions

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
V_{PORT}	VPORT = VPOS – VNEG	1.5	—	57	V
V_{HV_OP}	VNEG-VSS, VNEG-HSO, VPOS-VSS	1.5	—	57	V
V_{LV_OP}	VPOS referred low voltage pins: RFREQ, RDET, FBH	–5.5	—	0	V
V_{LV_OP}	VSS referred low voltage pins: VDD, FBL, EROUT	0	—	5.5	V
V_{ISNS_OP}	VSS referred current sensing pin: ISNS	–0.5	—	0.5	V
V_{LV_OP}	VNEG referred low voltage pins: RCL	0	—	5.5	V
V_{MV_VT15}	VSS referred medium voltage pin VT15[1]	12	14.5	16.5	V
I_{AVG}	Allowable continuous current on VPOS, SWO, VSS, HSO, VNEG	—	—	600	mA
I_{MAX}	Max current on HSO, VNEG, VPOS Max 75 ms 5% Duty Cycle	—	—	683	mA

Note:

1. V_{MV_VT15} is relevant for Si3404 only when an external auxiliary bias winding from the primary side of the transformer is being used to improve power conversion efficiency. This can be left undriven, in which case an internal regulator will be used.

Table 4.3. Electrical Characteristics

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
PoE PROTOCOL					
Detection					
V_{DET}	Signature Range (at V_{PORT})	1.5	—	10.1	V
	Signature Resistance (at V_{PORT})	23.75	—	26.25	kΩ
Classification					
V_{RESET}	Classification Reset (at V_{PORT})	0	—	2.81	V
V_{CLASS}	Classification Voltage ON (at V_{PORT})	—	—	14.5	V
	Classification Voltage OFF (at V_{PORT})	20.5	—		V
$I_{PortCLASS}$	Class 0 (R_{CLASS} > 681 Ω)	0	—	4	mA
	Class 1 (R_{CLASS} = 140 Ω @ 1%)	9	—	12	mA
	Class 2 (R_{CLASS} = 75 Ω @ 1%)	17	—	20	mA
	Class 3 (R_{CLASS} = 48.7 Ω @ 1%)	26	—	30	mA
Power On and UVLO					
V_{UVLO_R}	Hotswap closed and converter on	34	37	40	V
V_{UVLO_F}	Hotswap open and converter off	30	32	34	V
V_{UVLO_HYST}		3.5	4.5	6	V
Thermal Characteristics					
T_{shd}	Thermal shutdown	—	160	—	°C
T_{HYST}	Thermal shutdown hysteresis	—	20	—	°C
On-Chip Transient Voltage Suppression/Protection					
V_{PROT}	TVS protection activation voltage (VPOS-VNEG)	100	—	—	V
Hotswap Switch					
I_{inrush}	Inrush current	100	170	200	mA
$I_{MAXHSSW}$	Maximum continuous operating current	—	—	600	mA
V_{HSSW_ON}	Switch ON voltage	—	380	—	mV
V_{HSSW_OFF}	Switch OFF voltage, HSSW goes to overload cycle	—	3.5	—	V
I_{OVL}	Switch current limit in OVERLOAD State	—	10.5	—	mA
$T_{WAITHSSW}$	Wait time in OVERLOAD	80	96	116	ms
R_{ONHSSW}	Internal hotswap drain-source resistance while ON	0.65	1.5	2.9	Ω
DC-DC					

Symbol	Parameter (Condition)	Min	Typ	Max	Unit
$I_{SWOPEAK}$	Peak current limit of internal FET (SWO pin)	2.1	—	2.7	A
F_{OSCINT}	Using internal Oscillator	215	250	290	kHz
F_{OSCEXT}	Using external Oscillator, RFREQ = 215 kΩ	75	95	115	kHz
	Using external Oscillator, RFREQ = 39 kΩ	420	470	520	kHz
DUC	Output duty cycle of PWM	—	—	75	%
V_{FBREF}	FBH (referenced to VPOS) and FBL (referenced to VSS) reference voltage	1.28	1.32	1.36	V
V_{EROUT}	Operating voltage range of error input	1	—	4	V
T_{HICCUP}	Output short protection if EROUT is max	—	1	—	ms
V_{ISNS_OVC}	Overcurrent limit voltage on ISNS (ref. to VSS)	–305	–270	–255	mV
$T_{SOFTSTART}$	Startup time[1]	—	15	—	ms
R_{ONDCDC}	Internal dc-dc switching FET drain-source resistance while ON	—	0.9	1.2	Ω
Regulators					
VT15	Override internal regulator with transformer winding	12.5	—	16.5	V
VDD	5 V regulated output	4.9	5.2	5.5	V
VDD_{ILIM}	dc current limit of VDD	9.7	11.2	—	mA
C_{REG}	Filter capacitor on VDD	82	100	220	nF
Power Dissipation					
P_{INTMAX}	dc-dc max power internal FET	—	0.5	0.9	W
I_{PortOP}	Operating current (V_{PORT} 57 V; 250 kHz)	—	3	5	mA
Package Thermal Characteristics					
$\theta_{JA\text{-}EFF}$	QFN20[2]	—	46.8	—	C°/W

Note:

1. Depends on output load.
2. Assumes 4-Layer PCB with adequate layout.

5. Pin Descriptions

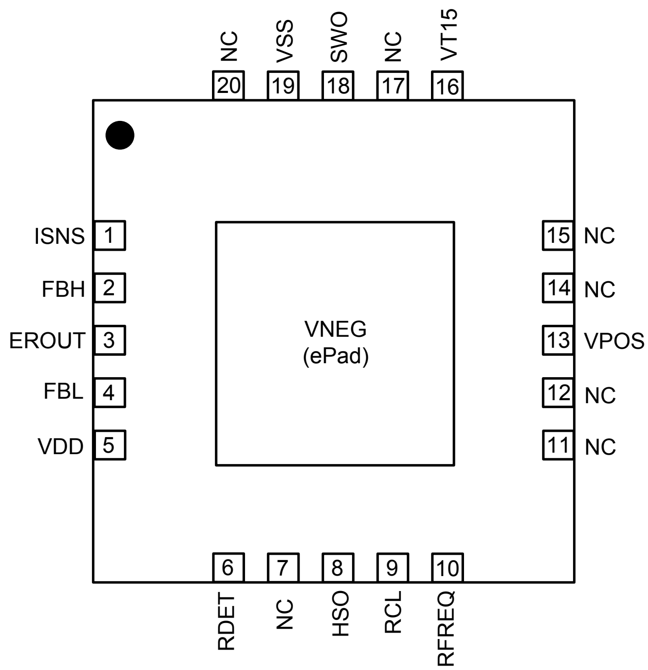


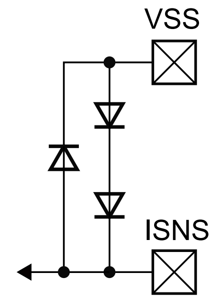
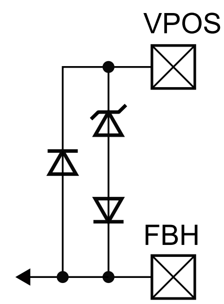
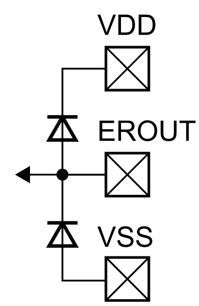
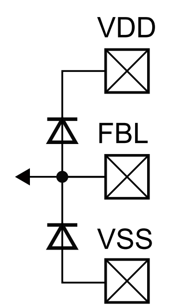
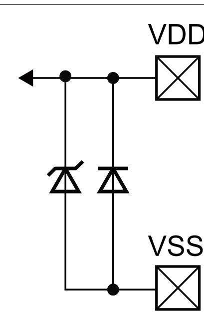
Figure 5.1. Si3404 Pinout

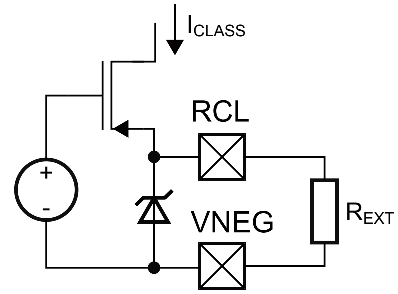
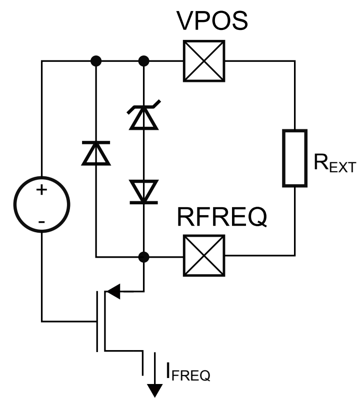
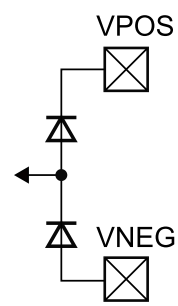
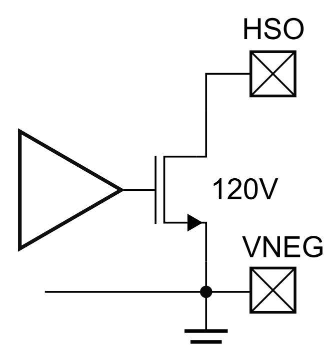
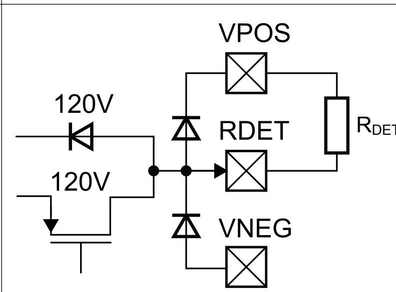
Table 5.1. Pin Descriptions

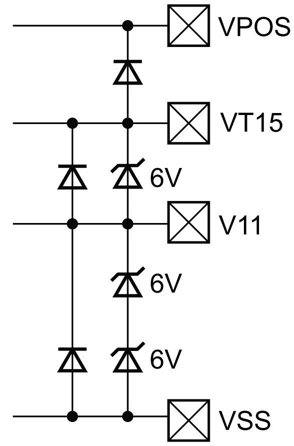
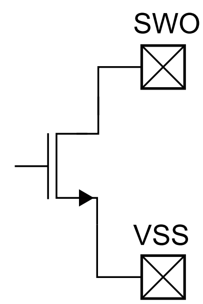
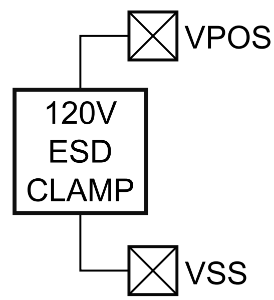
Si3404 Pins	Name	Ref	Dir.	Vrange	Description
1	ISNS	VSS	I	–0.5 to 0	Chip current sense resistor input
2	FBH	VPOS	I	0–5.5	High side (VPOS referred) dc-dc feedback (Buck converter)
3	EROUT	VSS	IO	0–5.5	Error amplifier current output, compensation impedance input
4	FBL	VSS	I	0–5.5	Low side (VSS referenced) dc-dc feedback (Flyback converter)
5	VDD	VSS	O	0–5.5	5 V regulator output
6	RDET	VPOS	IO	0–100	Detection resistor
8	HSO	VNEG	IO	0–100	Hotswap switch output
9	RCL	VNEG	IO	0–5.5	Classification resistor
10	RFREQ	VPOS	IO	0–5.5	Oscillator frequency tuning resistor, tie to VPOS to select default frequency
13	VPOS	—	IO	0–100	Rectified high-voltage supply positive rail
16	VT15	VSS	I	0–16.5	dc-dc transformer auxiliary winding input
18	SWO	VSS	O	0–120	Internal dc-dc switch output (NMOS drain)
19	VSS	—	IO	0	dc-dc converter primary ground
ePad	VNEG	—	IO	0	Rectified high voltage supply ground
7, 11, 12, 14, 15, 17, 20	NC	—	—	—	Connect to VNEG for better thermal performance

5.1 Detailed Pin Descriptions

Table 5.2. Circuit Equivalent and Description of Die Pads

Pin Name	Detailed Description	Circuit Detail
ISNS	Average current sense resistor input. The resistor value will set the maximum allowed current for the application. The overcurrent threshold voltage V_{ISNS_OVC}. Note that this pin voltage goes below VSS.	
FBH	High side dc-dc feedback input. Need to be tied to VPOS when not used. See VFBREF.	
EROUT	dc-dc converter error output; current out, voltage sense. Loop compensating impedance should be connected here. $I_{EROUT} = (V_{FBH} – V_{FBREF})$ x 50 µA or $I_{EROUT} = (V_{FBL} – V_{FBREF})$ x 50 µA	
FBL	Low side dc-dc feedback input. Need to be tied to VSS when not used. See V_{FBREF}	
VDD	Regulated 5 V relative to VSS. There is no foldback characteristic, reaching VDD_{ILIM} the output voltage decreases. The regulator needs C_{REG} external capacitance.	

Pin Name	Detailed Description	Circuit Detail
RCL	Classification resistor input. For class 0 this pin can be left floating. Pin is active only at time of classification.	
RFREQ	Used for adjusting the oscillator frequency. The frequency is inversely proportional to the value of the connected resistor.	
VPOS, VNEG	Main chip input power. Note that VNEG (the ePad on the bottom of the chip) also provides thermal relief.	
HSO	Hotswap Switch Output. The switch shorts the VNEG and HSO pins, and includes several other functions. See hotswap switch section for details.	
RDET	The user has to tie the RDET resistor between this pin and VPOS. During detection, a high voltage switch pulls down RDET to VNEG. After detection, the reference block uses RDET as absolute chip current reference, forcing –750 mV relative to VPOS, creating 30 µA for the internal blocks.	

Pin Name	Detailed Description	Circuit Detail
VT15	VT15 is input for an optional 15 V supply generated by an auxiliary transformer bias winding. If the bias winding voltage is lower than VT15_MIN, the internal 15 V coarse regulator will provide the current for the 11 V regulator. V11 is not available on the Si3404 but is included to show internal connections.	
SWO	dc-dc converter switching transistor drain output, Vmax = 120 V.	
VSS	dc-dc converter ground.	

6. Packaging

6.1 Package Outline: Si3404

The figure below illustrates the package details for the Si3404. The table lists the values for the dimensions shown in the illustration.

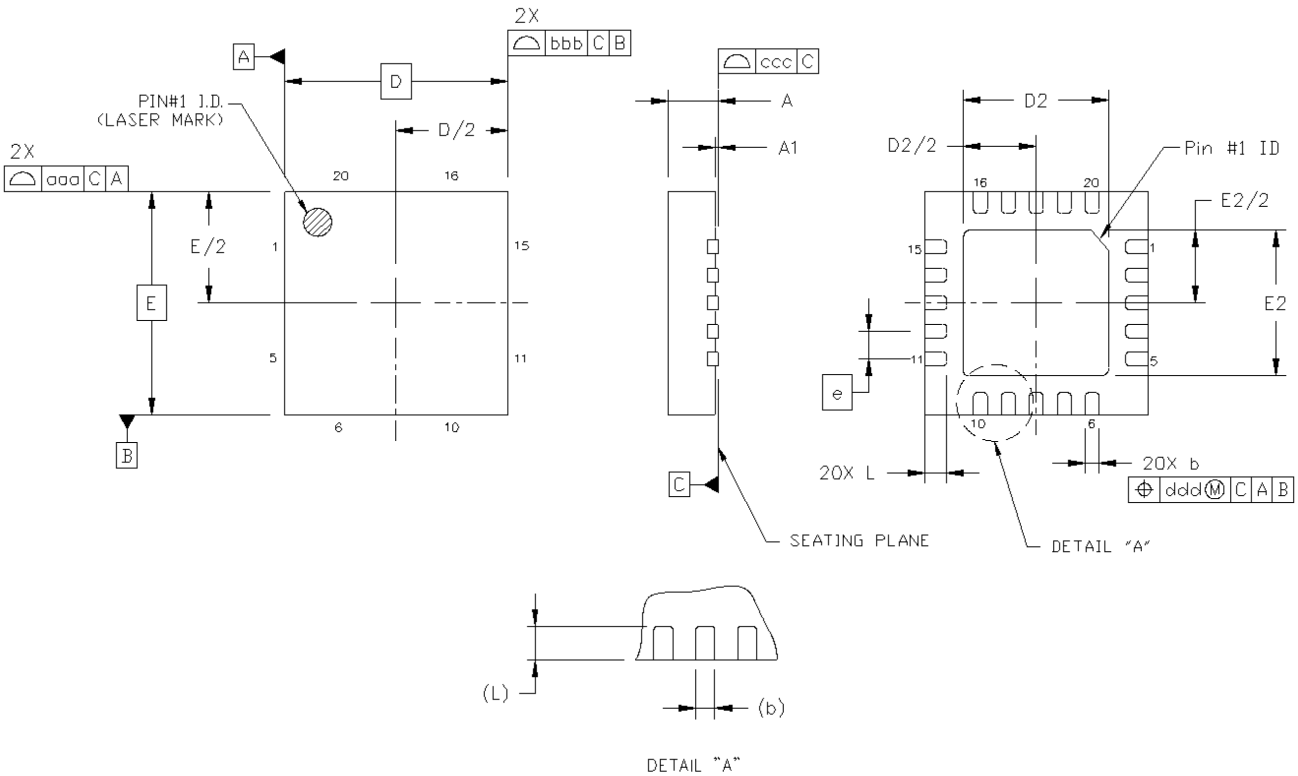


Figure 6.1. 20-Pin, QFN Package

Table 6.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	4.00 BSC.		
D2	2.55	2.60	2.65
e	0.50 BSC.		
E	4.00 BSC.		
E2	2.50	2.60	2.70
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 Land Pattern: Si3404

The figure below illustrates the land pattern details for the Si3404. The table lists the values for the dimensions shown in the illustration.

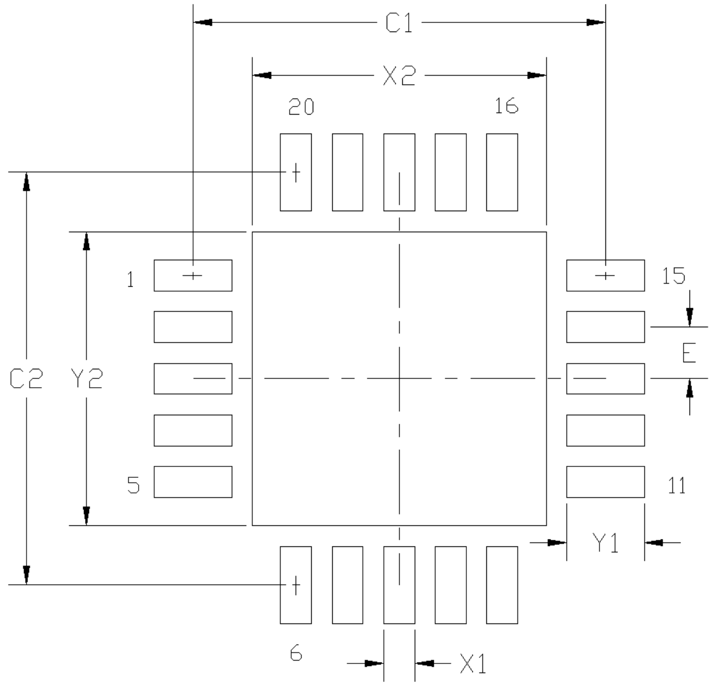


Figure 6.2. 20-Pin, QFN Land Pattern

Table 6.2. Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC	
X1	0.20	0.30
X2	2.55	2.65
Y1	0.65	0.75
Y2	2.55	2.65

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Si3404 Top Marking

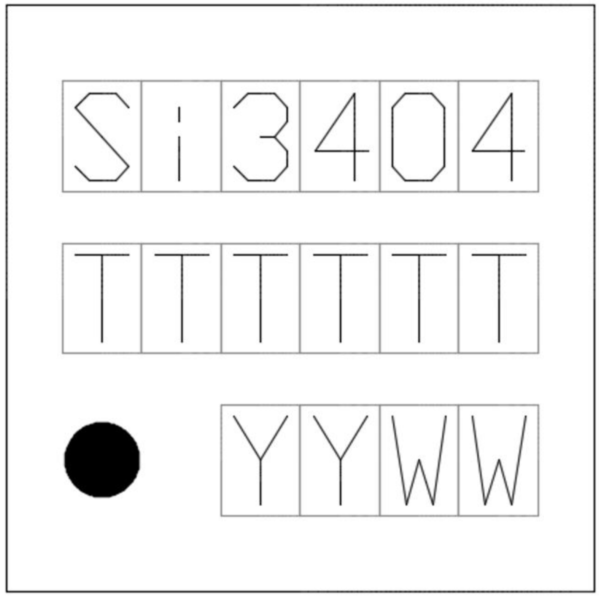


Figure 7.1. Si3404 Top Marking

Table 7.1. Si3404 Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Circle = 0.50 mm Diameter (Lower-Left Corner)	
Font Size:	0.6 Point (24 mils)	
Line 1 Mark Format:	Device Part Number	Si3404
Line 2 Mark Format:	TTTTTT	Trace code from the Assembly Purchase Order form
Line 3 Mark Format:	YY = Year WW = Work Week	Assembly Year Assembly Week

8. Revision History

Revision 1.1

October, 2021

- Updated Figure 2.4 Si3404 DC-DC Converter Block Diagram on page 7.
- Updated Table 6.2 Land Pattern Dimensions on page 22.
  - Updated Solder Mask Design spec.

Revision 1.0

July, 2018

- Updated Figure 2.2 Powered Device Voltages on page 5.
  - Removed Type 2 signaling from diagram.
- Updated Figure 2.3 Hotswap Switch 4-State Machine on page 6.
  - Clearer state transition diagram and improved transition descriptions.
- Updated 2.5.1 Average Current Sensing, Overcurrent, Low-Current Detection, and Output Short Protection.
  - Added information on output short protection.
- Updated Table 4.1 Absolute Maximum Ratings[1] on page 11.
  - Added min and max current for VPOS.
  - Added note about internal surge protection.
- Updated Table 4.2 Recommended Operating Conditions on page 12.
  - Added VPOS to I_{AVG} spec; changed I_{PEAK} to I_{MAX}, and removed SWO and VSS from specification.
- Updated Table 4.3 Electrical Characteristics on page 13.
  - Updated V_{DET} spec to include low threshold and high threshold specs.
  - Updated classification reset max voltage (V_{RESET}) based on final characterization data.
  - Updated classification voltage V_{CLASS} based on final characterization data.
  - Added max and min V_{UVLO_R}, V_{UVLO_F}, and V_{UVLO_HYST} max and min voltages.
  - Removed I_{OVL} max and min current.
  - Added min and max frequency to F_{OSCINT} based on final characterization data.
  - Removed “TBD” from DUC spec.
  - Added max and min V_{FBREF} voltage.
  - Added T_{HICCUP} typical spec.
  - Added max and min V_{ISNS_OVC} voltage.
  - Updated $T_{SOFTSTART}$ time based on application data and added note about dependence on output load.
  - Updated min VT15 based on characterization data.
  - Updated VDD min, typ, and max based on final characterization data.
  - Added VDD_{ILIM} max voltage.
  - Added min and max C_{REG} capacitance.
  - Updated P_{INTMAX} based on final characterization data.
  - Removed P_{MAX} spec.
  - Updated I_{PORTOP} max current based on final characterization data.
- Updated Table 5.1 Pin Descriptions on page 15.
  - Updated Vrange.
- Updated Table 5.2 Circuit Equivalent and Description of Die Pads on page 16.
  - Added detail to VT15 pin description.

Revision 0.5

February, 2018

- Updated 2. System Overview and 3. Application Examples.
  - Added theory of operation and application content.
- Updated Table 4.1 Absolute Maximum Ratings[1] on page 11, Table 4.2 Recommended Operating Conditions on page 12, and Table 4.3 Electrical Characteristics on page 13.
  - Clarified multiple parameters.
- Added 5.1 Detailed Pin Descriptions.
- Added 6. Packaging including outline and land pattern.

Revision 0.1

March, 2017

- Initial release.

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