ICs for Communications

Content Addressable Memory Element
CAME
PXB 4360 F Version 1.1

Data Sheet 07.2000

Version 1.1

PXB 4360 F **Revision History: Current Version: 07.2000**		
Previous Version: Preliminary Data Sheet 11.97 (DS 2)		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
The Data Sheet has been reorganized.		

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Edition 07.2000

This edition was realized using the software system FrameMaker®.

Published by Infineon Technologies AG,
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Balanstraße 73,
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Table of Contents Page

List of Figures

Page

List of Tables

Page

1 Overview

The PXB 4360 F ATM Content Addressable Memory Element (CAME) is a member of the Infineon ATM622 chip set. The entire chip set consists of:

- PXB 4330 E ATM Buffer Manager (ABM)
- PXB 4340 E ATM OAM Processor (AOP)
- PXB 4350 E ATM Layer Processor (ALP)
- PXB 4360 F Content Addressable Memory Element (CAME)

Main ATM Layer functionality is achieved with only two chips, ALP and ABM. The combination of these two devices provides elementary ATM functionality such as header translation, policing, OAM support, multicast, and traffic management (see **figure 1**). The functionality is upgradeable to full OAM support by the AOP (see **figure 2**) and to arbitrary header translation by the CAME (see **figure 3**).

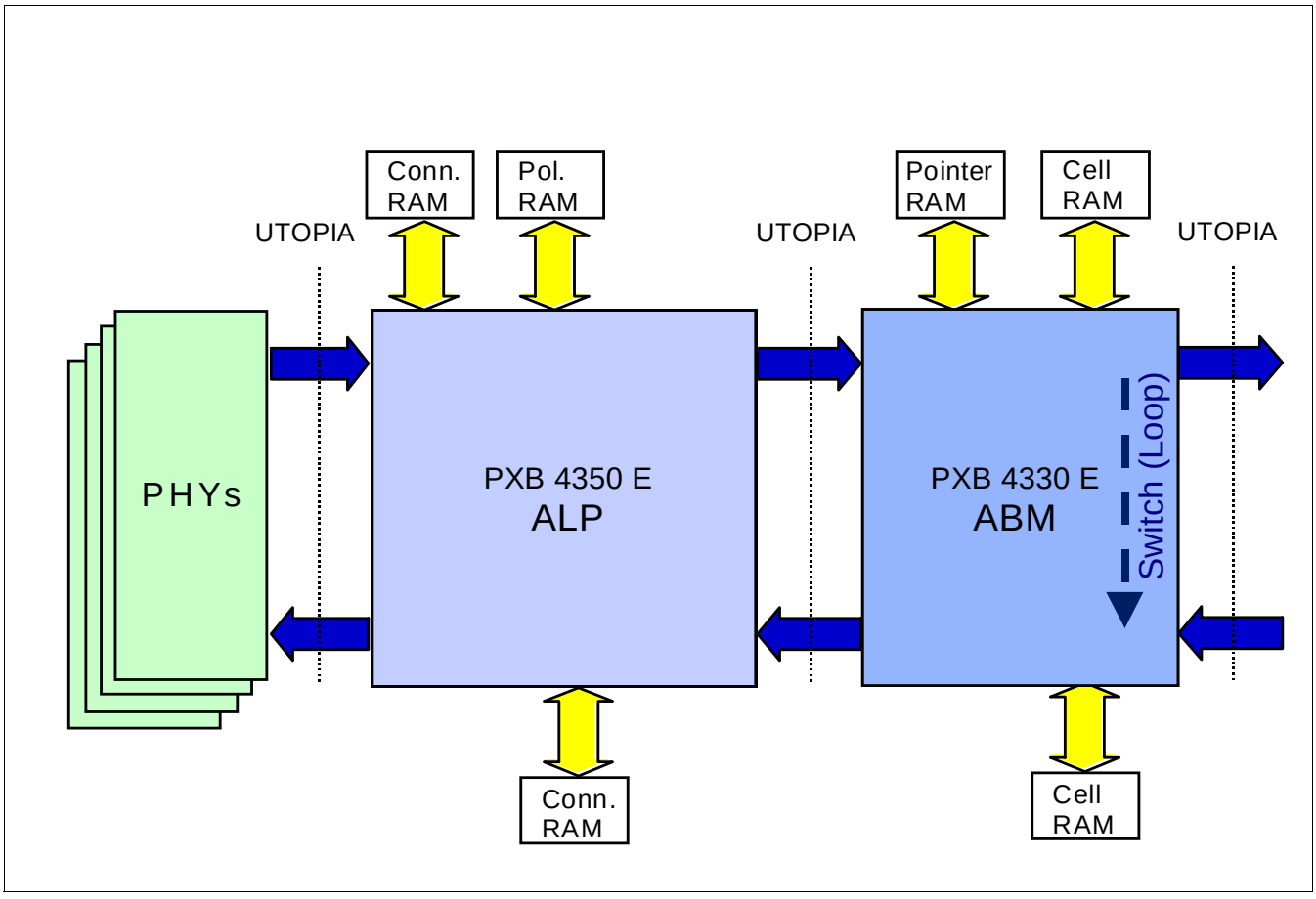


Figure 1 Chipset Configuration for Main ATM Layer Functionality

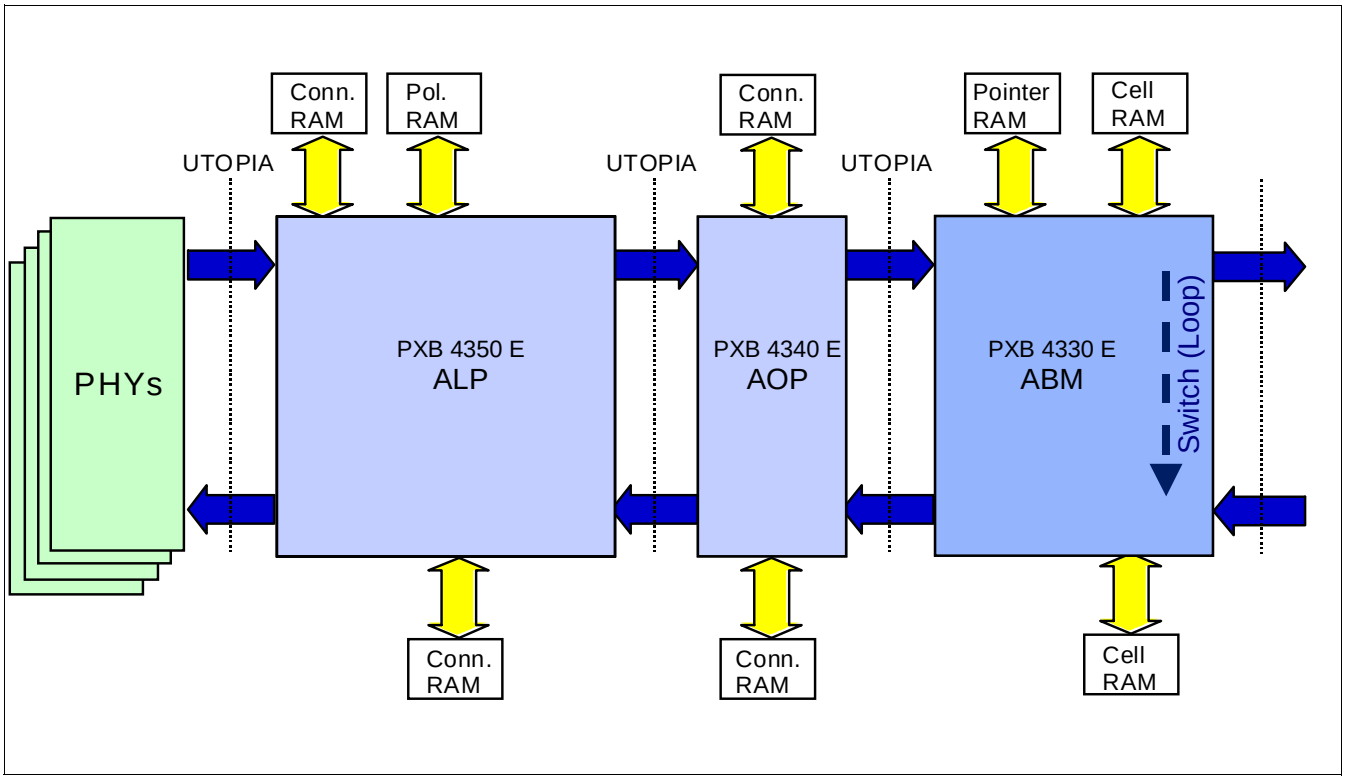


Figure 2 Chipset Configuration for Main ATM Layer Functionality Plus Full OAM

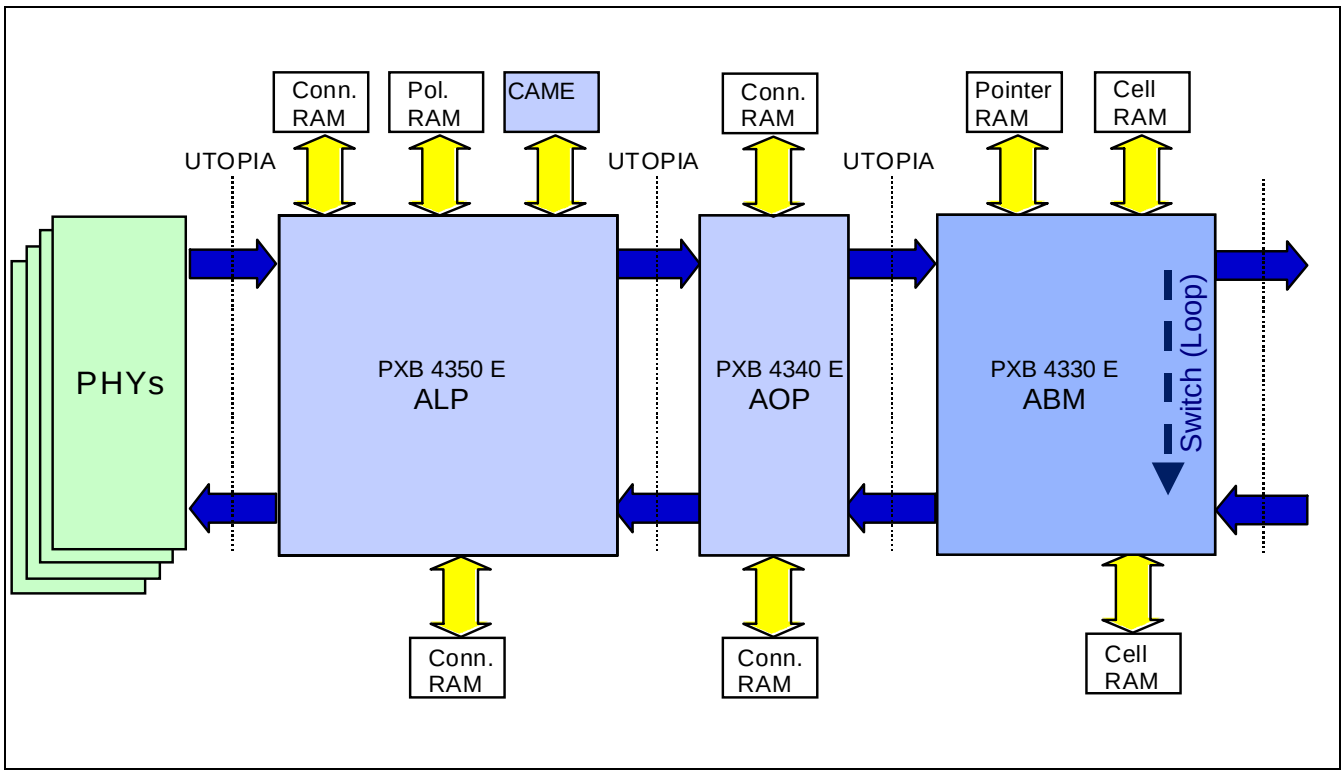


Figure 3 Chipset Configuration for Main ATM Layer Functionality Plus Full OAM and Arbitrary Header Translation

The ATM 622 Layer devices can be used as ....

...a full switch in:
ADSL Concentrators / Multiplexers (DSLAM)
Access Multiplexers
Access Concentrators
Multiservice switches

...Line card in:
Workgroup Switches
Edge Switches
Core Switches

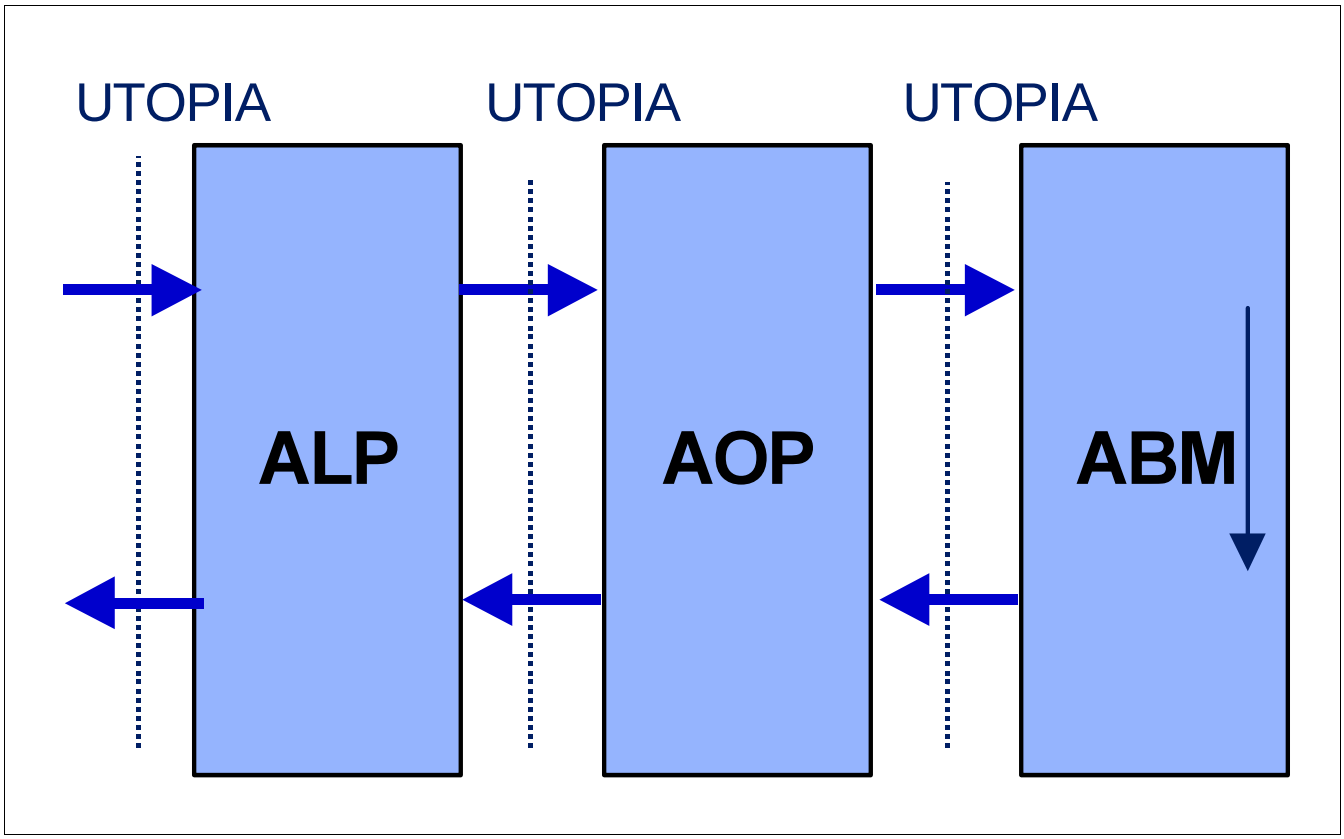


Figure 4 Miniswitch Configuration

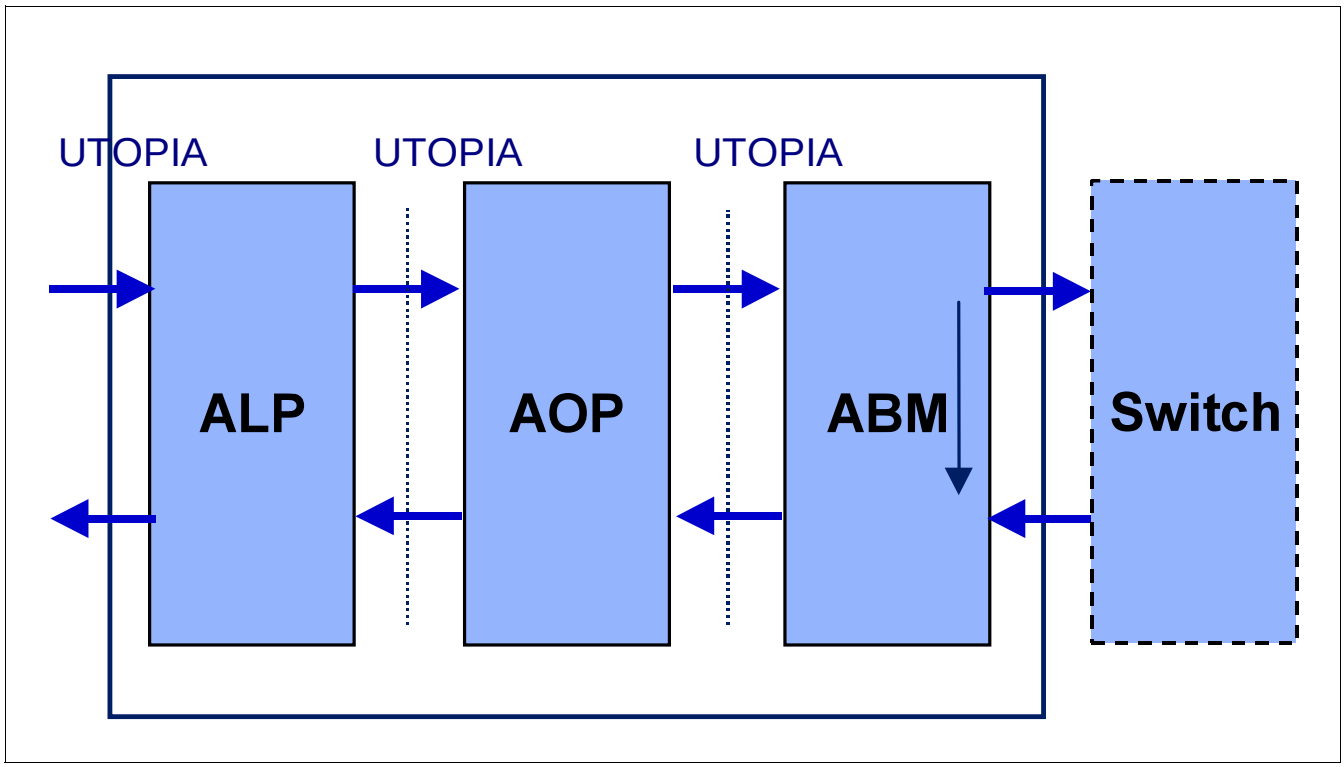


Figure 5 Line Card Configuration

Due to their immensely flexible scaling facilities, feature set, and throughput, the Infineon ATM622 layer chips are ideal devices for almost any ATM system solution.

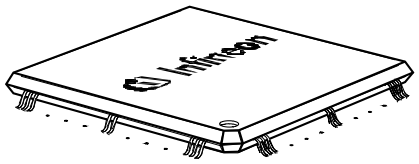
Content Addressable Memory Element
CAME

PXB 4360 F

Version 1.1

CMOS

Features



P-TQFP-144-2 / -3

- ALP Co-processor for Address Reduction to search for a Port Number PN, VPI and VCI the corresponding Local Connection Identifier LCI
- Delivers search result during one cell cycle for Bit rates up to 686 MBit/s
- CAME supports up to 8192 search entries
- Master or Slave mode is selectable to cascade 2 CAME chips to support up to 16384 search entries
- 16-bit or 32-Bit Data Interface is selectable; ALP uses the 16-Bit interface
- Microprocessor Interface is not necessary as CAME is configurated via Address and Data Bus
- Three search modes are supported:
  - Search for LCI and the corresponding PN, VPI and VCI
  - Search for PN, VPI and VCI the corresponding LCI
  - Search for PN and VPI the corresponding first valid LCI for F4 OAM cells
- Status Report provides:
  - Information on search result: single match, mismatch or multimatch
  - Information on whether the connection is valid or invalid for a given LCI, PN, VPI and VCI
  - Information on whether the VP is terminated or not for a given LCI, PN, VPI and VCI
- Parity error indication for Data Bus and CAME cascade error indication
- Boundary Scan support according to JTAG
- Technology:
  - TQFP-144 package
  - 3.3 V Power Supply
  - typical Power dissipation 0.3 W
  - Temperature range from 0°C to +70°C

Type	Package
PXB 4360 F	P-TQFP-144-2/-3

1.1 Logic Symbol

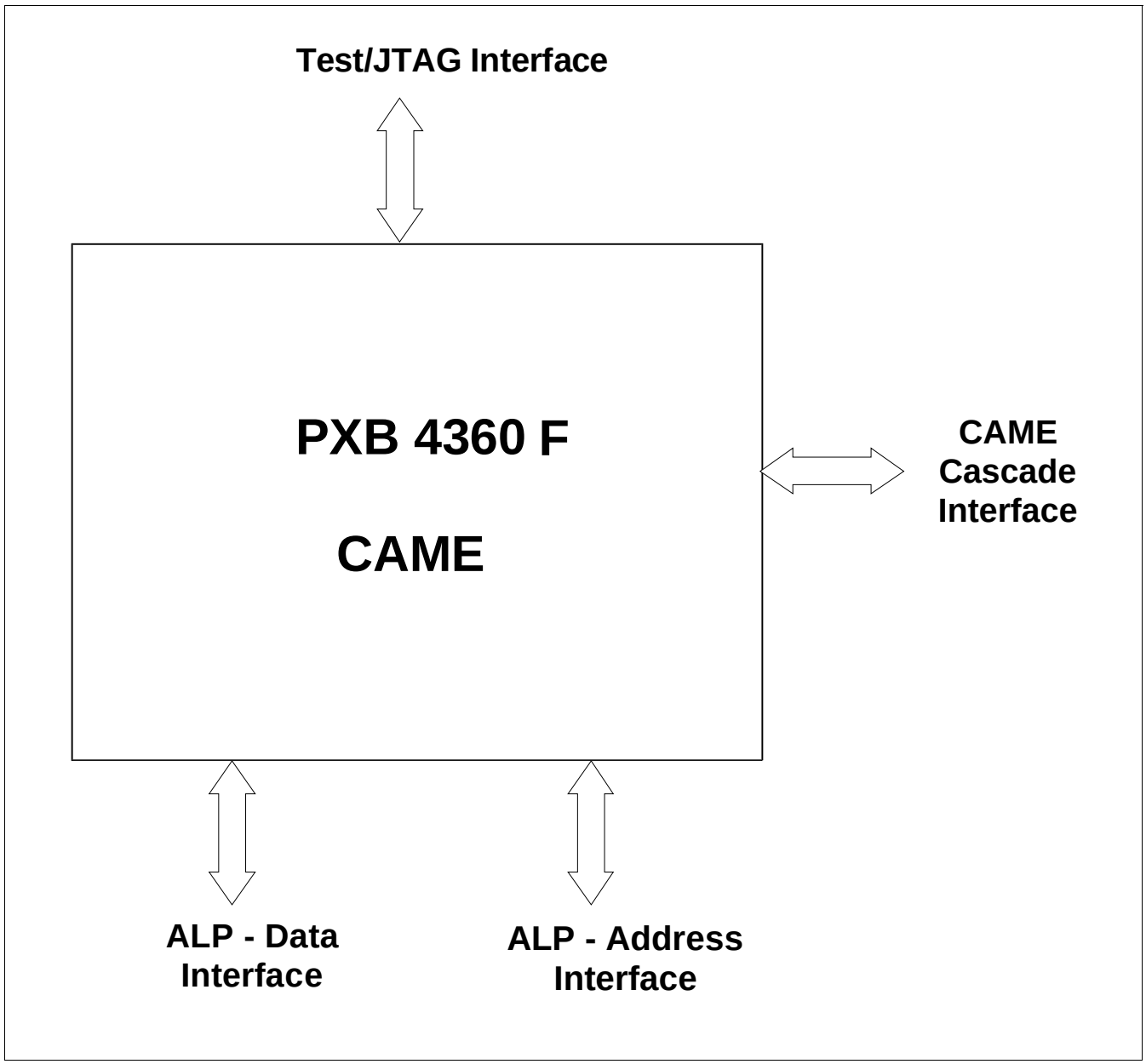


Figure 6 CAME Logic Symbol

1.2 Pin Configuration

(Top view)

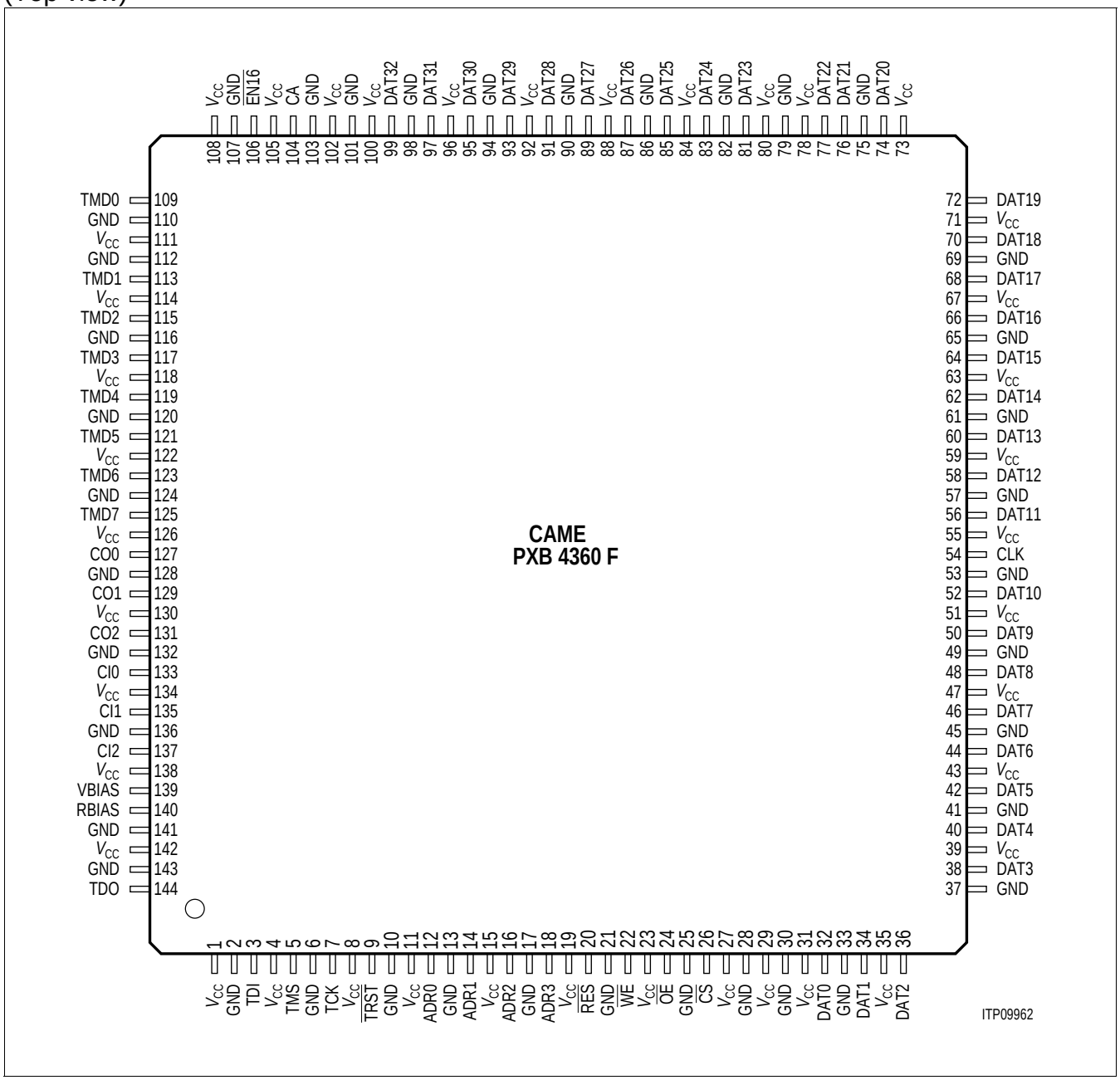


Figure 7 CAME Pin Configuration

1.3 Pin Definitions and Functions

The following explanations apply to all pins within a field in the following table:
Pins with a [1)] attached are connected with an internal pull up resistor.

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
General (2 pins)			
20	$\overline{\text{RES}}$	I	Hardware reset signal Active low
54	CLK	I	Clock input of bus interface
Data and Address Bus Interface between CAME and ALP (41 pins)			
99, 97, 95, 93, 91, 89, 87, 85, 83, 81, 77, 76, 74, 72, 70, 68, 66, 64, 62, 60, 58, 56, 52, 50, 48, 46, 44, 42, 40, 38, 36, 34, 32	DAT (32:0)	I/O	Data bus of bus interface including parity bit (DAT(0)).
18, 16, 14, 12	ADR (3:0)	I	Address bus of the bus interface
26	$\overline{\text{CS}}$	I	Chip enable signal of the bus interface. Active low
24	$\overline{\text{OE}}$	I	Output enable signal of the bus interface. Active low
22	$\overline{\text{WE}}$	I	Write enable signal of the bus interface. Active low
106	$\overline{\text{EN16}}$	I	16-Bit mode enable signal of the bus interface. If 0, then DAT(16:0) are used. If 1, then DAT(32:0) are used. With ALP, this pin should be 0 for use with the 16-bit data bus.
CAME Cascade Interface (7 pins)			

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
104	CA	I	Cascade interface address input
137, 135, 133	CI (2:0)	I	Cascade interface communication channel
131, 129, 127	CO (2:0)	O	Cascade interface communication channel. Do not connect in single CAME application.
JTAG Interface (5 pins)			
9 [1)]	$\overline{\text{TRST}}$	I	Boundary scan test reset Active low
3 [1)]	TDI	I	Boundary scan test data input
7 [1)]	TCK	I	Boundary scan test clock input
5 [1)]	TMS	I	Boundary scan test mode select
144	TDO	O	Boundary scan test data output
Additional Testpins (8 pins)			
125, 123, 121, 119, 117, 115, 113, 109	TMD (7:0)	O	Test Interface. Only for test purpose. Do not connect.
Miscellaneous (2 pins)			
139	VBIAS	I	Analog reference voltage input, used for a precise adjustment of the internal current sources. VBIAS value: 1.2 V ±10%. VBIAS = 1 switches into "powerdown" and disables CAME functionality.
140	RBIAS	O	Calibration output, used to define the bias current of the internal current sources. A resistor (12.1 kΩ ±1%) must be connected between the RBIAS pin and ground.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Supply and GND (79 pins)			
1, 4, 8, 11, 15, 19, 23, 27, 29, 31, 35, 39, 43, 47, 51, 55, 59, 63, 67, 71, 73, 78, 80, 84, 88, 92, 96, 100, 102, 105, 108, 111, 114, 118, 122, 126, 130, 134, 138, 142			VCC (P3V3) Supply Voltage (nominal 3.3 V)
2, 6, 10, 13, 17, 21, 25, 28, 30, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 75, 79, 82, 86, 90, 94, 98, 101, 103, 107, 110, 112, 116, 120, 124, 128, 132, 136, 141, 143			GND Digital ground (0 V)
Unconnected Pins (0 pins)			
			unconnected pins

2 System Integration

One CAME chip is connected to the ALP if only 8k connections are supported. For 16k connections, a second CAME is cascaded to the first CAME. The ALP is the master device that controls the CAME. If two CAME chips are cascaded, the second CAME must be configured as a slave device to be controlled by the first CAME, which is operated in master mode. The two configurations are illustrated in **figure 8** and **figure 9**.

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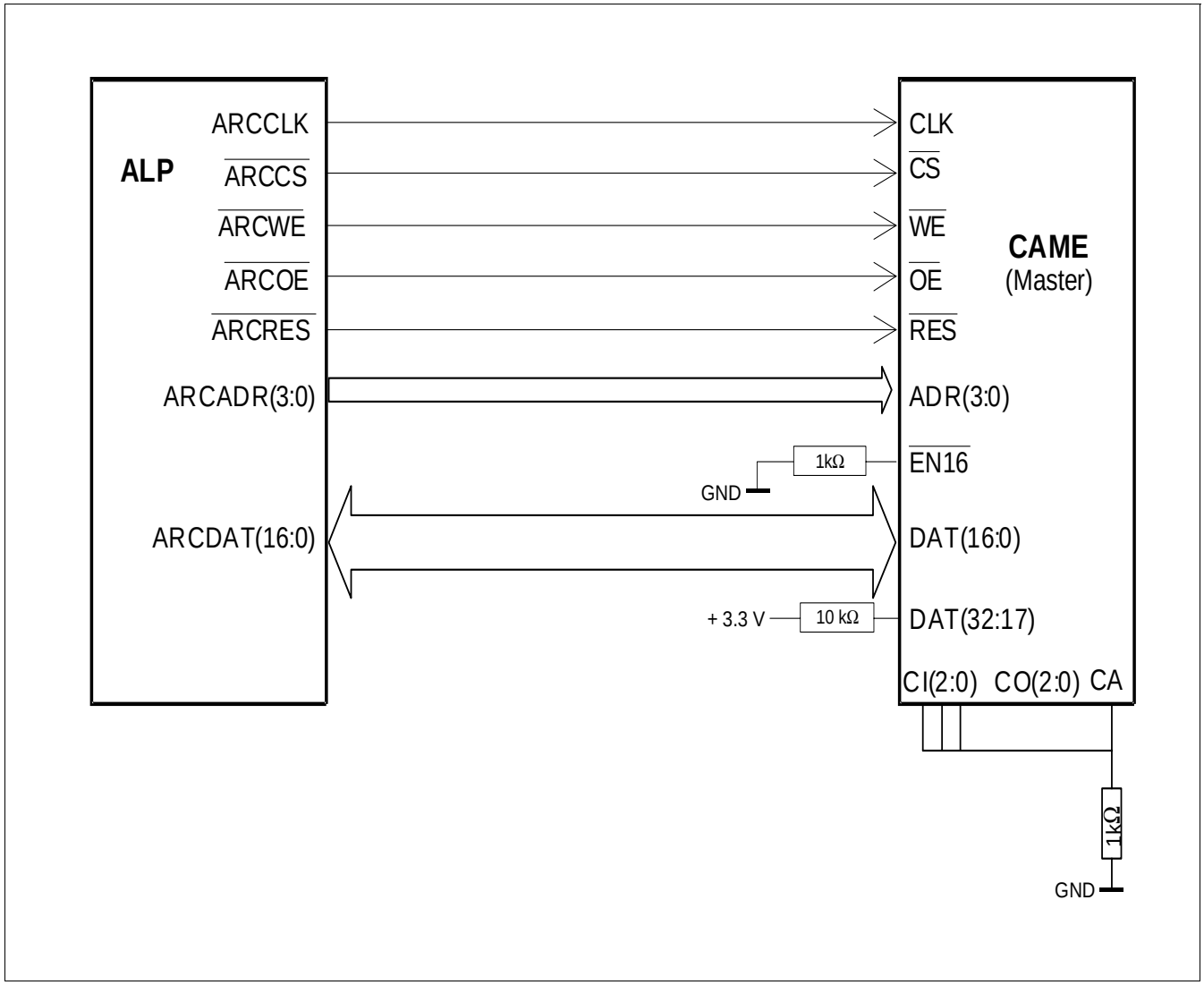


Figure 8 ALP and CAME Application for 8k Connections

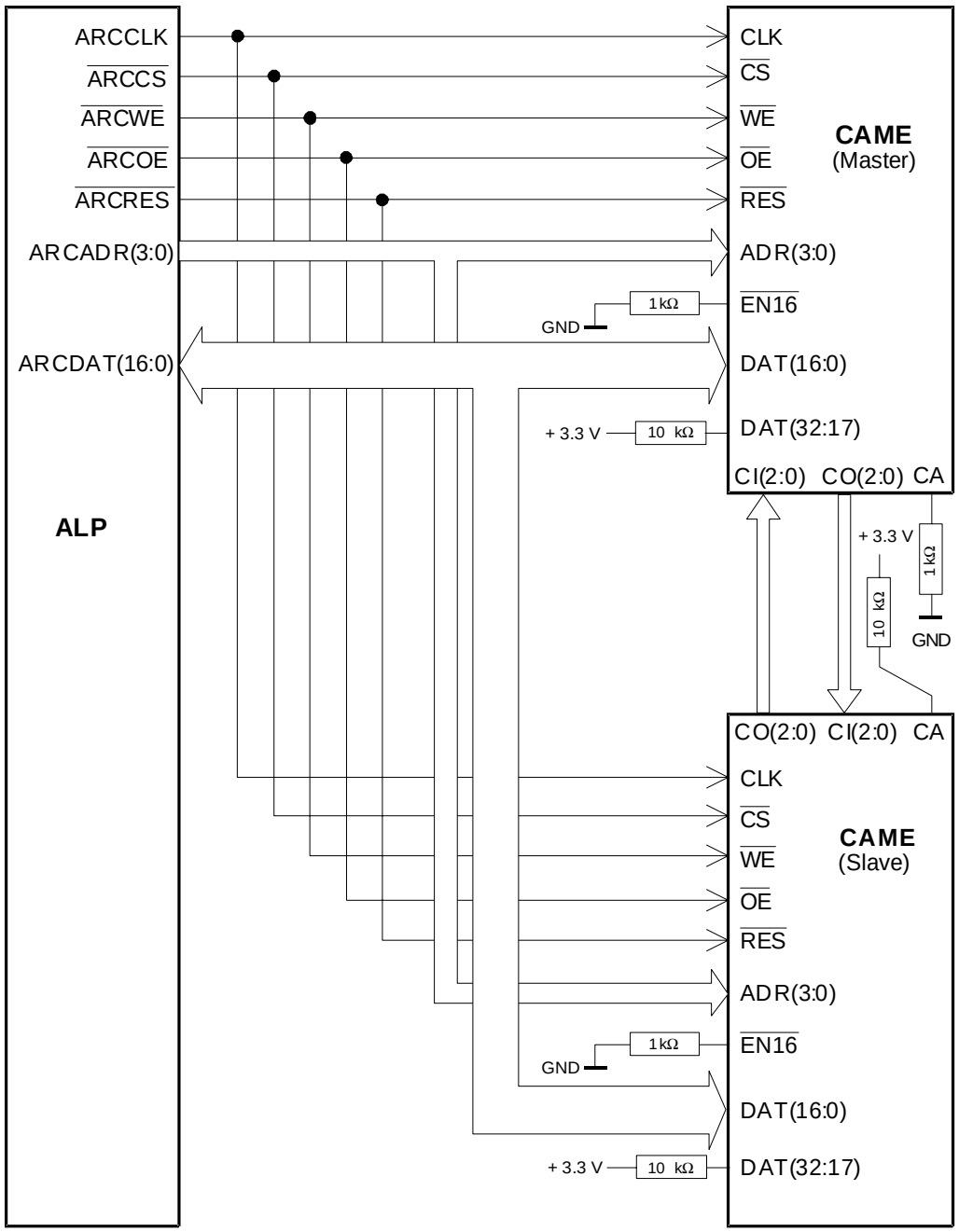


Figure 9 ALP and CAME Application for 16k Connections

3 Functional Overview

The PXB 4360 F is a Content Addressable Memory Element (CAME) that searches for a programmable 32-bit pattern the corresponding programmable 14-bit pattern; or vice versa. Additionally, two search bits are provided to support the search for unused entries and to support the search for F4-OAM connections in ATM. One CAME supports up to 8192 entries. This can be extended up to 16384 entries by adding a second, cascaded CAME, without the need for additional glue logic.

The target application of the CAME is the Address Reduction mechanism for ATM cells performed by the Infineon ATM layer chip ALP PXB 4350. The ALP extracts the Virtual Path Identifier of a standardized ATM cell (VPI) and the Virtual Channel Identifier of a standardized ATM cell (VCI) from the ATM Cell Header and sends them together with the Port Number as a 32-bit pattern to the CAME. After the search procedure of the CAME, the corresponding 14-Bit pattern is sent back to the ALP. The 14-bit pattern is used as a Local Connection Identifier (LCI) inserted into the ATM Cell Header. Herewith, the CAME translates any arbitrary address, within the address range of 2^{32}, into another arbitrary address within the address range of 2^{13} (or 2^{14} if two CAME chips are cascaded). The entire search process is completed during one ATM cell cycle with a bit rate of 686 MBit/s.

4 Data Flow and Functional Description of the CAME

The CAME can be configured, operated, and tested using six Request Commands. Each Request Command is a combination of various write and read commands transmitted via the Data bus of the CAME. The Address bus selects the Request Commands. The data flow for writing the search pattern into the CAME is such that the Local Connection Identifier (LCI) defines the address of the memory where the Port Number (PN), VPI, VCI, and the two auxiliary bits P_IP and VCON are stored. The CAME is operated inversely for cell processing. In the case of cell processing, the PN, VPI, and VCI address the memory in which the LCI is stored. As well as the LCI being transmitted to the ALP, a search report is also transmitted. Request Commands 1 and 2 are activated by the ALP during cell processing. Request Commands 3 through 6 are activated by the microprocessor via the ALP because the CAME has no microprocessor interface. All six Request Commands are described in the following sections.

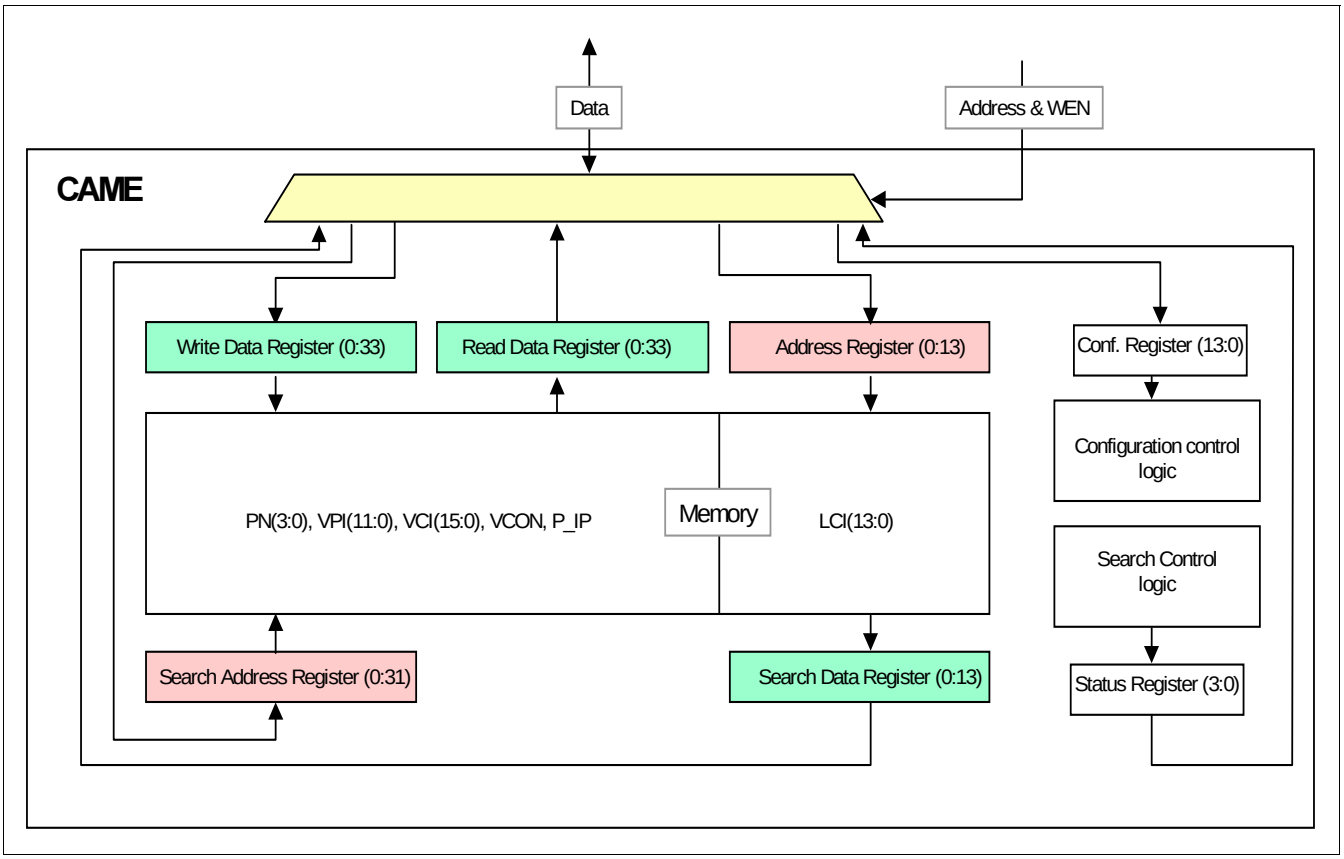


Figure 10 Block Diagram of the CAME

4.1 Programming of the Search and Search Result Pattern

Request Command number 4 should be used for the set up and release of a connection. First, the LCI (14 bits) and the two auxiliary bits VCON and P_IP are written into the Write Data Register and Address Register via the Data bus. Subsequently, the PN, VPI, and the VCI are written into the Write Data Register. Within the 16-bit word, any subdivision by the PN and VPI is allowed. The LCI of the Address Register defines the address of the memory in which the contents of the Write Data Register are written. After writing the entry into memory, status information on the current request is stored in the Status Register. The Status Register is read out at the end of each request.

The auxiliary bit VCON defines whether an entry is valid or invalid. This mechanism is used to prevent overwriting a valid connection, if the corresponding configuration bit CEE[1)] in the TESTMODE register is set. A second configuration bit, CLE[1)] of the TESTMODE register, is available to prevent a multimatch entry. If CLE and CEE are set, the CAME checks whether the PN, VPI, and VCI already exist. For the case that an entry exists (single or multimatch), the CAME prevents the writing and outputs a failure report to the Status Register. For the case that no entry exists (mismatch), the CAME writes the entry into memory if the LCI entry is invalid; otherwise, the writing is also prevented. If CEE and CLE are not set, there is no checking whether both a valid connection is changed and a multimatch condition is generated. The CEE and CLE have an influence on the execution time of Request Command number 4.

The auxiliary bit P_IP defines whether the connection point is a Path Intermediate Point. If the P_IP is set, the VCI values are ignored during the search process.

In the TESTMODE register, the TWE bit is provided for testing the memory. If it is set, the write request is converted into a test write request and all memory banks are written simultaneously.

4.2 Reading the Search Pattern for a Predefined LCI Value

Request Command number 5 should be used to check the Search Pattern PN, VPI, and VCI and the Search result pattern VCON and P_IP for a given LCI. First, the LCI (14 bits) is written into the Address Register, via the Data bus. Then the PN, VPI, VCI, VCON, and P_IP are written from memory to the Read Data Register. The Read Data Register and the Status Register are read out via the data bus of the CAME.

In the TESTMODE register, the TRE bit is provided for testing the memory. If it is set, the read request is converted into a test read request and all memory banks are read simultaneously.

4.3 Configuration and Testing of the CAME

Request Command number 3 should be used to search for a Search Pattern with deactivated search fields, as defined in the TESTMODE register. This Request Command should be activated by the microprocessor via the ALP and the CAME Interface. It is not used during normal cell processing. First, the PN, VPI, and VCI are written into the Search Address Register, via the Data bus. After a predefined search period, the search results (LCI and the two auxiliary bits VCON and P_IP) are written into the Search Data Register. The status information in the Status Register and the contents of the Search Data Register are read out via the Data bus of the CAME.

In the TESTMODE register, the bits VCEN, VPEN, and VSET are provided to define whether the VCI or the PN and VPI are ignored. Furthermore, it is possible to search for invalid and free entries, identified by VCON as equal to zero. Additionally, a TSE bit is implemented to convert the search request into a test search request which compares all memory banks in parallel.

Request Command number 6 is implemented to configure the CAME for operation and test. This request is a substitute for the microprocessor interface. The configuration and test mode commands are written into the TESTMODE register via the Data bus of the CAME. Herewith it is possible to:

- Check the cascade interface between the Master and Slave CAME devices
- Check the parity of the Data bus and Address bus of the CAME
- Read the version number of the CAME

1) Note that CEE and CLE are not supported by the ALP

- Configure the response on Write Request Command number 4
- Configure the response on Search Request Command number 3
- Configure the test functions of the CAME.

4.4 Search Operation for Cell Processing

Two Search Request Commands are supported by the CAME. Search Request Command number 1 is used for search processing of F4-OAM cells at the VP termination point. Normally, the F4-OAM cells are identified by VCI value 3 or 4 for segment or end-to-end flow. The ALP identifies the F4-OAM cells and uses Search Request Command number 1. Herewith, the PN and VPI are written into the Search Address Register via the Data bus of the CAME. After a predefined search period, the search results (LCI and the two auxiliary bits VCON and P_IP) are written into the Search Data Register. Subsequently, the search data and status information are read from the ALP. In the case of a valid search result, the LCI value is written into the GFC, VPI and UDF1 fields of the ATM cell. Herewith, the CAME and ALP borrow a VCI from the user cell which identifies the F4-OAM cells as VCI value 3 or 4 in order to transmit the F4-OAM cell to the AOP. This mechanism reduces the number of LCI needed for to transport F4-OAM cells between the ALP and the AOP. The ALP ignores the multimatch alarm from the CAME for the F4-OAM cells as it is obvious that a terminated VP delivers a match for all VCIs if only the PN and VPI value are used as a search pattern. The LCI value used is the lowest LCI.

Search request number 2 is used for search processing of cells belonging to a VC or VP connection. This search request is identical to Search Request Command 1 except that the VCI value is also written into the Search Address Register. For VP connections, the auxiliary bit P_IP must be set which suppresses the VCI search pattern. Herewith, only the PN and VPI values are considered.

The data structures of the six Request Commands and the corresponding write and read commands for the 16-bit and 32 bit modes are described in the following sections.

4.4.1 Data Structure of Request Commands for 16-Bit Mode

CAME Data bit (16) is used as parity line and completes the ARCDAT(1:15) and ACRADR(0:3) to odd parity. Note: Shaded fields represent unused bits.

Request Number 1[1)]
Search Processing for OAM F4 Flow

	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address C_H		PN(3:0)				VPI(11:0)											
Wait for command execution																	
Read from address 6_H		V	I	LCI(13:0)													
Read from address E_H														S3	S2	S1	S0

Request Number 2
Search processing for ATM Cells belonging to VPC and VCC

	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address D_H		PN(3:0)				VPI(11:0)											
Write to address 5_H		VCI(15:0)															
Wait for command execution																	
Read from address 6_H		V	I	LCI(13:0)													
Read from address E_H														S3	S2	S1	S0

Request Number 3
Search Processing activated by the Microprocessor

	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address E_H		PN(3:0)				VPI(11:0)											
Write to address 6_H		VCI(15:0)															
Wait for command execution																	
Read from address 6_H		V	I	LCI(13:0)													
Read from address E_H														S3	S2	S1	S0

[1)] Structure applies to 4-bit PN and 12-bit VPI. If 6-bit PN and 10-bit VPI are selected, the structure of the first dword is bit 15..10 = PN(5:0), bit 9..0 = VPI(9:0) for all requests.

Request Number 4
Write Command for Setup and Release of Connections by the Microprocessor

	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address 2_H		V	I	LCI(13:0)													
Write to address B_H		PN(3:0)				VPI(11:0)											
Write to address 3_H		VCI(15:0)															
Wait for command execution																	
Read from address 6_H																	
Read from address E_H														S3	S2	S1	S0

Request Number 5
Read Command for Verification of the Connection Entry by the Microprocessor

	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address 0_H				LCI(13:0)													
Wait for command execution																	
Read from address 1_H		PN(3:0)				VPI(11:0)											
Read from address 9_H		VCI(15:0)															
Read from address 6_H		V	I														
Read from address E_H														S3	S2	S1	S0

Request Number 6
CAME Test and Configuration Command by the Microprocessor

	bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address 7_H				Testmode(13:0)													
Wait for command execution																	
Read from address 7_H				Testmode(13:0)													
Read from address F_H														S3	S2	S1	S0

4.4.2 Data Structure of the Request Commands for 32-Bit Mode

Note: Shaded fields represent unused bits.

Request Number 1[1)]
Search Processing for OAM F4 Flow

bit:	**31**	**23**	**15**	**7**	**0**
Write to address 4_H of CAME					
	PN(3:0)	VPI(11:0)			
Wait for command execution					
Read from address 6_H of CAME					

	S3	S2	S1	S0	V	I	LCI(13:0)	

Request Number 2
Search processing for ATM Cells belonging to VPC and VCC

bit:	**31**	**23**	**15**	**7**	**0**
Write to address 5_H of CAME					
	PN(3:0)	VPI(11:0)	VCI(15:0)		
Wait for command execution					
Read from address 6_H of CAME					

	S3	S2	S1	S0	V	I	LCI(13:0)	

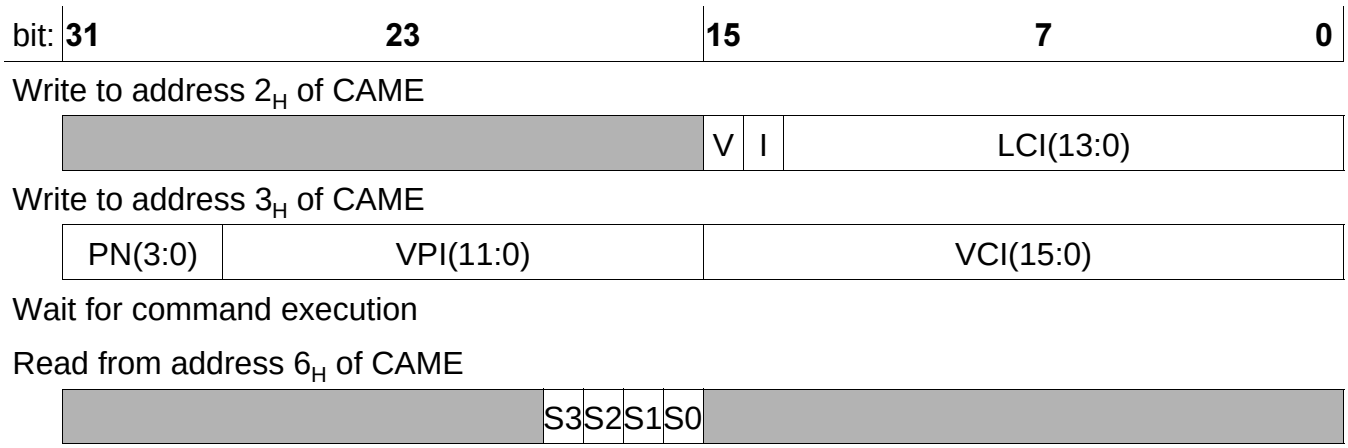
Request Number 3
Search Processing activated by the Microprocessor

bit:	**31**	**23**	**15**	**7**	**0**
Write to address 6_H of CAME					
	PN(3:0)	VPI(11:0)	VCI(15:0)		
Wait for command execution					
Read from address 6_H of CAME					

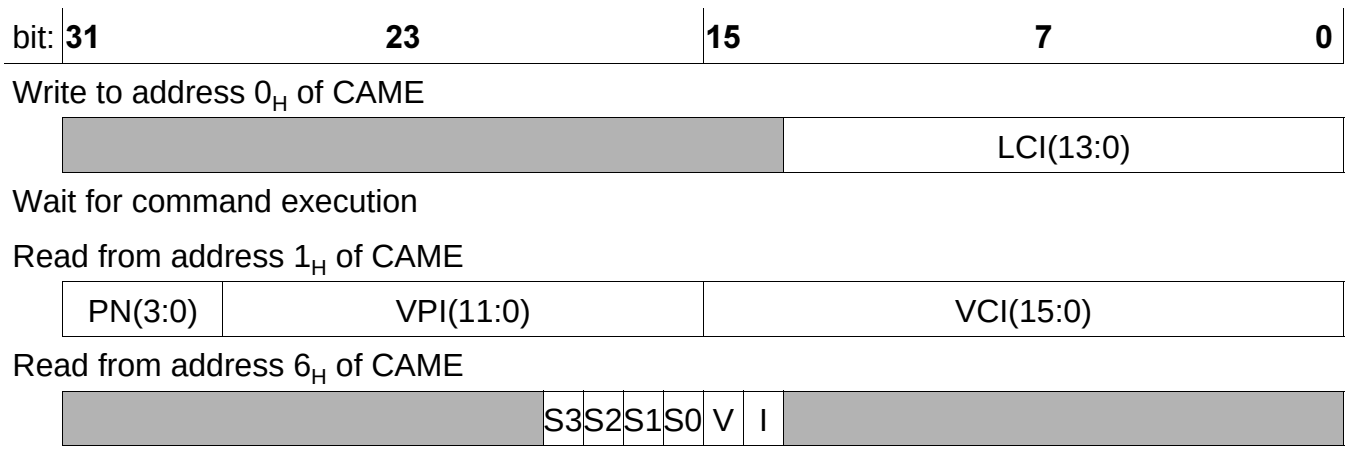
	S3	S2	S1	S0	V	I	LCI(13:0)	

[1)] Structure applies to 4-bit PN and 12-bit VPI. If 6-bit PN and 10-bit VPI are selected, the structure of the first dword is bit 31..26 = PN(5:0), bit 25..16 = VPI(9:0) for all requests.

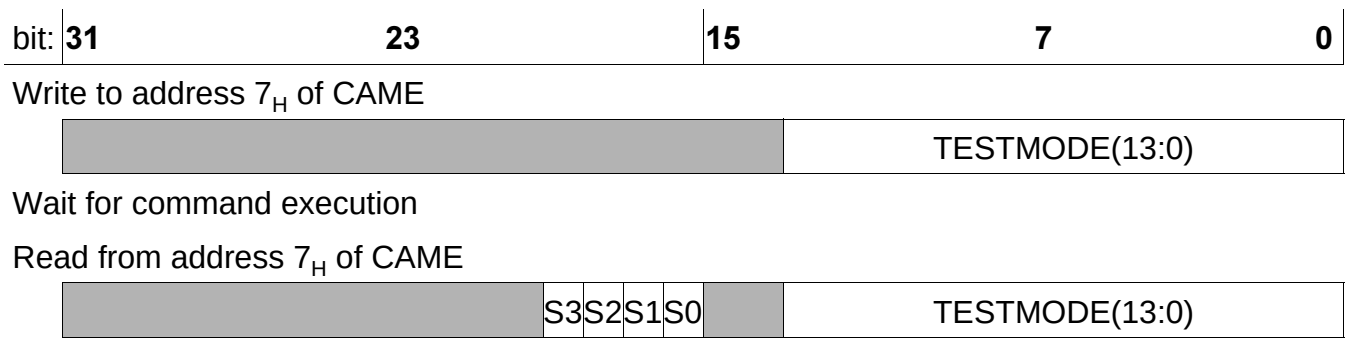
Request Number 4
Write Command for Setup and Release of Connections by the Microprocessor



Request Number 5
Read Command for Verification of the Connection Entry by the Microprocessor



Request Number 6
CAME Test and Configuration Command by the Microprocessor



Note: The I bit represents the P_IP flag, the V bit represents the VCON flag.

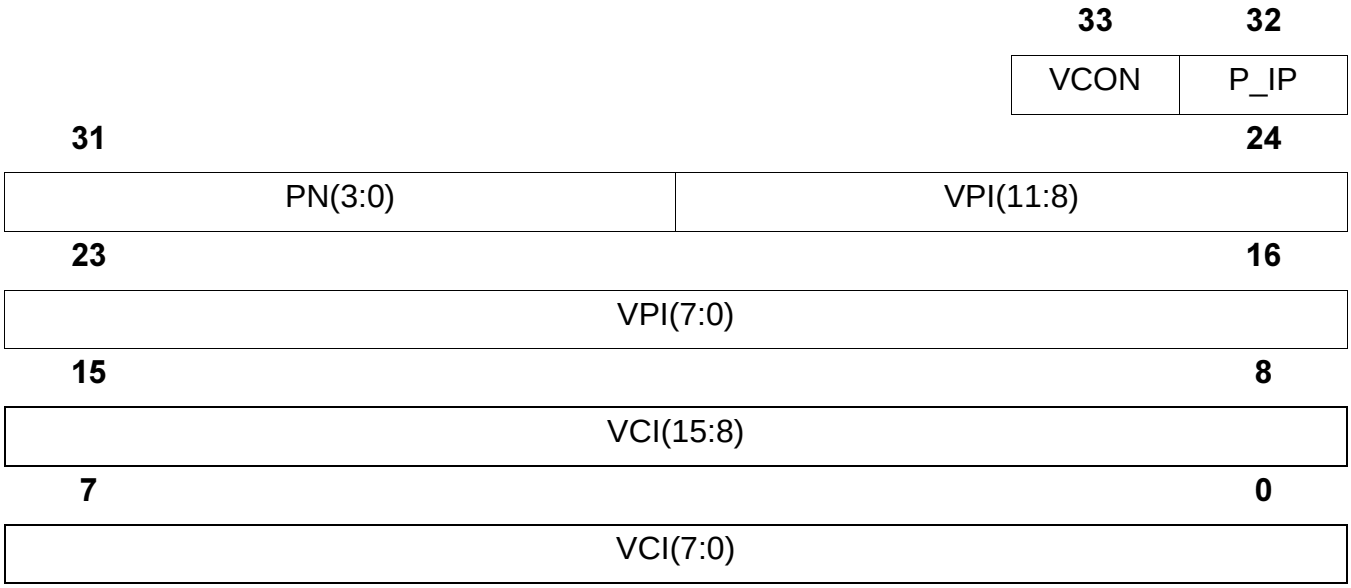
5 Registers

A request command is a sequence of write and read commands at different addresses. The address selects the register and the consequent action performed by the CAME. Therefore, different request commands can write to or read from the same register.

5.1 Write Data Registers

Each of these registers contains a complete entry consisting of PN/VPI/VCI, the P_IP flag and the VCON flag. The registers are loaded from the bus interface at the beginning of write request #4. During request #4, their contents are transferred to the line in CAME memory which is selected with the Address Register (DLCI).

Write Address 2_H, 3_H, B_H
Value after reset undefined



16-Bit Mode	request 4:	2_H for VCON, P_IP 3_H for VCI(15:0) B_H for PN(3:0), VPI(11:0)
32-Bit Mode	request 4:	2_H for VCON, P_IP 3_H for PN(3:0), VPI(11:0), VCI(15:0)

Note: Structure applies to 4-bit PN and 12-bit VPI. If 6-bit PN and 10-bit VPI are selected, the structure is bit 31..26 = PN(5:0) and bit 25..24 = VPI(9:8) for all registers with PN and VPI.

VCON Valid Connection flag:

0 Connection not valid.

1 Connection valid.

P_IP Path Intermediate point flag:

0 Address reduction is performed over PN, VPI and VCI.

1 Path intermediate point; address reduction is performed only over PN and VPI.

PN (3:0) Port Number

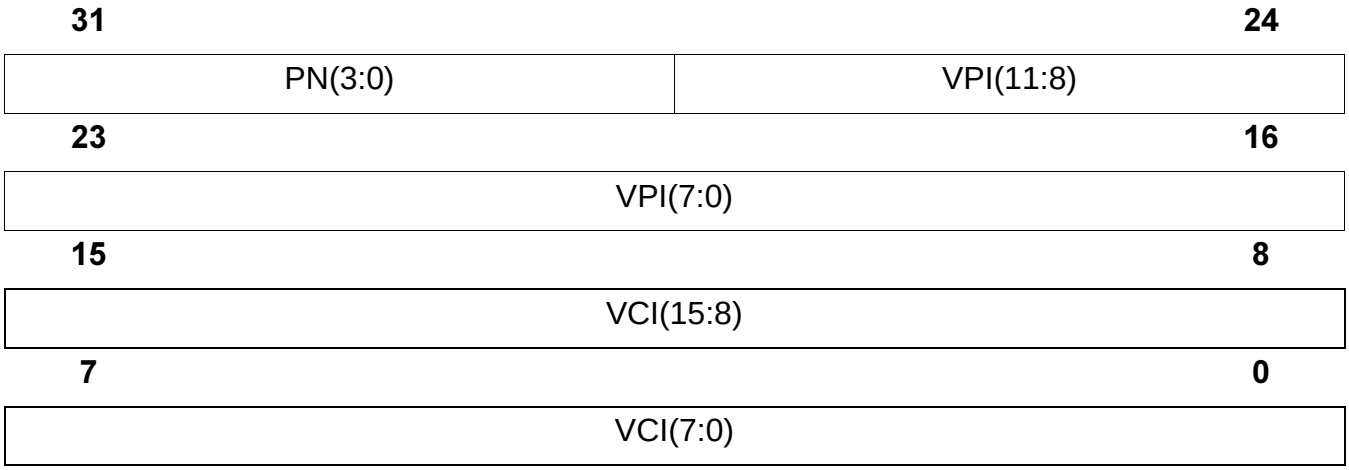
VPI (11:0) VPI value of the ATM Header. PN and VPI are in a 16-bit field. Within the 16 bits, any subdivision into the PN and VPI is allowed.

VCI (15:0) VCI value of the ATM Header.

5.2 Search Address Register

These registers contain the PN, VPI, VCI combination which will be compared to all lines in CAME during search requests #1,#2 and #3. The registers are loaded from the bus interface at the beginning of the respective search request.

Write Address 4_H, 5_H, 6_H, C_H, D_H, E_H
Value after reset undefined



16-Bit Mode	request 1:	C_H for PN (3:0), VPI (11:0)
	request 2:	5_H for VCI (15:0) D_H for PN (3:0), VPI (11:0)
	request 3:	6_H for VCI (15:0) E_H for PN (3:0), VPI (11:0)
32-Bit Mode	request 1:	4_H for PN (3:0), VPI (11:0)
	request 2:	5_H for PN (3:0), VPI (11:0), VCI (15:0)
	request 3:	6_H for PN (3:0), VPI (11:0), VCI (15:0)

PN (3:0) Port Number

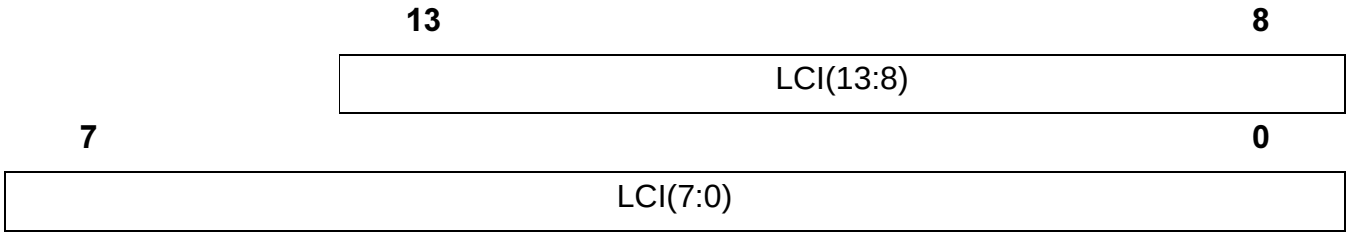
VPI (11:0) Virtual Path Identifier value of the ATM Header. PN and VPI are in a 16-bit field. Any subdivision within the 16-bits for the PN and VPI is allowed.

VCI (15:0) Virtual Channel Identifier value of the ATM Header.

5.3 Address Register (DLCI)

This register contains the address of the line to which data is written in a write request #4, or from which data is read in a read request #5. The DLCI register is loaded from the bus interface at the beginning of the respective read or write request.

Write Address 0_H, 2_H
Value after reset undefined



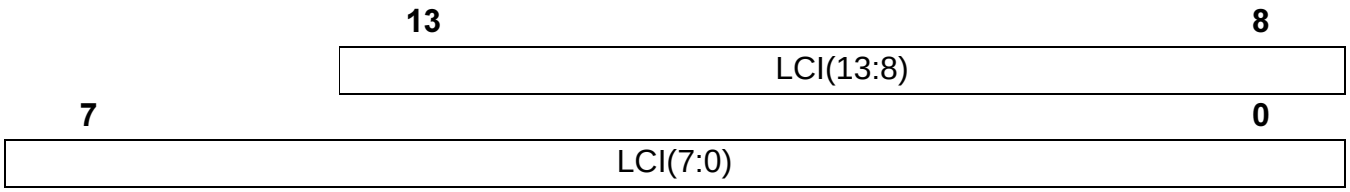
16-Bit Mode	request 4:	2_H for LCI (13:0)
	request 5:	0_H for LCI (13:0)
32-Bit Mode	request 4	2_H for LCI (13:0)
	request 5:	0_H for LCI (13:0)

LCI (13:0) Local Connection Identifier

5.4 Search Result Data Register (SLCI)

The result of searching in the memory array is the LCI value of the first line that matches the data in the SPN/SVPI/SVCI registers. This result is stored in the SLCI register. At the end of all search requests (#1..3), the ALP can read the resulting LCI from the SLCI register. For the other requests (# 4 & #5), the LCI value is set to zero.

Read Address 6_H
Value after reset undefined



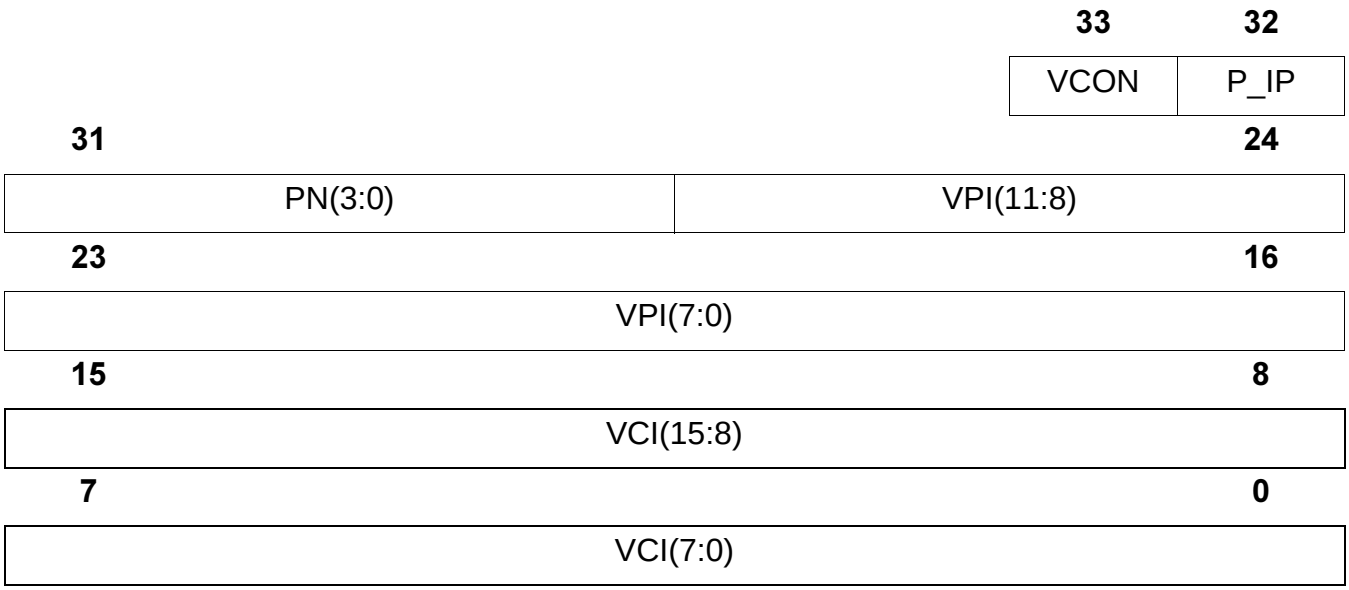
16-Bit Mode	request 1, 2, 3:	6_H for LCI (13:0)
32-Bit Mode	request 1, 2, 3:	6_H for LCI 13:0)

LCI (13:0) Local Connection Identifier

5.5 Read Data Register

These registers contain a complete entry consisting of PN/VPI/VCI, the P_IP flag and the VCON flag. The read data contained in the CAME memory line, selected with the DLCI register contents, is transferred to these registers. At the end of a read request #5, the ALP can read the resulting data from the RPN,RVPI,RVCI,RI,RV registers.

Read Address 1_H, 6_H, 9_H
Value after reset undefined



16-Bit Mode	request 5:	1_H for PN(3:0), VPI(11:0) 6_H for VCON, P_IP 9_H for VCI(15:0)
32-Bit Mode	request 5:	1_H for PN(3:0), VPI(11:0), VCI(15:0) 6_H for VCON, P_IP

VCON Valid Connection flag:

0 Connection not valid.

1 Connection valid.

P_IP Path Intermediate Point flag:

0 Address reduction is performed over PN / VPI / VCI.

1 Path Intermediate Point; address reduction is performed only over PN / VPI.

PN (3:0) Port Number

VPI (11:0) Virtual Path Identifier value of the ATM Header. PN and VPI are in a 16-bit field. Any subdivision within the 16 bits for the PN and VPI is allowed.

VCI (15:0) Virtual Channel Identifier

5.6 Description of Status Information

Status information generated by the control logic in the CAME indicates the success of commands or detected failures. At the end of each command cycle, status information about the current operation is transferred from the CAME to the ALP. The 4-bit status field consists of two bits (S3,S2) with command independent information and two bits (S1,S0) with command related details.

The data bus parity error is returned if a parity error at the data bus interface was detected by the CAME since the last completed request. In all requests, the master CAME checks whether the slave also accepted a request. This information is transferred at the Cascade Interface. If the slave signals at CO(1..0) that it has recognized no request the “cascade error” status is generated in the master (Note: if LCI 2000..3FFF$_H$ is accessed in a single CAME configuration, “cascade error” is also indicated because this case cannot be distinguished from a two-chip configuration with a defect on the second chip). A “command cycle error” is internally set after reading the status at the end of a request, or if a write access was performed while a command cycle was running.

If a parity error is detected in one of the write accesses at the start of a command, the command is discarded, internal status information is set to “parity error”, and the control logic waits for one of the two possible final bus read accesses (address #6 or #7). After the final bus read access, the CAME is ready for the next command cycle. After a command cycle is finished, the internal status contains a “command cycle error”. This status is changed with the start of a new command cycle. If the start of a command cycle is not recognized by the CAME, the error status above is still present at the next status read access.

For S3/S2 = 1/0, coding of S1/S0 depends on the command just finished in the following way: Status information can be read any time at address 6 and address 7. **figure 11** at page 35 shows the conditions under which the status information changes. The five states, named as OK, Busy, Alarm, Error(cmd), Error(parity) and shown in this figure, are coded by the status bits S3..0. The start of a request can take place in the “OK”, “Alarm”, or “Error (cascade or command cycle)” state. If a parity error is detected, the “Parity Error” state is entered. This state is left only on reading of the status information. All write accesses are ignored while the status is in “Parity Error” state. If no parity error has occurred, the command is processed. This is indicated by the “Busy” state. In this state, writing generates a “command cycle error” and no internal register is changed by the write access. Reading is allowed in “Busy” state. Depending on the result of the request, either the “OK”, “Alarm”, or “Error (cascade or command cycle)” status is entered. After reading the status once, the “Error (command cycle)” is entered. This supports the recognition of a missing command cycle start.

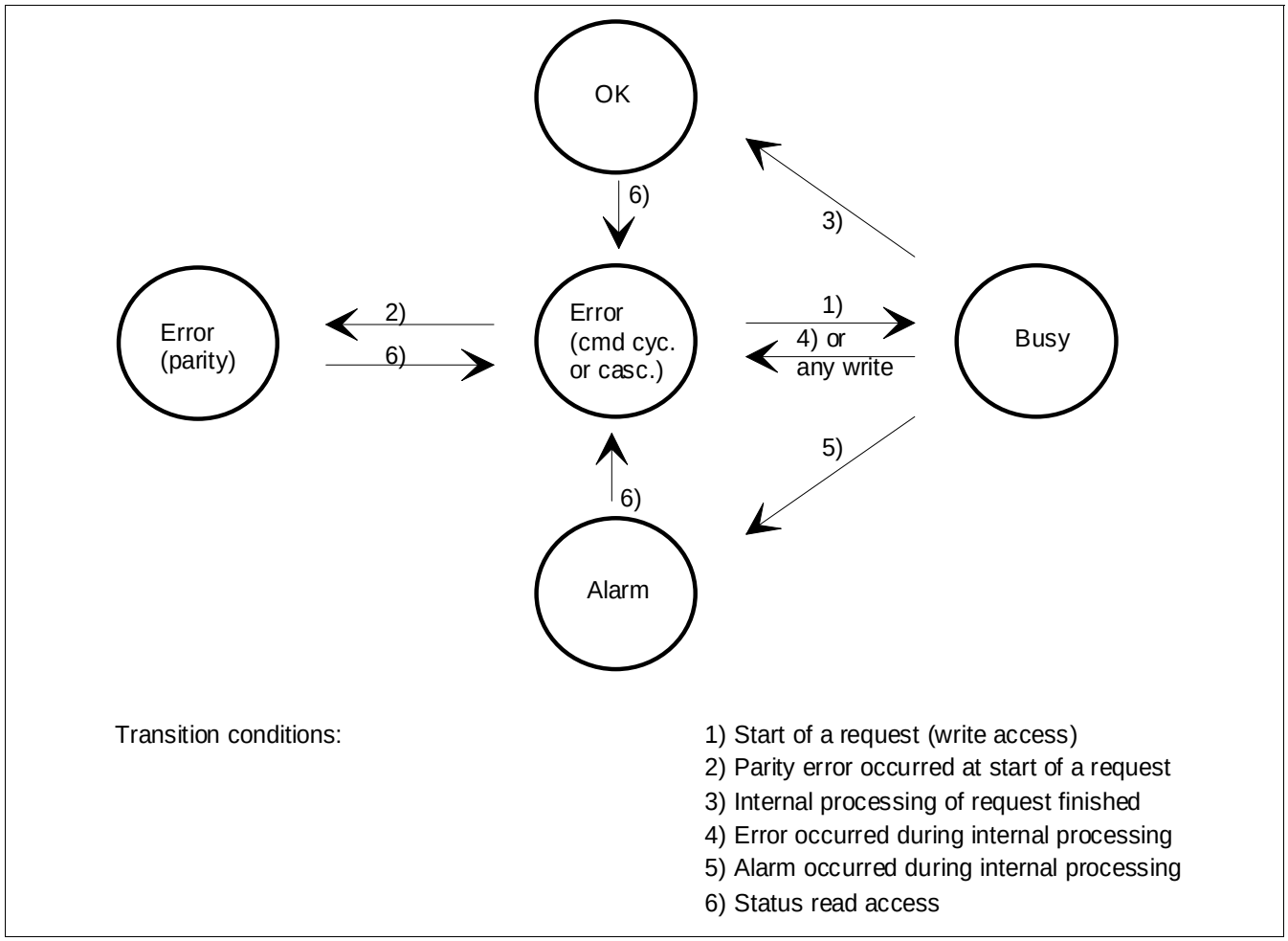


Figure 11 State Diagram of Status Generation

5.6.1 Status Register

Read Address 6_H, 7_H, E_H, F_H
Value after reset 0000_H

4			0
S3	S2	S1	S0

16-Bit Mode	request 1, 2, 3, 4, 5:	E_H for S3, S2, S1, S0
	request 6:	F_H for S3, S2, S1, S0
32-Bit Mode	request 1, 2, 3, 4, 5:	6_H for S3, S2, S1, S0
	request 6:	7_H for S3, S2, S1, S0

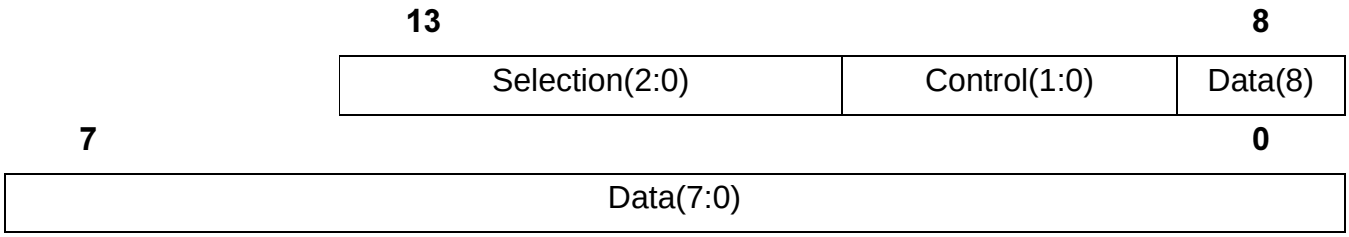
S3..0 S3 / S2 :S1/S0

00	Ok	Command was executed without problems. Indication in S1/S0: S1/S0 = 0/0.
01	Busy	Command execution is still in progress. Indication in S1/S0: S1/S0 = 0/0.
10	Alarm	Operation was not successful for CAME memory content dependent reasons. Indication in S1 / S0:
	00	Mismatch (at search requests #1..3). The search pattern was not found in any line. The LCI returned is invalid ($01FF_H$).
	01	Multimatch (at search requests #1..3). The search pattern was found in more than one line. The LCI of the lowest matching line is returned.
	10	Test search fault (at search requests #1..3). After “test search,” the search pattern was not found in all 16 blocks at the same line offset and nowhere else. The LCI returned is invalid.
	00	Refused entry (at write request #4). Attempt to write an entry to CAME which is already stored in a line of this chip (or the second CAME). This mode can be activated with MODE register bit CEE.
	01	Refused line (at write request #4). Attempt to write a valid entry in a line already containing valid information. This mode can be activated with MODE register bit CLE.
	00	Test read fault (at read request #5). The contents read from all 16 blocks at the same line offset were not equal. The read result returned is invalid.
11	Error	A hardware error was detected. Indication in S1 / S0:
	00	Data bus parity error.
	01	Cascade error.
	10	Command cycle error.

5.7 Testmode Register

The testmode register is used in the test request #6. The testmode register acts as an intermediate stage for access to the configuration (MODE, TMODE), test (TMUX) and version (VER0..3) registers which are selected by the selection field. The control field defines the read and modify-and-read operation as well as access to the master or slave device. The data field is used as MODE, TMODE, and TMUX registers as well as Version register (VER0..3) selected by the selection register.

Read/write Address 7_H
Value after reset undefined



16-Bit Mode	request 6: 7_H for TESTMODE(13:0)
3-Bit Mode	request 6: 7_H for TESTMODE(13:0)

Selection (2:0) Selection field defines which one of the eight registers is selected

000	MODE register used for Cascade Interface test, configuration of the request #3 and #4
001	TMODE register used for checking of the internal memory
010	TMUX register for test purposes only.
011	Reserved
100	Read Version number Octet 0; VER0 register used for reading
101	Read Version number Octet 1; VER1 register used for reading
110	Read Version number Octet 2; VER2 register used for reading
111	Read Version number Octet 3; VER3 register used for reading

Control (1) Control field

0	Modify and Read; not usable for selection (100:111)
1	Read

Control (0) Control field

0	Master is accessed
1	Slave is accessed

Data (8:0) Data field

5.7.1 Data Field of Testmode Register (Selection is MODE)

For request #1, the VSET portion for comparison is **internally** set to 1, VPED is set to 0 and VCED set to 1. In request #2, the settings VSET = 1, VCED = 0 and VPED = 0 are used. For request #3, all three VSET, VCED and VPED **are programmable** in the MODE register. Both modes of searching as well as searching for invalid lines are possible under microprocessor control during cell processing.

For SW convenience and acceleration of the connection data update, write request #4 may be extended by using the CEE and CLE bits in the MODE register. If CEE is set to 1 before writing a pattern to a line, searching for this pattern in the CAME (and the optional second CAME) is performed. If this pattern is already present, the command cycle is finished without writing to the line. This failure is reported in the status register. Next, if enabled, prior to writing with CLE set to 1, the destination line is checked to determine if it already contains a valid entry (with VCON = 1). Writing is prevented only if a valid pattern (VCON =1) is intended to be written over a valid entry and the failure is reported in the status field.

*Note: Command execution time varies with CEE and CLE usage. The number of clock cycles required for request processing prohibits their usage in 622 Mbit/s systems. The command execution times are listed in **table 11** on page 35.*

							8
							VCED
7							0
VPED	VSET	DPG	CIO2	CIO1	CIO0	CLE	CEE

VCED VCI Evaluation Disable.
This bit has no influence on any requests except request #3:

0 Default

1 VCI is ignored in search requests of type #3.

VPED VPI Evaluation Disable.
This bit has no influence on any requests except request #3:

0 Default

1 PN / VPI is ignored in search requests of type #3.

VSET For VCON comparison internally Set value for search request #3:

0 Free empty lines are localized.

1 Default

DPG Disturbed Parity Generation.
Generate a bus parity error in the read access at the end of this command cycle. This bit is automatically reset. DPG is not supported by the ALP!

0 Default

CIO2 CI(2) / CO(2) data
If this bit is written, it determines the setting of the CO(2) output while it is used for Cascade Interface check. If it is read, it reflects the level at the CI(2) input.

y Default
y depends on the CI input with the same index

CIO1 CI(1) / CO(1) data
If this bit is written, it determines the setting of the CO(1) output while it is used for cascade interface check. If it is read, it reflects the level at the CI(1) input.

y Default
y depends on the CI input with the same index

CIO0 CI(0) / CO(0) data
If this bit is written, it determines the setting of the CO(0) output while it is used for Cascade Interface check. If it is read, it reflects the level at the CI(0) input.

y Default
y depends on the CI input with the same index

CLE Check of a Line before write Enable.
This means writing of a valid entry (with its VCON bit set to 1) over a valid entry in memory (also with VCON bit contained in this line set to 1) is not performed; instead, in the status field, an alarm is returned. Activation of this bit prolongs the write request (restricted usage in 622 Mbit/s systems). CLE is not supported by the ALP!

0 Default

CEE Check of an Entry before write Enable.
Search is performed for occurrence of write pattern in the CAME (and a cascaded CAME, if connected). If the pattern is already present, the related line will not be updated and an alarm is returned in the status field. Activation of this bit prolongs the write request (restricted usage in 622 Mbit/s systems). CEE is not supported by the ALP!

0 Default

5.7.2 Data Field of Testmode Register (Selection is TMODE)

TMODE register use is allowed only if the MODE register is set to the default values mentioned in **section 5.7.1** on page 39. The TMODE register bits cause the following functional changes:

8			
reserved(5)			
7			**0**
reserved(4:0)	TWE	TRE	TSE

reserved (5:0) Reserved, do not activate.

000000 Default

TWE Test Write Enable.
Enables writing to all memory banks in parallel. This bit changes a write request #4 to a “test write” request.

0 Default

TRE Test Read Enable.
Enables parallel reading from all banks at the same offset. This bit changes a read request #5 to a “test read” request.

0 Default

TSE Test Search Enable.
Enables parallel comparing in all banks. This bit changes a search request #3 to a “test search” request.

0 Default

5.7.3 Data Field of Testmode Register (Selection is TMUX)

8
TMUX(8)

7	0
TMUX(7:0)	

TMUX (8:0) For test only. This register should be set to 0 for normal operation (TMUX disabled):

000000000 Default

5.7.4 Data Field of Testmode Register (Selection is VER0)

8
VER0(8)

7	0
VER0(7:0)	

VER0 (8)

0 Value

VER0 (7:0) Version number, octet 0.
Version number bits 7..0 contain $2F_H$.

5.7.5 Data Field of Testmode Register (Selection is VER1)

8
VER1(8)

7	0
VER1(7:0)	

VER1 (8)

0 Value

VER1 (7:0) Version number, octet 1.
Version number bits 15..8 contain 70_H.

5.7.6 Data Field of Testmode Register (Selection is VER2)

8
VER2(8)

7	0
VER2(7:0)	

VER2 (8)

0 Value

VER2 (7:0) Version number, octet 2.
Version number bits 23..16 contain $0B_H$.

5.7.7 Data Field of Testmode Register (Selection is VER3)

8
VER3(8)

7	0
VER3(7:0)	

VER3 (8)

0 Value

VER3 (7:0) Version number, octet 3.
Version number bits 31..24 contain $0B_H$.

6 Interface Description

6.1 Data Bus and Address Bus Interface

All communication with ALP is done using the data interface. The data interface consists of the following signals, as shown in **table 1**:

Table 1 Data Interface Signals

Signal Name	Explanation	Type
DAT(0)	Odd parity. Selected to create parity over ADR and DAT	bidirectional
DAT(31..1)[1)]	Data Bus	bidirectional
DAT(32)	Data Bus	bidirectional
ADR(2..0)	Address Bus	input
ADR(3)	Address Bus	input
$\overline{WE}$	Write Enable	input
$\overline{OE}$	Output Enable	input
$\overline{CE}$	Chip Enable	input
CLK	Clock	input
$\overline{EN16}$	Selection of bus width	input

[1)] DAT(15:1) are needed with ALP V1.1. DAT(32:17) are reserved for future use.

CAME will be accessed only if $\overline{CE}$ is low at the rising edge of CLK. If $\overline{WE}$ is low at the time, a write cycle will be executed; if $\overline{WE}$ is high, a read cycle will be executed. The $\overline{OE}$ signal controls the CAME output buffers for read accesses only. The $\overline{EN16}$ signal determines data bus width, which is 16-bit for $\overline{EN16}$ at low level, and 32-bit otherwise. This signal is intended for static adjustment of bus width.

Parity generation in 16-bit Mode extends over DAT(16..0) and ADR(3..0). In 32-bit Mode, it extends over DAT(32..0) and ADR(3..0). In 32-bit interface mode, ADR(3) is not needed and must be connected to ground; thus, parity generated over DAT(32..0) and ADR(2..0) is accepted correctly. In both cases, DAT(0) is used as a parity line and completes the corresponding DAT and ADR lines to odd parity. In 16-bit Mode, only the lower part of the data bus is used. The upper bus half (index 17..32) is ignored during write accesses to CAME and is 0 during read accesses.

6.2 Cascade Interface

For more demanding applications, two CAME chips can be cascaded to build up one virtual device with double capacity and the identical physical bus interface to an external controller. The Cascade Interface is used for this purpose and consists of the CO(2..0) outputs and the CI(2..0) and CA inputs as shown in **figure 12**.

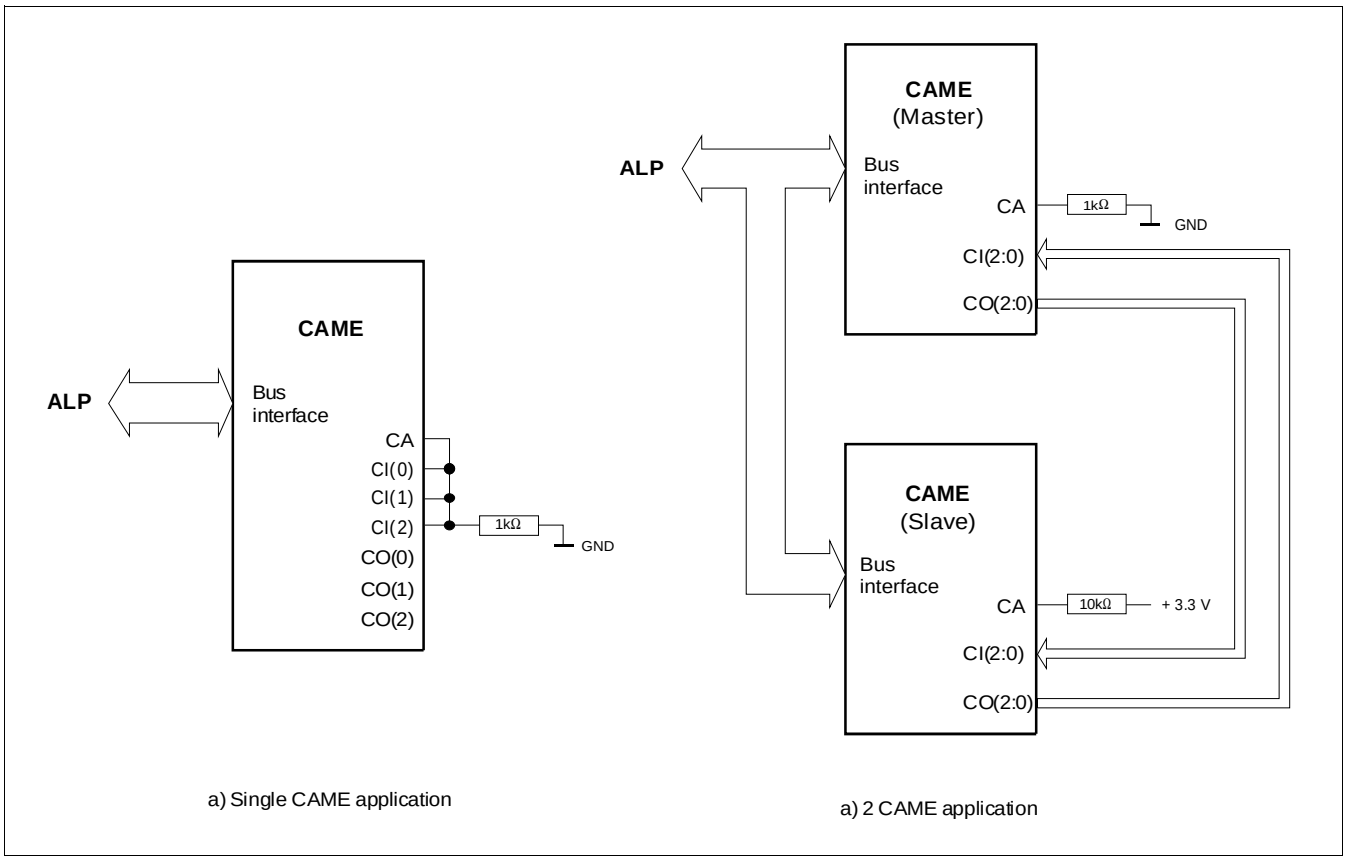


Figure 12 Cascade Interface - Interconnection of 2 CAME Chips

Both CAME chips receive the same requests from ALP. Depending on the request, the determination of which chip may answer at the end of the request is either known in advance (read, write and test requests #4..6) or results from the operation (search requests #1..3). In the second case, the master must inform the slave of its search result and indicate whether or not it processes the search request. The same report takes place from the slave to the master. This is done with the signals CO(1..0). Processing the crosswise transferred status information is done according to **table 4**. The timing of this transfer is defined in **table 15**. The interpretation of the CO(1..0) signals at this time is done according to **table 2**.

In order to avoid bus conflicts on reading of cascaded CAME chips, the master has the opportunity to disable data output of the slave CAME using the CO(2) signal. This signal is important in case of a parity error, for example.

The CO(2..0) outputs must be connected to the CI(2..0) inputs of the opposite CAME.

For single chip applications, the CAME device must be configured as master by CA and the CI(1..0) inputs must be supplied with low level, pretending an “always mismatch” condition of the non-existent slave. The CI(2) input is not evaluated by a chip configured as master, but it needs connection to ground.

Table 2 Cascade Interface Signals

Signal Name	Code	Function	Type
CA	0	Device is master, its LCI range is 0..8191	input
	1	Device is slave, its LCI range is 8192..16383	
CI(1..0)	00	A search request (#1..3 or #4 with MODE.CEE= 1) is running with the result mismatch on the opposite chip	input
	01	A search request (#1..3 or #4 with MODE.CEE= 1) is running with the result of single match or multimatch on the opposite chip	
	10	No request is processed by the opposite chip	
	11	Request #4..6 is processed by the opposite chip	
CI(2)	0	CI(2) is ignored by a master. A slave interprets CI(2) as follows: Data output at DAT is prohibited in read cycles	input
	1	Data output at DAT is allowed in read cycles	
CO(1..0)	00	A search request (#1..3 or #4 with MODE.CEE= 1) is running with the result mismatch	output
	01	A search request (#1..3 or #4 with MODE.CEE= 1) is running with the result of single match or multimatch	
	10	No request is processed	
	11	Request #4..6 is processed	
CO(2)	0	CO(2) of a slave is undefined.A master outputs CO(2) as follows: Prohibit data output of a slave in read cycles	output
	1	Allow data output of a slave in read cycles	

6.2.1 Cascade Logic

If two CAME chips are cascaded, the selection of which device will react and may respond is made based on the command started. No additional preparation at the bus interface is necessary. In read or write command cycles, the LCI - at least part of the command word -

determines which chip performs the operations and may send back the results to ALP. Therefore, the chip not selected chip must also wait for the end of the current request before a new request may be started. In search cycles, both CAME chips start searching in parallel. Only one chip will respond to ALP, determined by the search result. Only for test request #6 must an extra bit, TESTMODE(9), be spent in the instruction word for selection between master and slave.

Table 3 Selection Criteria for Different Instructions

Command Type	Selection of Master	Selection of Slave
Search - Requests #1..3	Refer to table 4	
Write - Request #4	0 ≤ LCI ≤ 8191	8192 ≤ LCI ≤ 16383
Read - Request #5	0 ≤ LCI ≤ 8191	8192 ≤ LCI ≤ 16383
Test - Request #6	TESTMODE(9) = 0	TESTMODE(9) = 1

With two cascaded CAME chips, each CAME first searches alone. When the match state of master and slave is known, the master reports his local result to the slave. It is only necessary to report “mismatch” or “not mismatch” conditions. The same is done by the slave. Both chips determine their reaction and the overall status according to **table 4**, which includes all combinations of local master and slave search results. The fields of this table contain the overall status of the result for which device returns the result to ALP and which stays inactive.

For example, if both chips detect a single match, the slave knows about its own state and the detection of at least an additional match in the master (Master.CO(2..0) = Slave.CI(2..0)) and knows that a global multimatch results. As the slave in this case, it must not respond to ALP. The master also detects a global multimatch the same way (Slave.CO(2..0) = Master.CI(2..0)) and responds to ALP.

Table 4 Responding Device and Overall Result after Search Operation

	Master Device		
	Mismatch Master.CO(1..0) = 00	Single Match Master.CO(1..0) = 01	Multimatch Master.CO(1..0) = 01
Slave Device			
Mismatch Slave.CO(1..0) = 00	Master: Mismatch Slave: inactive	Master: Single Match Slave: inactive	Master: Multimatch Slave: inactive
Single Match Slave.CO(1..0) = 01	Master: inactive Slave: Single Match	Master: Multimatch Slave: inactive	Master: Multimatch Slave: inactive
Multimatch Slave.CO(1..0) = 01	Master: inactive Slave: Multimatch	Master: Multimatch Slave: inactive	Master: Multimatch Slave: inactive

In summary, the condition for the CAME to become active at the end of an error-free search cycle is:

If the Slave receives 00 for “Mismatch” on CI(1..0) and recognizes an internal “Single Match” or “Multimatch” condition it may respond to the master; it must not respond in all other cases.

A master will not respond at the end of the current command cycle only if it detects an internal “Mismatch” condition and the slave reports at CI(1..0) with 01 no “Mismatch”; in all other cases the master responds.

In the case of a communication fault at the beginning of a request, the determination of which chip may respond is not performed. The reason may be a parity error. To avoid bus conflicts, the slave always must be controlled by the master chip for data output in case of reading. This is done by the master with the CO(2) signal.

If the slave outputs the codes 10 (no request processed) or 11 (request #4..6 processed) at CO(1..0) while the master processes a search request, the overall status “cascade error” is reported by the master.

If the master processes one of the requests without searching, then only if the slave outputs the code 10 (no request processed) is the overall status “cascade error”. In the other cases, no error is recognized. The code 00 from a slave is accepted intentionally, even if it pretends a search operation, because, for non-cascaded applications, the CI(2..0) inputs are connected to ground.

Finally, if the master holds the internal status “data bus parity error” or “command cycle error,” no request is processed by the master. In this case, the slave status is ignored.

This behavior is summarized in **table 5**. The master will always report the cascade, parity, and command cycle errors.

Table 5 Overall Status in Case of Errors

	Master CO(1..0) = 00 or 01 (requests with searching)	CO(1..0) = 11 (requests without searching)	CO(1..0) = 10 (No request processed)
Slave CO(1..0) = 00 or 01	See table 4	Status of read, write and test requests	Parity or command cycle error
CO(1..0) = 11	Cascade error	Reported by the pre-selected device	Parity or command cycle error
CO(1..0) = 10	Cascade error	Cascade error	Parity or command cycle error

6.3 Clock and Reset

The system clock is passed to CAME at the CLK input. For typical applications, it will be equal to ALP SYS_CLK/2 = 25.92 MHz. This is the only clock supply for the CAME (if the BSCAN interface clock is ignored). It determines operation of the bus interface and the timing of all clocked internal functions. The ALP delivers the CLK signal for the CAME without any glue logic, as depicted in **figure 13**.

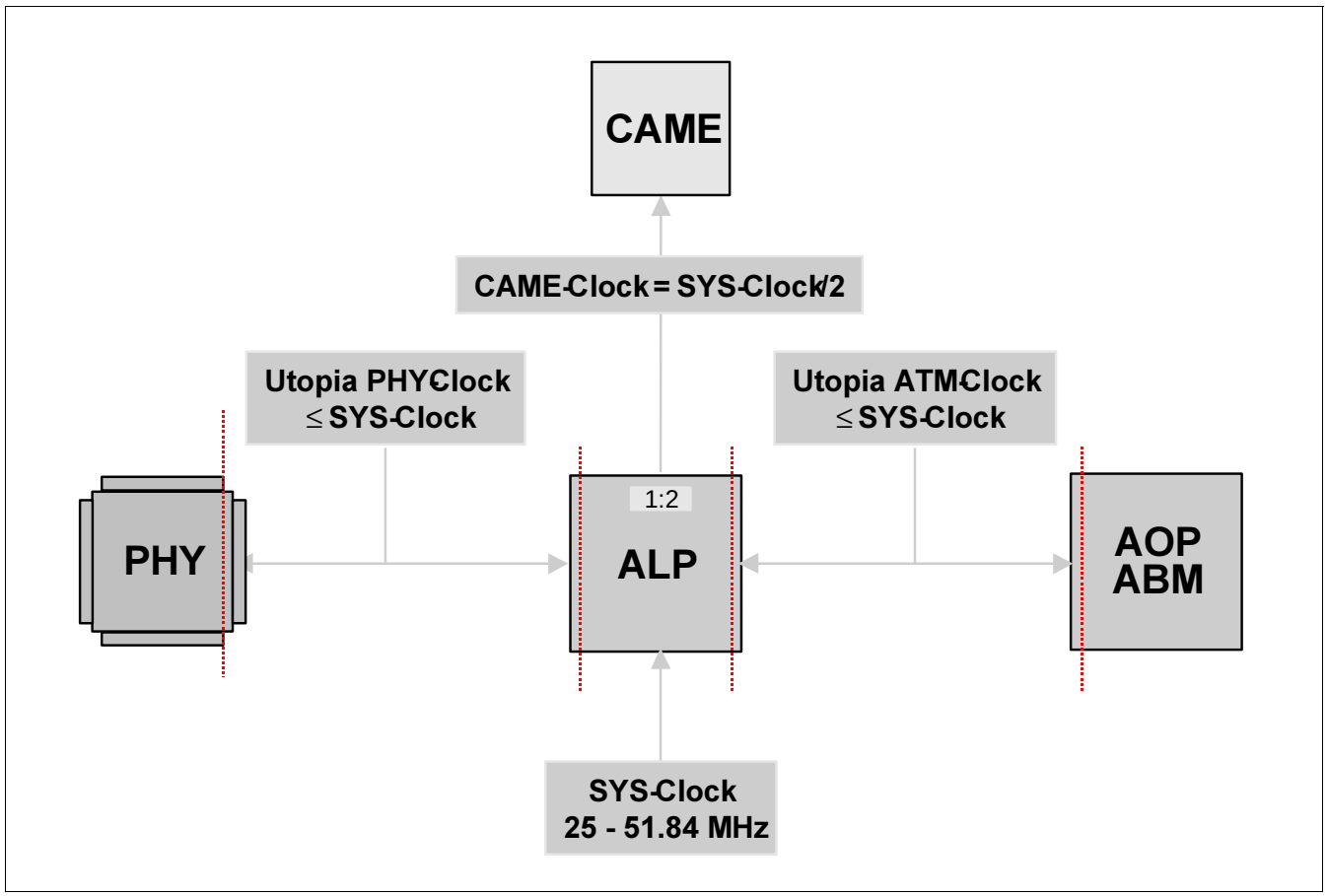


Figure 13 Clock Interface of the CAME

The $\overline{\text{RESET}}$ signal is an active low input. As long as it is connected to a low level, the data bus DAT(32..0) will be forced to a high-impedance state, CO(2..0) are set to 000. TDO and TMD(7..0) are not influenced.

When the transition low → high is detected at $\overline{\text{RESET}}$, the internal control logic is reset, the internal status is “ok” and all test function registers are set to their default values as outlined in section 5.7 on page 37. Thus, test multiplexer selection and the CO(2..0) outputs are influenced. Internal registers around the memory array are also cleared. The contents of the memory array are not changed intentionally, but memory protection during reset is not implemented.

As long as $\overline{\text{RESET}}$ stays at a high level, normal operation will occur.

6.4 Boundary Scan Interface

Factory test is supported by the Boundary Scan Interface. It consists of four inputs for control of the TAP-controller and one output described in table 6. The TAP-controller is a part of the BSCAN logic.

Table 6 Boundary Scan Interface

Signal	Explanation
TCK	Clock input
TDI	Serial Data Input, accepted with rising TCK edge
TDO	Serial Data Output, changes with falling TCK edge
TMS	Test Mode Select signal, accepted with rising TCK edge, defines TAP controller operation mode.
$\overline{\text{TRST}}$	Test interface Reset signal, low level initializes the TAP-controller asynchronously

According to IEEE-Standard 1149.1, boundary scan also provides a 32-bit identification register. In CAME, it contains the boundary scan ID number $0B0B702F_H$.

Table 7 CAME Boundary Scan Table

Boundary Scan Number	PIN-Nr.	Signal Name	Type
1	12	ADR(0)	I
2	14	ADR(1)	I
3	16	ADR(2)	I
4	18	ADR(3)	I
5	20	$\overline{\text{RES}}$	I
6	22	$\overline{\text{WE}}$	I
7	24	$\overline{\text{OE}}$	I
8	26	$\overline{\text{CS}}$	I
9	32	DAT(0)	O
10	32	DAT(0)	I
11	34	DAT(1)	O
12	34	DAT(1)	I

Table 7 CAME Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal Name	Type
13	36	DAT(2)	O
14	36	DAT(2)	I
15	38	DAT(3)	O
16	38	DAT(3)	I
17	40	DAT(4)	O
18	40	DAT(4)	I
19	42	DAT(5)	O
20	42	DAT(5)	I
21	44	DAT(6)	O
22	44	DAT(6)	I
23	46	DAT(7)	O
24	46	DAT(7)	I
25	48	DAT(8)	O
26	48	DAT(8)	I
27	50	DAT(9)	O
28	50	DAT(9)	I
29	52	DAT(10)	O
30	52	DAT(10)	I
31	54	CLK	I
32	-	Control pad for DAT(32:0)	-
33	56	DAT(11)	O
34	56	DAT(11)	I
35	58	DAT(12)	O
36	58	DAT(12)	I
37	60	DAT(13)	O
38	60	DAT(13)	I

Table 7 CAME Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal Name	Type
39	62	DAT(14)	O
40	62	DAT(14)	I
41	64	DAT(15)	O
42	64	DAT(15)	I
43	66	DAT(16)	O
44	66	DAT(16)	I
45	68	DAT(17)	O
46	68	DAT(17)	I
47	70	DAT(18)	O
48	70	DAT(18)	I
49	72	DAT(19)	O
50	72	DAT(19)	I
51	74	DAT(20)	O
52	74	DAT(20)	I
53	76	DAT(21)	O
54	76	DAT(21)	I
55	77	DAT(22)	O
56	77	DAT(22)	I
57	81	DAT(23)	O
58	81	DAT(23)	I
59	83	DAT(24)	O
60	83	DAT(24)	I
61	85	DAT(25)	O
62	85	DAT(25)	I
63	87	DAT(26)	O
64	87	DAT(26)	I

Table 7 CAME Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal Name	Type
65	89	DAT(27)	O
66	89	DAT(27)	I
67	91	DAT(28)	O
68	91	DAT(28)	I
69	93	DAT(29)	O
70	93	DAT(29)	I
71	95	DAT(30)	O
72	95	DAT(30)	I
73	97	DAT(31)	O
74	97	DAT(31)	I
75	99	DAT(32)	O
76	99	DAT(32)	I
77	104	CA	I
78	106	$\overline{\text{EN16}}$	I
79	109	TMD(0)	O
80	113	TMD(1)	O
81	115	TMD(2)	O
82	117	TMD(3)	O
83	119	TMD(4)	O
84	121	TMD(5)	O
85	123	TMD(6)	O
86	125	TMD(7)	O
87	127	CO(0)	O
88	129	CO(1)	O
89	131	CO(2)	O
90	133	CI(0)	I

Table 7 CAME Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal Name	Type
91	135	CI(1)	I
92	137	CI(2)	I

6.5 Microprocessor and Control Interface

No Microprocessor Interface is implemented in the CAME. In the CAME, data and control interfaces are identical. For the interface description, refer to "Data Bus and Address Bus Interface" on page 6-45.

The CAME mode register access takes place with request #6. For details about command transfer, refer to **section 5.7,** page 37.

6.6 Reference for Internal Current Sources

Adjustment of internal current sources is done using the RBIAS and VBIAS pins. VBIAS must be connected to a precision voltage reference with 1.2 V ± 10%. Additionally, between the RBIAS pin and ground, a resistor with 12.1 kΩ ± 1% is necessary.

VBIAS= 1 is interpreted as "powerdown" and disables the CAME functionality.

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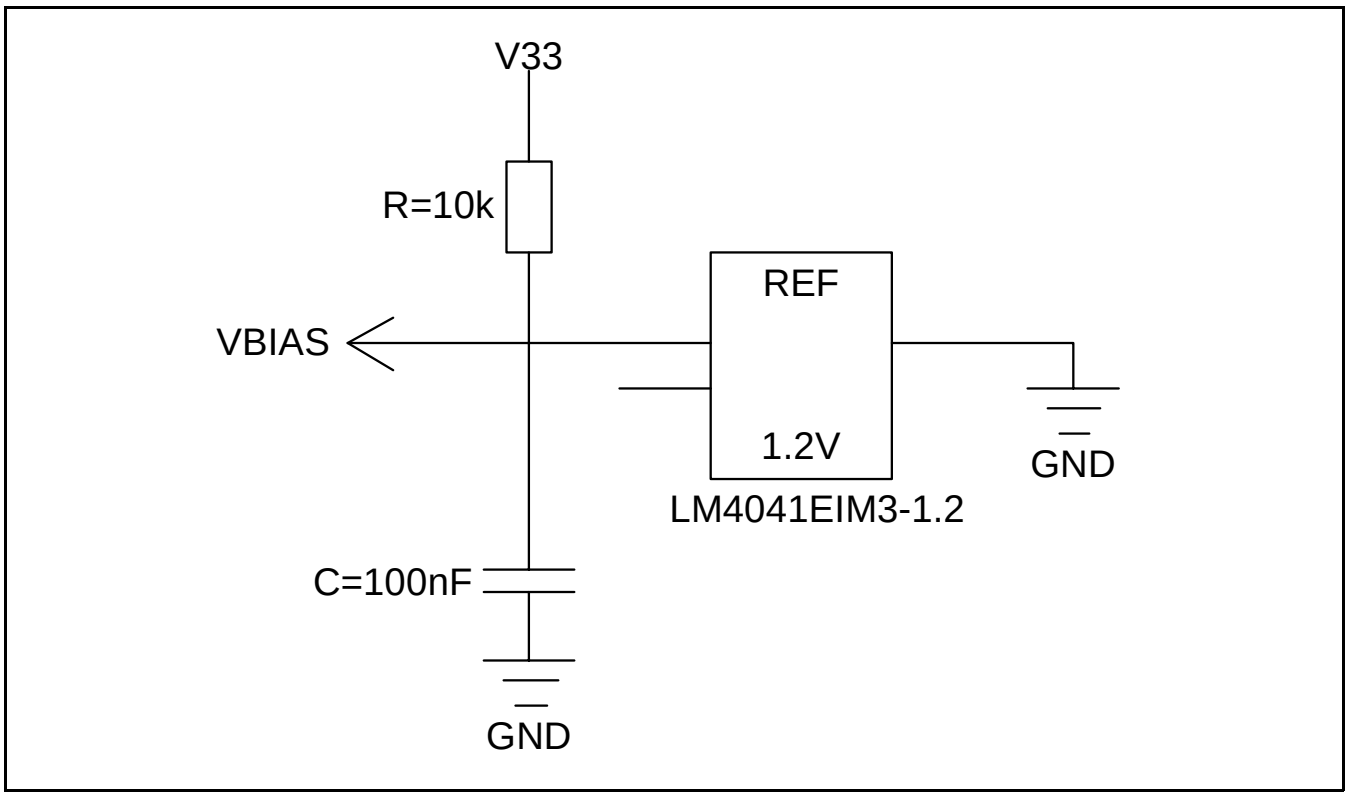


Figure 14 Example for VBIAS Reference Voltage Circuit

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply Voltage	V_{CC}	-0.5 to 4.6	V
Input Voltage	V_{IN}	-0.5 to V_{CC}+0.5	V
Output Voltage	V_{OUT}		V
Power Dissipation	P_V	<0.3	W
Storage Temperature	T_S	-65 to 150	°C

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Conditions

Table 9 Operating Conditions

Parameter	Symbol	Limit Values	Unit
Supply Voltage	V_{CC}	3.135 to 3.465	V
Ground	*GND*	0	V
Input Voltage	V_{IN}	0 to V_{CC}	V
Output Voltage	V_{OUT}	0 to V_{CC}	V
Input low Voltage	V_{IN}	0 to 0.8	V
Input high Voltage	V_{IN}	2.0 to V_{CC}	V
Ambient Temperature	T_A	0 to 70	°C
Junction Temperature	T_J	max. 100	°C

7.3 DC Characteristics for all Interfaces

Table 10 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	
Output High Voltage	V_{OH}	2.4			V	$V_{OH}=V_{DD}$ or V_{SS}
Output Current at high Voltage	I_{OH}	-8			mA	$V_{IN}=V_{CC}$ or 0 V
Output Current at low Voltage	I_{OL}			8	mA	$V_{IN}=V_{CC}$ or 0 V
Input Leakage Current at low Voltage (all inputs except TCK, TMS, TDI, TRSTN)	I_{IL}	-1		1	mA	$V_{IN}=V_{CC}$ or 0 V
Input Leakage Current at high Voltage (all inputs except TCK, TMS, TDI, TRSTN)	I_{IH}	-1		1	mA	$V_{IN}=V_{CC}$ or 0 V
Input Leakage Current at low Voltage (inputs TCK, TMS, TDI, TRSTN)	I_{IL}	-1		-14	mA	V_{IN}=0 V
Input Leakage Current at high Voltage (inputs TCK, TMS, TDI, TRSTN)	I_{IH}	-1		1	mA	$V_{IN}=V_{CC}$

7.4 Capacitances

Table 11 Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance	C_{IN}		5	pF
Input/Output Capacitance	$C_{IN/OUT}$		7	pF

7.5 AC Characteristics

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 5%, V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical 1
and to V_{IL} = 0.4 V for a logical 0

All outputs are measured at V_H = 2.0 V for a logical 1
and at V_L = 0.8 V for a logical 0

The AC testing input/output waveforms are shown in **figure 15**.

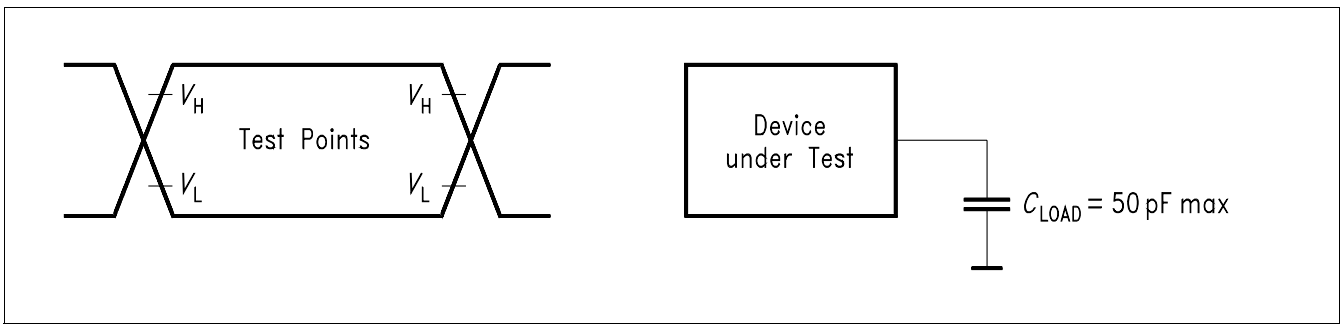


Figure 15 Input/Output Waveform for AC Measurements

7.5.1 Boundary-Scan Test Interface

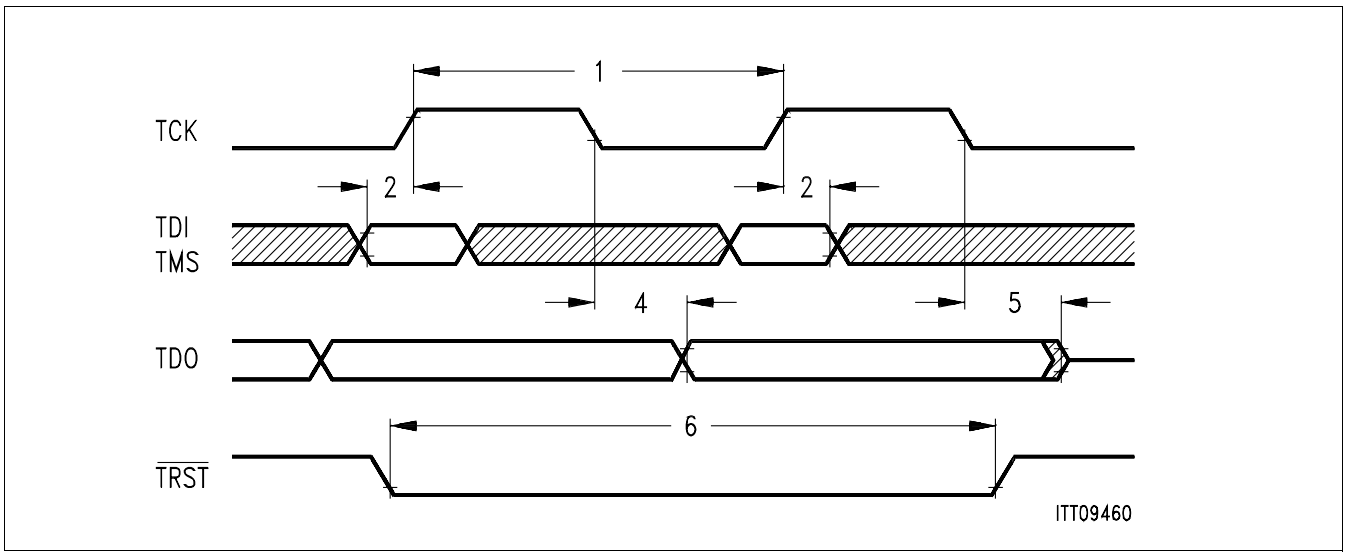


Figure 16 Boundary-Scan Test Interface Timing Diagram

Table 12 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{TCK}: Period TCK	160			ns
1A	F_{TCK}: Frequency TCK	0		6.25	MHz
2	Set up time TMS, TDI before TCK rising	10			ns
3	Hold time TMS, TDI after TCK rising	10			ns
4	Delay TCK falling to TDO valid	0		30	ns
5	Delay TCK falling to TDO high impedance	0		30	ns
6	Pulse width $\overline{\text{TRST}}$ low	100			ns

7.5.2 AC Characteristics of CAME Data Interface to the ALP

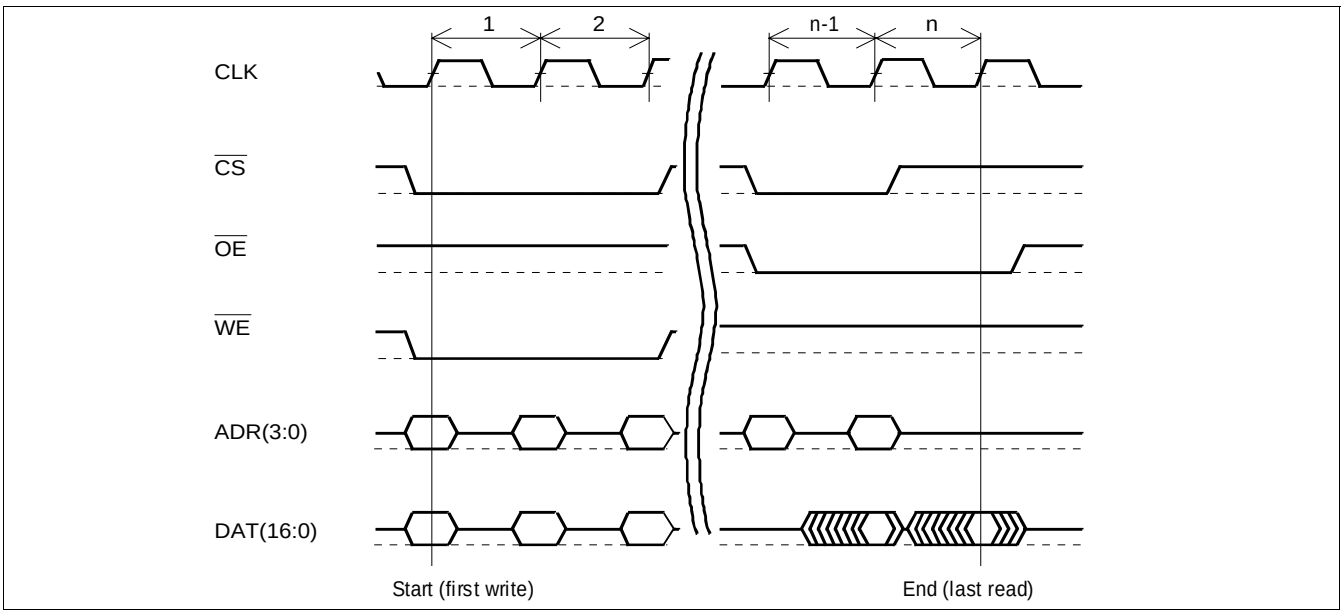


Figure 17 Example of Execution Timing for Write Command (Request #4)

Table 13 Duration of Command Execution

Parameter	Max. execution time		Unit
	for 32-bit interface	for 16-bit interface	
Request number 1: Cell processing search for PN/VPI reduction	12	13	clock cycles
Request number 2: Cell processing search for, PN/VPI/VCI reduction	12	14	clock cycles
Request number 3: Search request by the microprocessor	12	14	clock cycles
Request number 4: CAME Write command	8	10[1)]	clock cycles
Extended modes:			
MODE.CEE = 0, MODE.CLE = 1	12	14	clock cycles
MODE.CEE = 1, MODE.CLE = 0	14	16	clock cycles
MODE.CEE = 1, MODE.CLE = 1	16	18	clock cycles
Request number 5: CAME Read command	11	13	clock cycles
Request number 6: Test and configuration of the CAME	8	9	clock cycles

1) Only this mode is selected by the ALP PXB 4350 E.

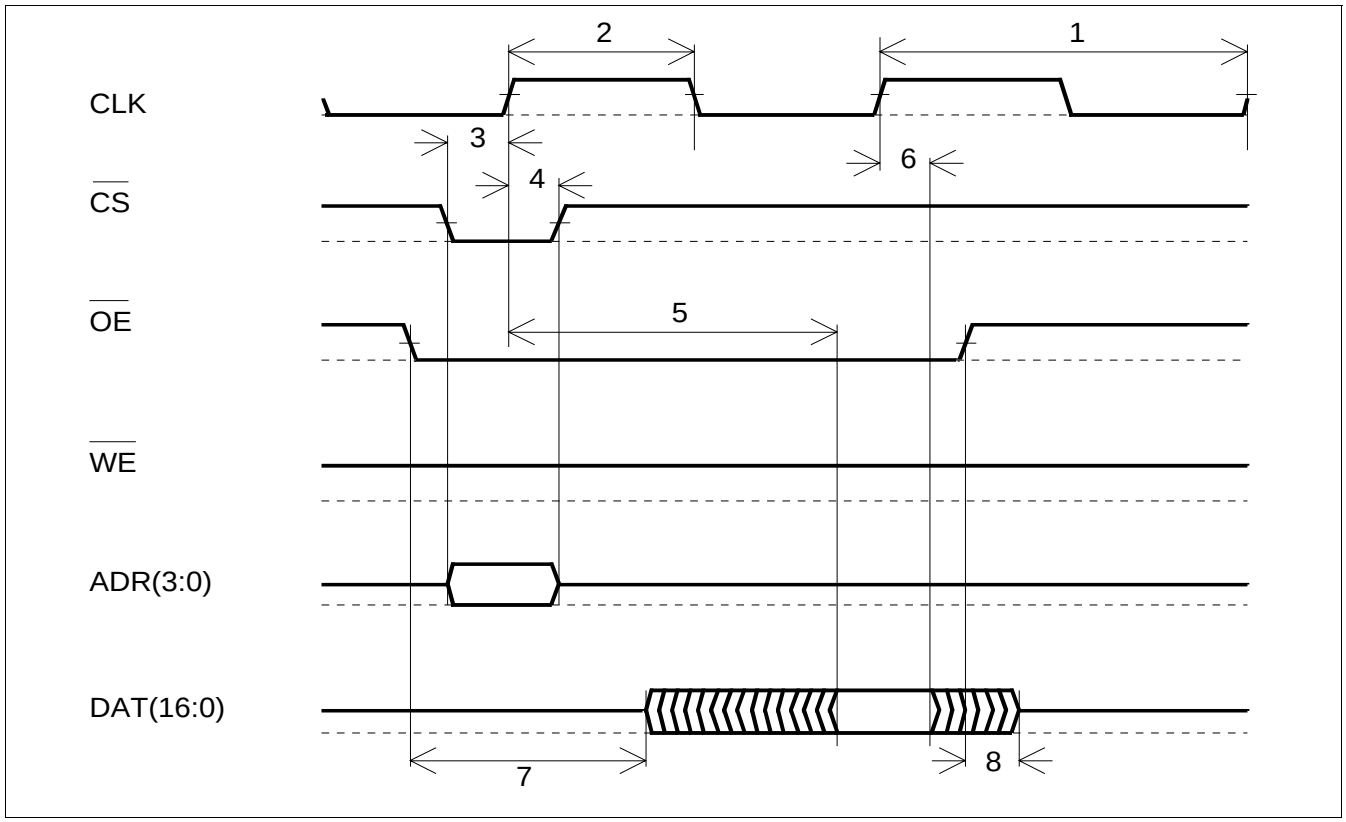


Figure 18 CAME Read Cycle

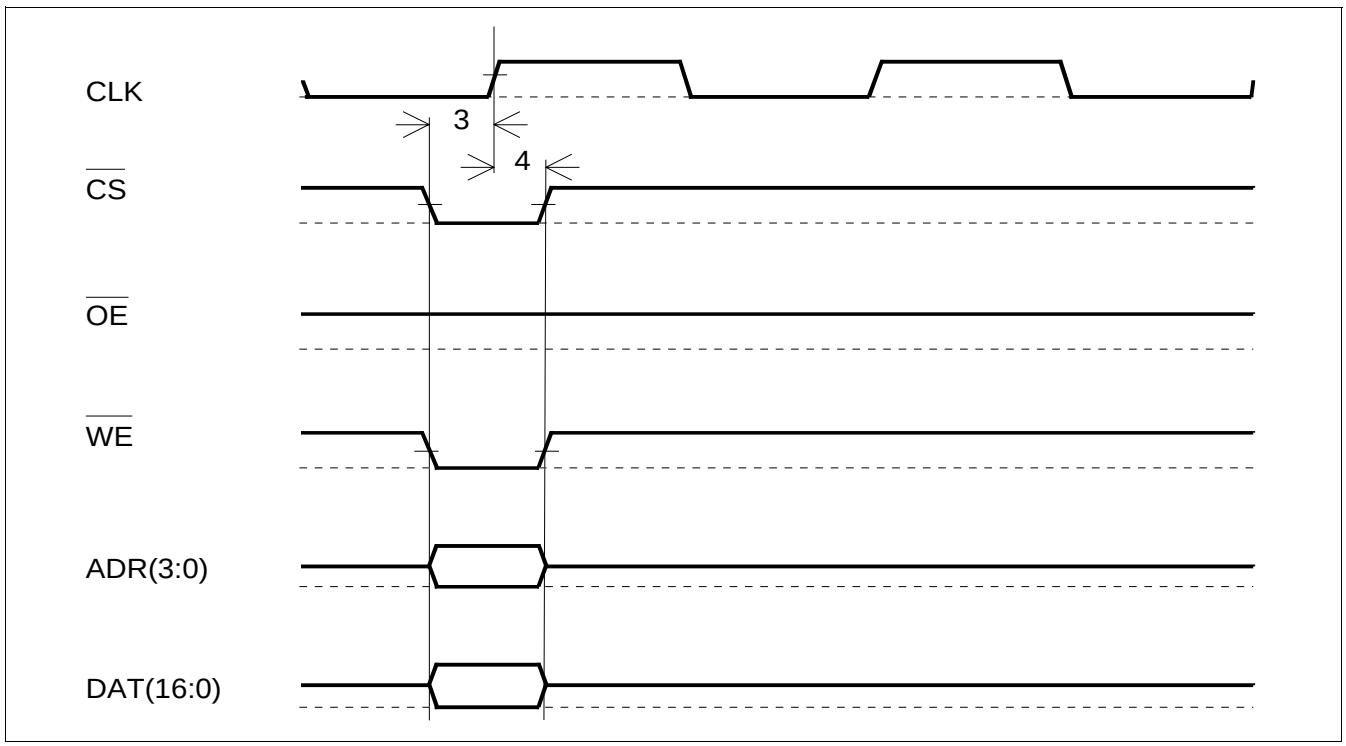


Figure 19 CAME Write Cycle

Table 14 Parameters for Read/Write Access

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	CLK frequency	0.01		25.92	MHz
2	CLK duty cycle	40		60	%
3	Set up time of $\overline{CS}$, $\overline{WE}$, ADR and DAT in read and write cycle to CLK ↑	4			ns
4	Hold time of $\overline{CS}$, $\overline{WE}$, ADR and DAT in read and write cycle from CLK ↑	4			ns
5a[1)]	Data access of DAT in read cycle from CLK ↑ (32-bit access)			35	ns
5b[1)]	Data access of DAT in read cycle from CLK ↑ (16-bit access)			19	ns
6	Data hold of DAT in read cycle from CLK ↑	4			ns
7	$\overline{OE}$ low of DAT in read cycle to Output active			21	ns
8	$\overline{OE}$ high of DAT in read cycle to Output Z			21	ns

[1)] The ALP PXB 4350 E uses only the 16-bit access

7.5.3 AC Characteristics of CAME Cascade Interface

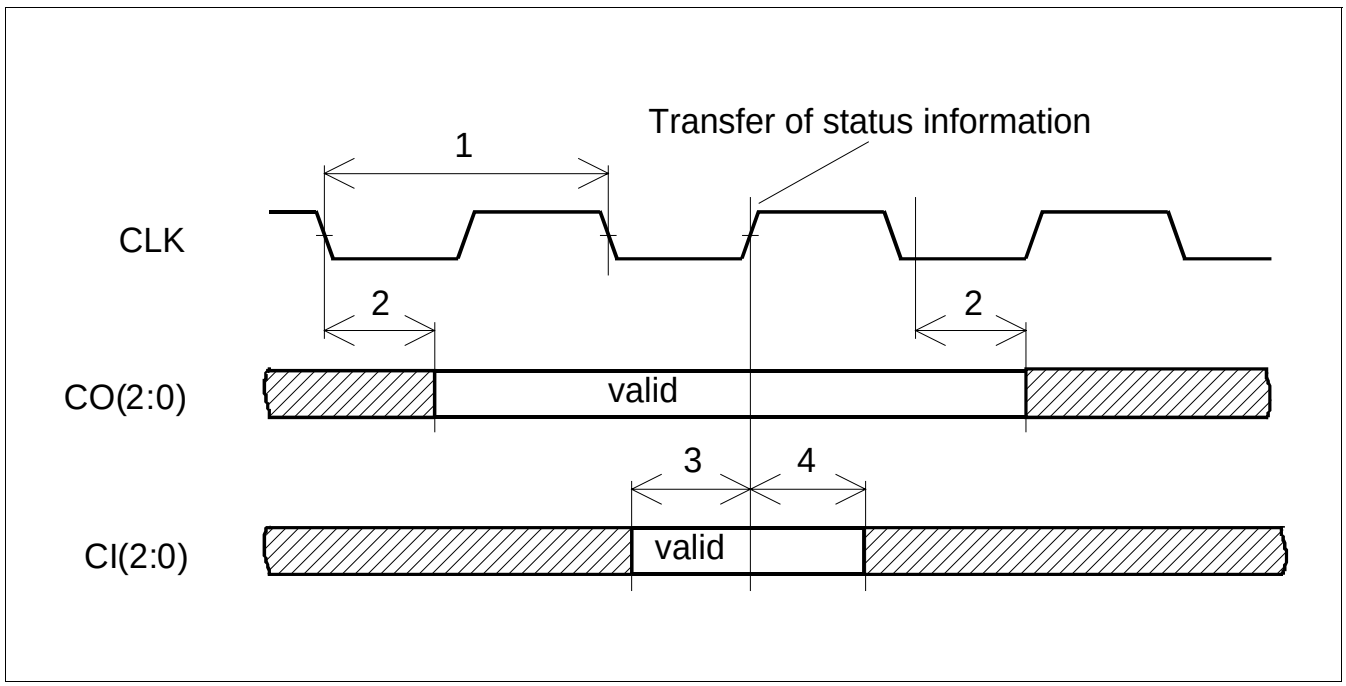


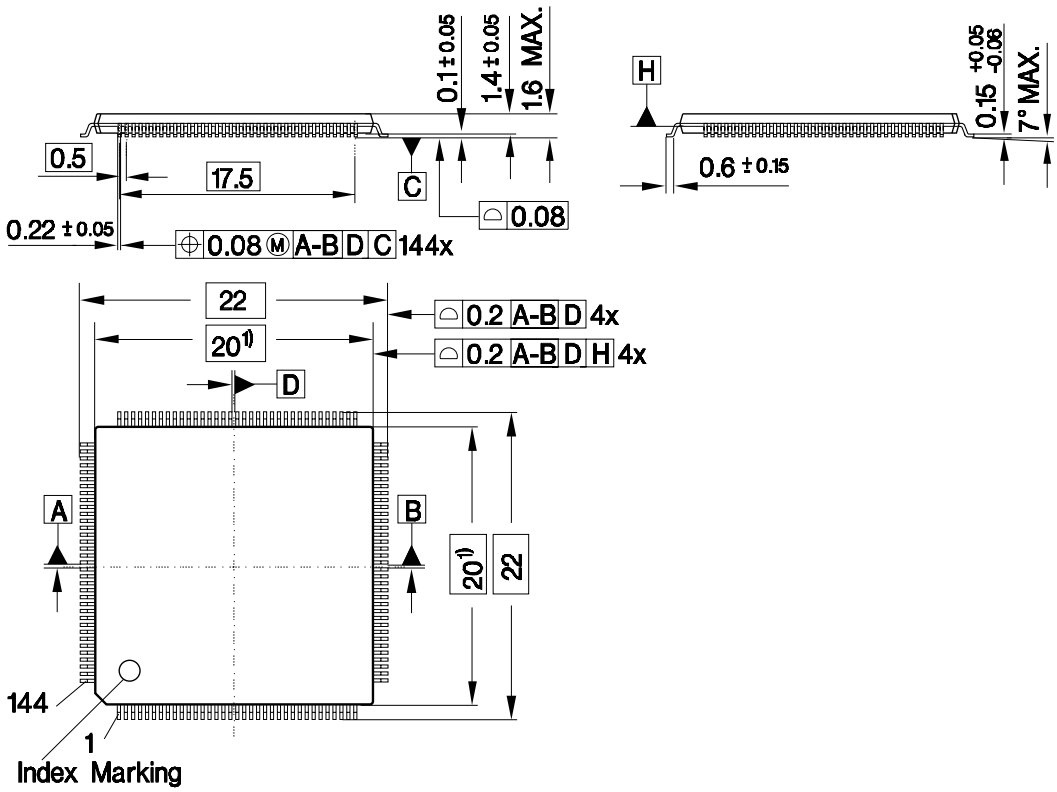
Figure 20 Timing of Cascade Interface

Table 15 Cascade Interface Timing Parameters

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	CLK frequency	0.01		25.92	MHz
2	CO change from CLK ↓			22	ns
3	Set up time to CLK ↑	17			ns
4	Hold time from CLK ↑	2			ns

8 Package Outlines

TQFP-144
(144 pin Thin Plastic Quad Flatpack)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 21 Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

9 References

1. Joint Test Action Group JTAG standard IEEE Std. 1149.1

10 Acronyms

ABM	PXB 4330 E **A**TM **B**uffer **M**anager
ALP	PXB 4350 E **A**TM **L**ayer **P**rocessor
AOP	PXB 4340 E **A**TM **O**AM **P**rocessor
ARC	**A**ddress **R**eduction **C**ircuit
byte	octet = 8 bits
CAME	**C**ontent **A**ddressable **M**emory **E**lement
double word	32 bits
F4	Virtual Path Layer
F5	Virtual Channel Layer
HT	**H**eader **T**ranslation
I/O	**I**nput/**O**utput
IP	**I**ntermediate **P**oint
LCI	**L**ocal **C**onnection **I**dentifier
LSB	**L**east **S**ignificant **B**it
octet	byte = 8 bits
OAM	**O**peration **A**nd **M**aintenance
PN	**P**ort **N**umber
SSRAM	**S**ynchronous **S**tatic **R**andom **A**ccess **M**emory
tbd	**t**o **b**e **d**efined
TEP	**T**erminating **E**nd **P**oint
VCC	**V**irtual **C**hannel **C**onnection
VCI	**V**irtual **C**hannel **I**dentifier of standardized ATM cell
VP-	**V**irtual **P**ath specific
VPC	**V**irtual **P**ath **C**onnection
VPI	**V**irtual **P**ath **I**dentifier of standardized ATM cell
word	16 bits