



PN532/C1

Near Field Communication (NFC) controller

Rev. 3.2 — 20 September 2012
120132

Product short data sheet
COMPANY PUBLIC

1. General description

The PN532 is a highly integrated transceiver module for contactless communication at 13.56 MHz based on the 80C51 microcontroller core. It supports 6 different operating modes:

- ISO/IEC 14443A/MIFARE Reader/Writer
- FeliCa Reader/Writer
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE Card MIFARE Classic 1K or MIFARE Classic 4K card emulation mode
- FeliCa Card emulation
- ISO/IEC 18092, ECMA 340 Peer-to-Peer

The PN532 implements a demodulator and decoder for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The PN532 handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The PN532 supports MIFARE Classic 1K or MIFARE Classic 4K card emulation mode. The PN532 supports contactless communication using MIFARE Higher transfer speeds up to 424 kbit/s in both directions.

The PN532 can demodulate and decode FeliCa coded signals. The PN532 handles the FeliCa framing and error detection. The PN532 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The PN532 supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision. This must be implemented in firmware as well as upper layers.

In card emulation mode, the PN532 is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The PN532 generates the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S²C interface.

Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the PN532 offers the possibility to communicate to another NFCIP-1 compliant device, at transfer speeds up to 424 kbit/s. The PN532 handles the complete NFCIP-1 framing and error detection.

The PN532 transceiver can be connected to an external antenna for Reader/Writer or Card/PICC modes, without any additional active component.



The PN532 supports the following host interfaces:

- SPI
- I²C
- High Speed UART (HSU)

An embedded low-dropout voltage regulator allows the device to be connected directly to a battery. In addition, a power switch is included to supply power to a secure IC.

2. Features and benefits

- 80C51 microcontroller core with 40 KB ROM and 1 KB RAM
- Highly integrated demodulator and decoder
- Buffered output drivers to connect an antenna with minimum number of external components
- Integrated RF level detector
- Integrated data mode detector
- Supports ISO/IEC 14443A/MIFARE
- Supports ISO/IEC 14443B (Reader/Writer mode only)
- Typical operating distance in Reader/Writer mode for communication to ISO/IEC 14443A/MIFARE, ISO/IEC 14443B or FeliCa cards up to 50 mm depending on antenna size and tuning
- Typical operating distance in NFCIP-1 mode up to 50 mm depending on antenna size, tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE or FeliCa card emulation mode of approximately 100 mm depending on antenna size, tuning and external field strength
- Supports MIFARE Classic 1K or MIFARE Classic 4K encryption in Reader/Writer mode and MIFARE higher transfer speed communication at 212 kbit/s and 424 kbit/s
- Supports contactless communication according to the FeliCa protocol at 212 kbit/s and 424 kbit/s
- Integrated RF interface for NFCIP-1 up to 424 kbit/s
- Possibility to communicate on the RF interface above 424 kbit/s using external analog components
- Supported host interfaces
 - ◆ SPI interface
 - ◆ I²C interface
 - ◆ High-speed UART
- Dedicated host interrupts
- Low power modes
 - ◆ Hard-Power-Down mode (1 μ A typical)
 - ◆ Soft-Power-Down mode (22 μ A typical)
- Automatic wake-up on I²C, HSU and SPI interfaces when device is in Power-down mode
- Programmable timers
- Crystal oscillator
- 2.7 to 5.5 V power supply operating range

- Power switch for external secure companion chip
- Dedicated IO ports for external device control
- Integrated antenna detector for production tests
- ECMA 373 NFC-WI interface to connect an external secure IC

3. Applications

- Mobile and portable devices
- Consumer applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BAT}	Battery supply voltage		2.7		5.5	V
ICV _{DD}	LDO output voltage	V _{BAT} > 3.4 V V _{SS} = 0 V	[1] 2.7	3	3.4	V
PV _{DD}	Supply voltage for host interface	V _{SS} = 0 V	1.6	-	3.6	V
SV _{DD}	Output voltage for secure IC interface	V _{SS} = 0 V (SV _{DD} Switch Enabled)	DV _{DD} - 0.5	-	DV _{DD}	V
I _{HPD}	Hard-Power-Down current consumption	V _{BAT} = 5 V	-	-	2	μA
I _{SPD}	Soft-Power-Down current consumption	V _{BAT} = 5 V, RF level detector on	-	-	45	μA
I _{DVDD}	Digital supply current	V _{BAT} = 5 V, SV _{DD} switch off	[1] -	25	-	mA
I _{SVDD}	SV _{DD} load current	V _{BAT} = 5 V, SV _{DD} switch on	-	-	30	mA
I _{AVDD}	Analog supply current	V _{BAT} = 5 V	-	6	-	mA
I _{TVDD}	Transmitter supply current	During RF transmission, V _{BAT} = 5 V	-	60 [3]	150 [4]	mA
P _{tot}	Continuous total power dissipation	T _{amb} = -30 to +85 °C	[2] -	-	0.5	W
T _{amb}	Operating temperature range		-30	-	+85	°C

[1] DV_{DD}, AV_{DD} and TV_{DD} must always be at the same supply voltage.

[2] The total current consumption depends on the firmware version (different internal IC clock speed)

[3] With an antenna tuned at 50 Ω at 13.56 MHz

[4] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5321A3HN/C1xx ^{[1][2][4]}	HVQFN40	Heatsink Very thin Quad Flat package; 40 pins, plastic, body 6 x 6 x 0.85 mm; leadless; MSL level 2 ^[3] .	SOT618-1

- [1] xx refers to the ROM code version. The ROM code functionalities are described in the User-Manual document. Each ROM code has its own User-Manual.
- [2] This NXP IC is licensed under Innovatron's ISO/IEC 14443 Type B patent license.
- [3] This is tested according the joint IPC/JEDEC standard J-STD-020C of July 2004.
- [4] Purchase of an NXP Semiconductors IC that complies with one of the NFC Standards (ISO/IEC18.092; ISO/IEC21.481) does not convey an implied license under any patent right on that standards.

6. Block diagram

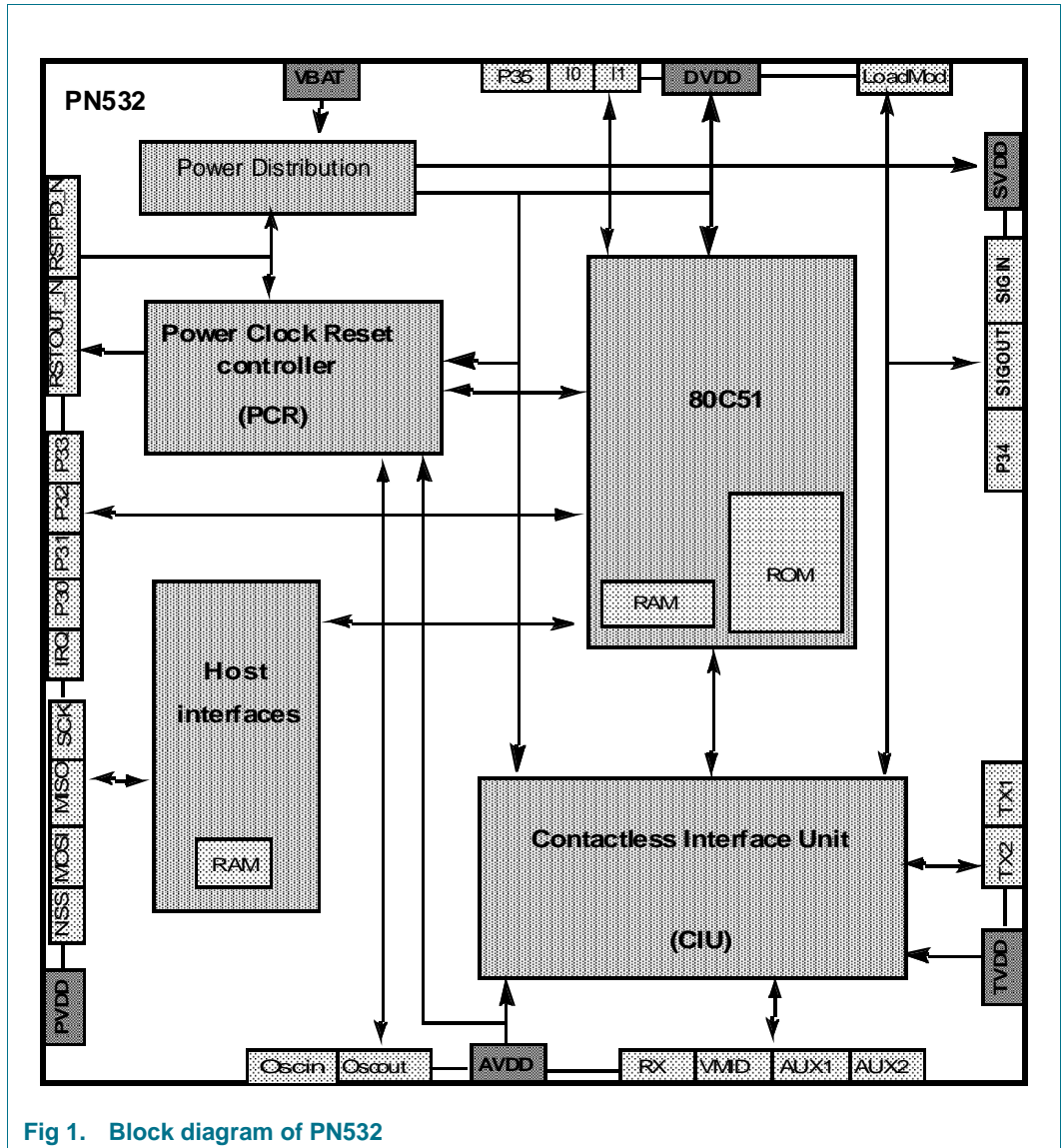


Fig 1. Block diagram of PN532

7. Functional description

7.1 Contactless Interface Unit (CIU)

The PN532 CIU is a modem for contactless communication at 13.56 MHz. It supports 6 different operating modes

- ISO/IEC 14443A/MIFARE Reader/Writer.
- FeliCa Reader/Writer.
- ISO/IEC 14443B Reader/Writer
- ISO/IEC 14443A/MIFARE Card 1K or MIFARE 4K card emulation mode
- FeliCa Card emulation
- ISO/IEC 18092, ECMA 340 NFCIP-1 Peer-to-Peer

The CIU implements a demodulator and decoder for signals from ISO/IEC 14443A/MIFARE compatible cards and transponders. The CIU handles the complete ISO/IEC 14443A framing and error detection (Parity & CRC).

The CIU supports MIFARE Classic 1K or MIFARE Classic 4K card emulation mode. The CIU supports contactless communication using MIFARE Higher transfer speeds up to 424 kbit/s in both directions.

The CIU can demodulate and decode FeliCa coded signals. The CIU digital part handles the FeliCa framing and error detection. The CIU supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions.

The CIU supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision which must be implemented in firmware as well as upper layers.

In card emulation mode, the CIU is able to answer to a Reader/Writer command either according to the FeliCa or ISO/IEC 14443A/MIFARE card interface scheme. The CIU generates the load modulation signals, either from its transmitter or from the LOADMOD pin driving an external active circuit. A complete secure card functionality is only possible in combination with a secure IC using the NFC-WI/S²C interface.

Compliant to ECMA 340 and ISO/IEC 18092 NFCIP-1 Passive and Active communication modes, the CIU offers the possibility to communicate to another NFCIP-1 compliant device, at transfer speeds up to 424 kbit/s. The CIU handles the complete NFCIP-1 framing and error detection.

The CIU transceiver can be connected to an external antenna for Reader/Writer or Card/PICC modes, without any additional active component.

7.1.1 Feature list

- Frequently accessed registers placed in SFR space
- Highly integrated analog circuitry to demodulate and decode received data
- Buffered transmitter drivers to minimize external components to connect an antenna.
- Integrated RF level detector
- Integrated data mode detector
- Typical operating distance of 50 mm in ISO/IEC 14443A/MIFARE or FeliCa in Reader/Writer mode depending on the antenna size, tuning and power supply
- Typical operating distance of 50 mm in NFCIP-1 mode depending on the antenna size, tuning and power supply
- Typical operating distance in ISO/IEC 14443A/MIFARE card or FeliCa card operation mode of about 100 mm depending on the antenna size, tuning and the external field strength
- Supports MIFARE Classic 1K or MIFARE Classic 4K encryption in Reader/Writer mode
- Supports MIFARE higher data rate at 212 kbit/s and 424 kbit/s
- Supports contactless communication according to the FeliCa scheme at 212 kbit/s and 424 kbit/s
- Support of the NFC-WI/S²C interface
- 64 byte send and receive FIFO-buffer
- Programmable timer
- CRC Co-processor
- Internal self test and antenna presence detector
- 2 interrupt sources
- Adjustable parameters to optimize the transceiver performance according to the antenna characteristics

7.1.2 Simplified block diagram

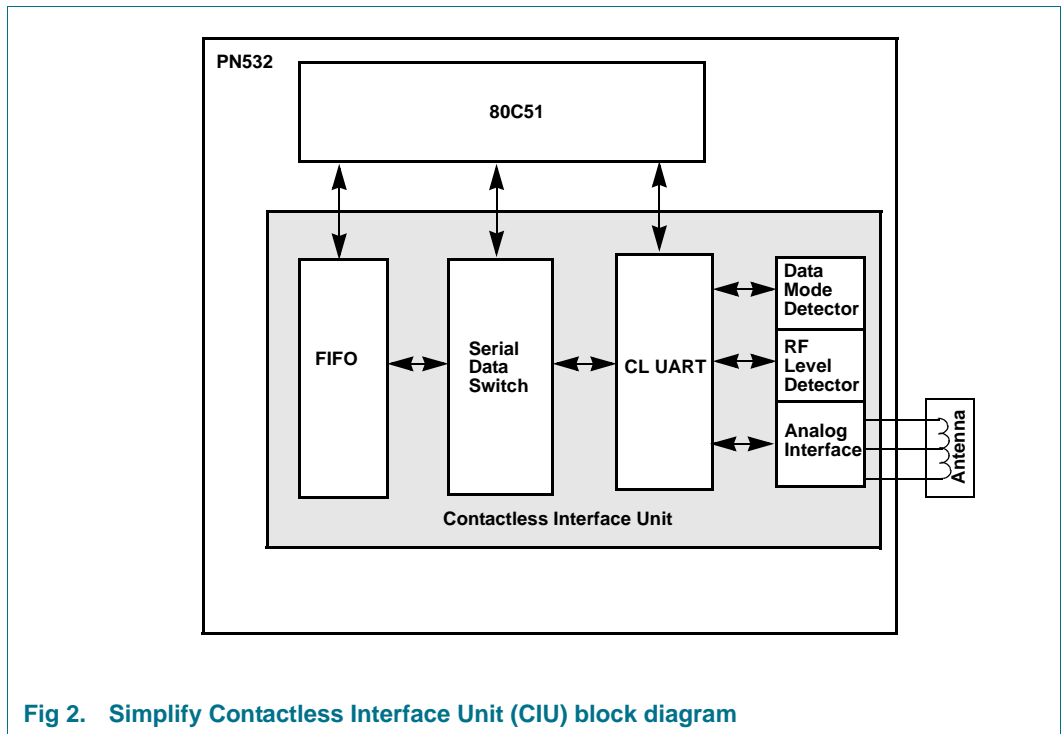


Fig 2. Simplify Contactless Interface Unit (CIU) block diagram

The Analog Interface handles the modulation and demodulation of the analog signals according to the Card emulation mode, Reader/Writer mode and NFCIP-1 mode communication scheme.

The RF level detector detects the presence of an external RF-field delivered by the antenna to the RX pin.

The data mode detector detects a ISO/IEC 14443-A MIFARE, FeliCa or NFCIP-1 mode in order to prepare the internal receiver to demodulate signals, which are sent to the PN532.

The NFC-WI/S²C interface supports communication to secure IC. It also supports digital signals for transfer speeds above 424 kbit/s.

The CL UART handles the protocol requirements for the communication schemes in co-operation with the appropriate firmware. The FIFO buffer allows a convenient data transfer from the 80C51 to the CIU and vice versa.

7.1.3 Reader/Writer modes

All indicated modulation indices and modes in this chapter are system parameters. This means that beside the IC settings a suitable antenna tuning is required to achieve the optimal performance.

7.1.3.1 ISO/IEC 14443A Reader/Writer

The following diagram describes the communication on a physical level, the communication overview in the [Table 3](#) describes the physical parameters.

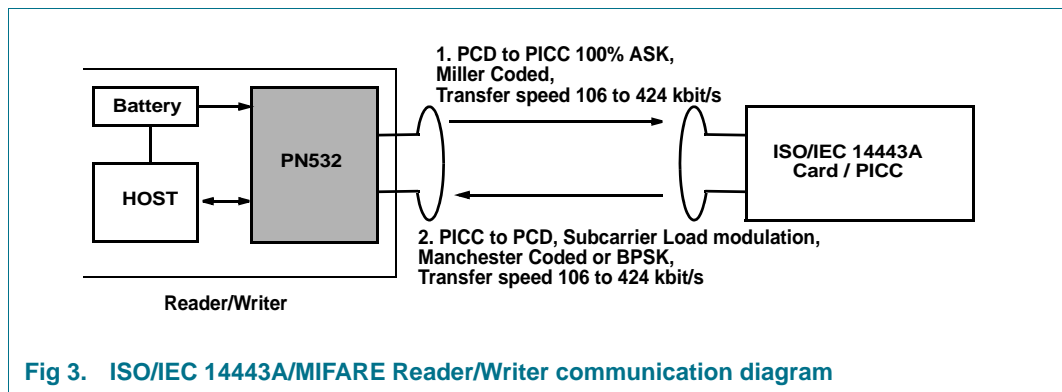


Fig 3. ISO/IEC 14443A/MIFARE Reader/Writer communication diagram

Table 3. Communication overview for ISO/IEC 14443A/MIFARE Reader/Writer

Communication scheme		ISO/IEC 14443A MIFARE	MIFARE Higher Baud Rate	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
PN532 to PICC/Card	Modulation	100% ASK	100% ASK	100% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC/Card to PN532	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz ₁₆	13.56 MHz ₁₆	13.56 MHz ₁₆
	Bit coding	Manchester coding	BPSK	BPSK

The internal CRC co-processor calculates the CRC value according the data coding and framing defined in the ISO/IEC 14443A part 3, and handles parity generation internally according to the transfer speed.

With appropriate firmware, the PN532 can handle the complete ISO/IEC 14443A/MIFARE protocol.

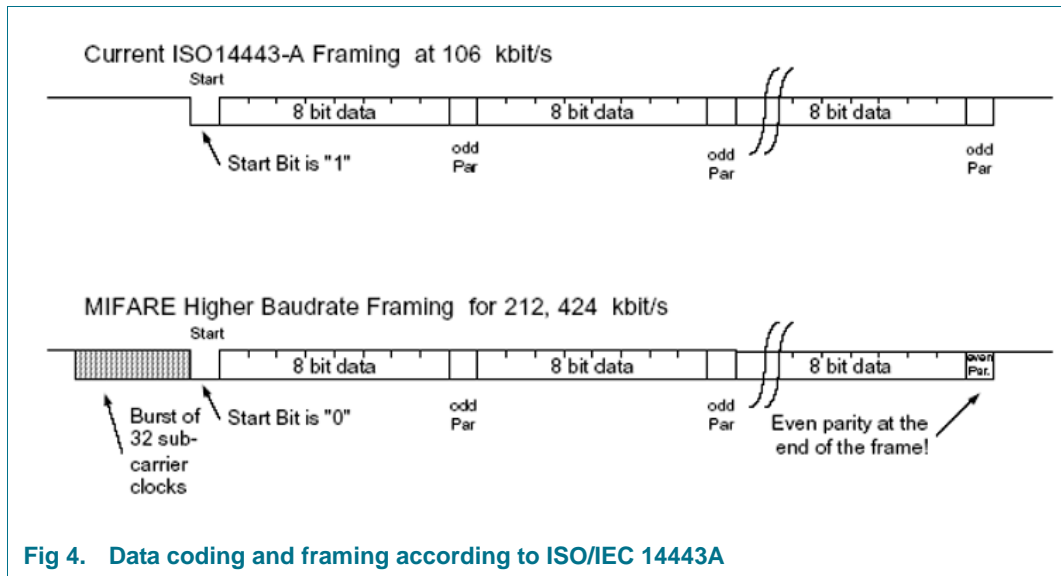


Fig 4. Data coding and framing according to ISO/IEC 14443A

7.1.3.2 FeliCa Reader/Writer

The following diagram describes the communication at the physical level. [Table 4](#) describes the physical parameters.

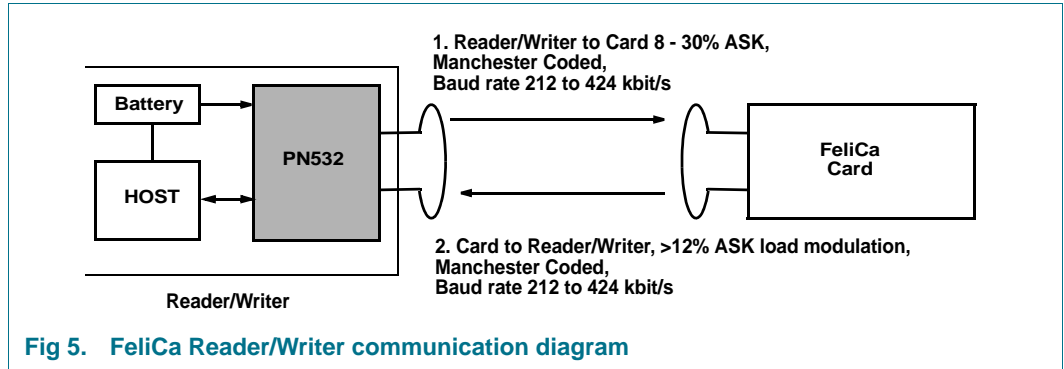


Table 4. Communication overview for FeliCa Reader/Writer

Communication scheme		FeliCa	FeliCa higher baud rate
Baud rate		212 kbit/s	424 kbit/s
Bit length		$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
PN532 to PICC/Card	Modulation	8 - 30% ASK	8 - 30% ASK
	Bit coding	Manchester coding	Manchester coding
PICC/Card to PN532	Modulation	>12% ASK	>12% ASK
	Bit coding	Manchester coding	Manchester coding

With appropriate firmware, the PN532 can handle the FeliCa protocol.

The FeliCa Framing and coding must comply with the following table:

Table 5. FeliCa Framing and Coding

Preamble						SYNC		LEN	n-Data				CRC	
00h	00h	00h	00h	00h	00h	B2h	4Dh							

To enable the FeliCa communication a 6-byte preamble (00h, 00h, 00h, 00h, 00h, 00h) and 2-byte SYNC bytes (B2h, 4Dh) are sent to synchronize the receiver.

The following LEN byte indicates the length of the sent data bytes plus the LEN byte itself. The CRC calculation is done according to the FeliCa definitions with the MSB first.

To transmit data on the RF interface, the 80C51 has to send the LEN and data bytes to the CIU. The Preamble and SYNC bytes are generated by the CIU automatically and must not be written to the FIFO. The CIU performs internally the CRC calculation and adds the result to the frame.

The starting value for the CRC Polynomial is 2 null bytes: (00h), (00h)

Example of frame:

Table 6. FeliCa framing and coding

Preamble						SYNC		LEN	2 Data Bytes		CRC	
00	00	00	00	00	00	B2	4D	03	AB	CD	90	35

7.1.3.3 ISO/IEC 14443B Reader/Writer

The CIU supports layers 2 and 3 of the ISO/IEC 14443 B Reader/Writer communication scheme, except anticollision which must be implemented in firmware as well as upper layers.

The following diagram describes the communication at the physical level. [Table 7](#) describes the physical parameters.

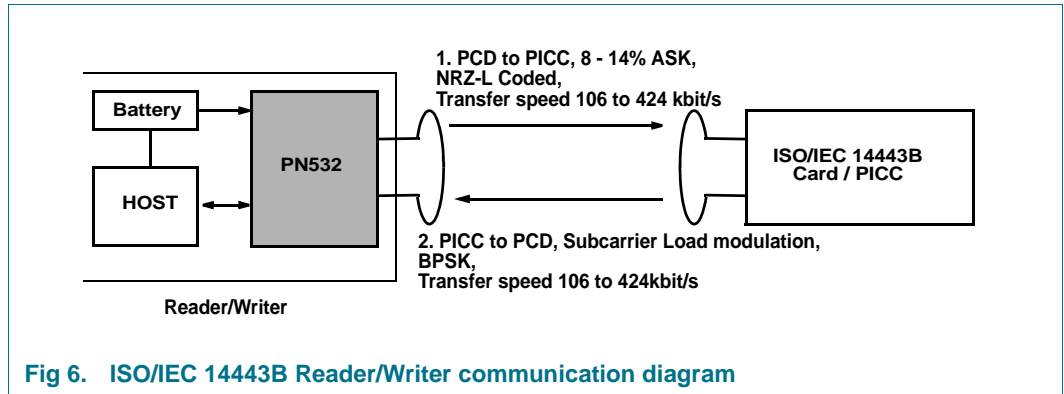


Fig 6. ISO/IEC 14443B Reader/Writer communication diagram

With appropriate firmware, the PN532 can handle the ISO/IEC 14443B protocol.

Table 7. Communication overview for ISO/IEC 14443B Reader/Writer

Communication scheme		ISO/IEC 14443B	Type B higher baud rate	
		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
PN532 to PICC/Card	Modulation	8 -14% ASK	8 -14% ASK	8 -14% ASK
	Bit coding	NRZ-L	NRZ-L	NRZ-L
PICC/Card to PN532	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz ₁₆	13.56 MHz ₁₆	13.56 MHz ₁₆
	Bit coding	BPSK	BPSK	BPSK

7.1.4 ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode

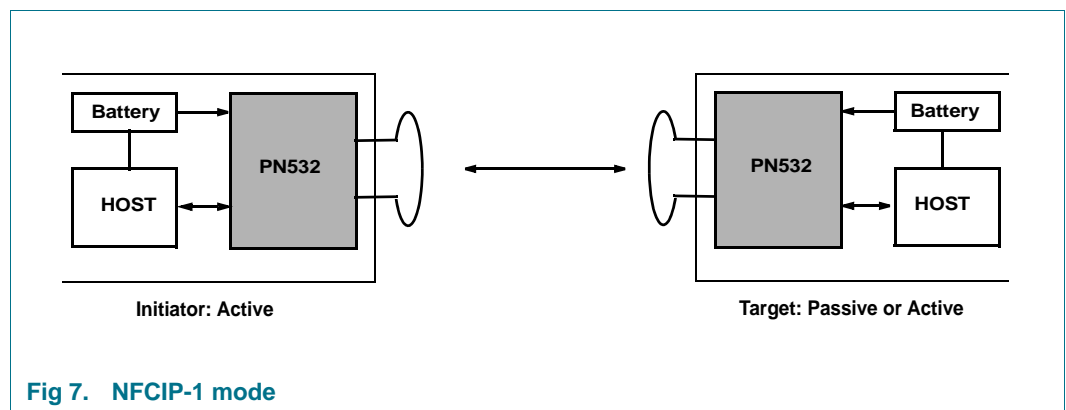
A NFCIP-1 communication takes place between 2 devices:

- Initiator: generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self generated and self modulated RF field for Active Communication mode.

The NFCIP-1 communication differentiates between Active and Passive communication modes.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data
- Passive Communication mode means that the Target answers to an Initiator command in a load modulation scheme. The Initiator is active in terms of generating the RF field.

In order to fully support the NFCIP-1 standard the PN532 supports the Active and Passive Communications mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard



With appropriate firmware, the PN532 can handle the NFCIP-1 protocol, for all communication modes and data rates, for both Initiator and Target.

7.1.4.1 ACTIVE Communication mode

Active Communication Mode means both the Initiator and the Target are using their own RF field to transmit data.

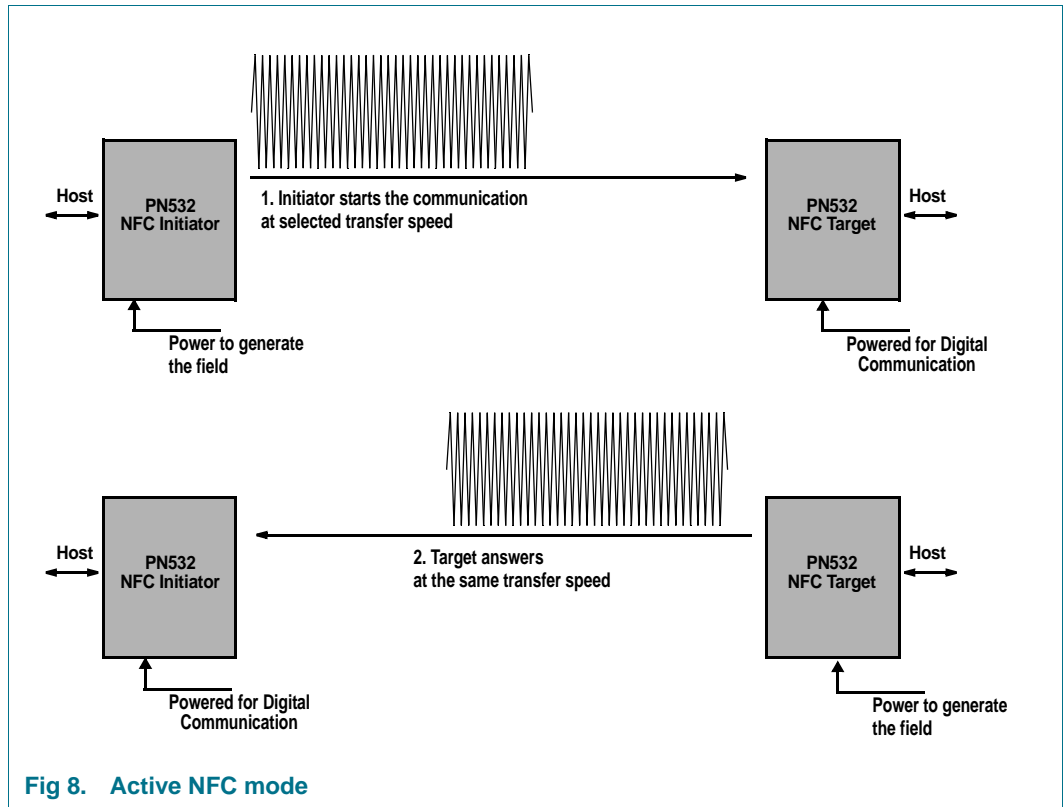


Fig 8. Active NFC mode

The following table gives an overview of the active communication modes:

Table 8. Communication overview for NFC Active Communication mode

Communication scheme		ISO/IEC 18092, ECMA 340, NFCIP-1		
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
Initiator to Target	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded
Target to Initiator	Modulation	100% ASK	8-30%ASK	8-30%ASK
	Bit coding	Miller Coded	Manchester Coded	Manchester Coded

7.1.4.2 PASSIVE Communication mode

Passive Communication Mode means that the target answers to an Initiator command in a load modulation scheme.

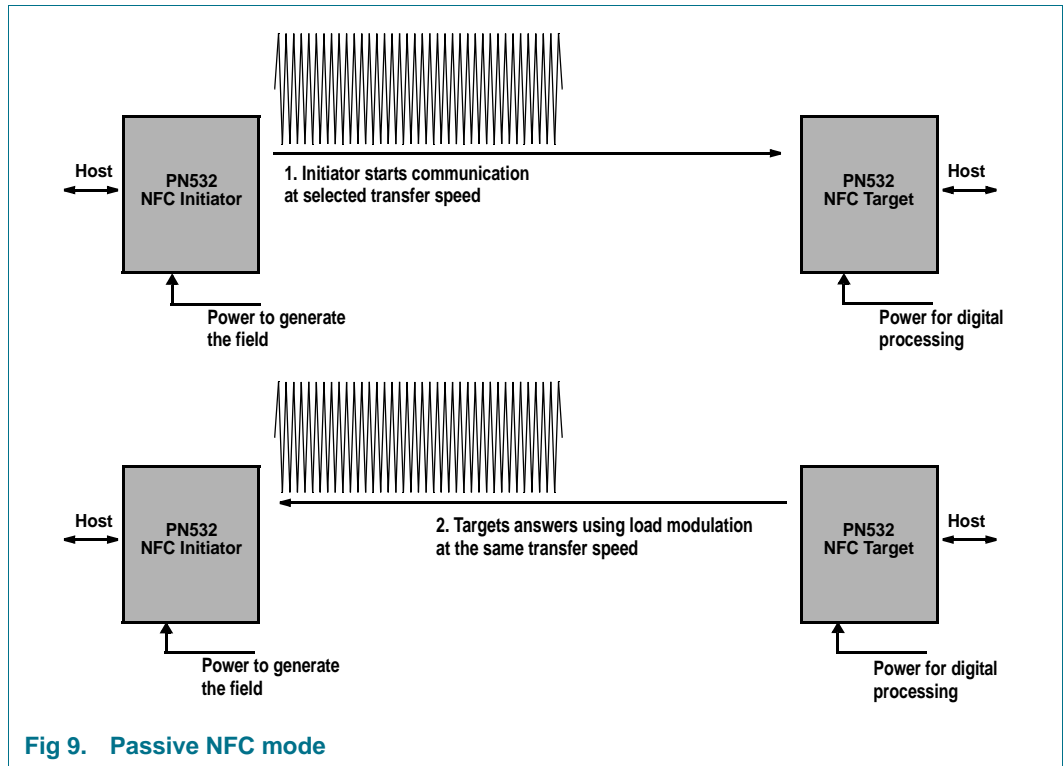


Fig 9. Passive NFC mode

The following table gives an overview of the active communication modes:

Table 9. Communication overview for NFC Passive Communication mode

Communication scheme		ISO/IEC 18092, ECMA 340, NFCIP-1		
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56\text{MHz}} \approx 9.44\mu\text{s}$	$\frac{64}{13.56\text{MHz}} \approx 4.72\mu\text{s}$	$\frac{32}{13.56\text{MHz}} \approx 2.36\mu\text{s}$
PN532 to PICC/Card	Modulation	100% ASK	100% ASK	100% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PICC/Card to PN532	Modulation	Subcarrier load modulation	>12% ASK	>12% ASK
	Subcarrier frequency	13.56 MHz/16	No subcarrier	No subcarrier
	Bit coding	Manchester coding	Manchester coding	Manchester coding

7.1.4.3 NFCIP-1 framing and coding

The NFCIP-1 framing and coding in Active and Passive communication modes are defined in the NFCIP-1 standard: ISO/IEC 18092 or ECMA 340.

7.1.4.4 NFCIP-1 protocol support

The NFCIP-1 protocol is not completely described in this document. For detailed explanation of the protocol refer to the ISO/IEC 18092 / ECMA340 NFCIP-1 standard. However the datalink layer is according to the following policy:

- Transaction includes initialization, anticollision methods and data transfer. This sequence must not be interrupted by another transaction.
- Speed should not be changed during a data transfer

In order not to disturb current infrastructure based on 13.56 MHz general rules to start NFC communication are defined in the following way:

- Per default NFCIP-1 device is in target mode, meaning its RF field is switched off.
- The RF level detector is active.
- Only if application requires the NFCIP-1 device shall switch to Initiator mode.
- Initiator shall only switch on its RF field if no external RF field is detected by RF Level detector during a time of TIDT.
- The initiator performs initialization according to the selected mode.

7.1.5 Card operating modes

The PN532 can be addressed like a FeliCa or ISO/IEC 14443A/MIFARE card. This means that the PN532 can generate an answer in a load modulation scheme according to the ISO/IEC 14443A/MIFARE or FeliCa interface description.

Remark: The PN532 does not support a secure storage of data. This has to be handled by a dedicated secure IC or a host. The secure IC is optional.

Remark: The PN532 can not be powered by the field in this mode and needs a power supply.

7.1.5.1 ISO/IEC 14443A/MIFARE card operating mode

With appropriate firmware, the PN532 can handle the ISO/IEC 14443A including the level 4, and the MIFARE protocols.

The following diagram describes the communication at the physical level. [Table 10](#) describes the physical parameters.

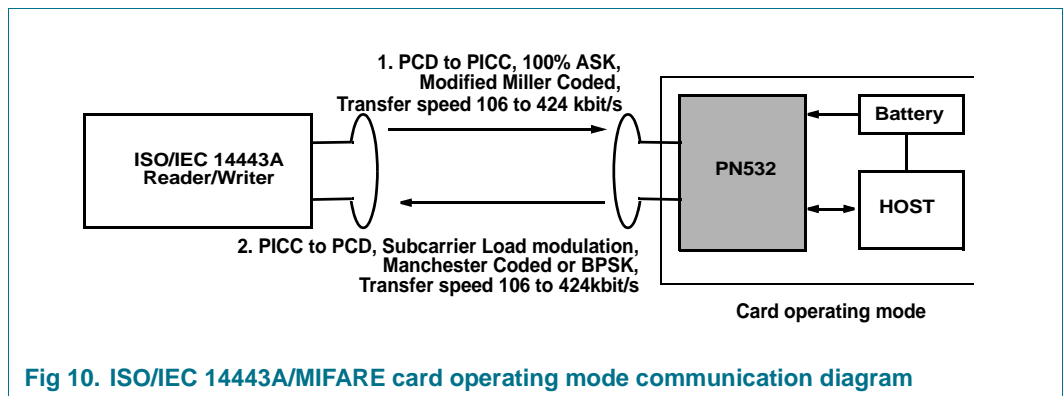


Fig 10. ISO/IEC 14443A/MIFARE card operating mode communication diagram

Table 10. Communication overview for ISO/IEC 14443A/MIFARE Card operating mode

Communication scheme		ISO/IEC 14443A MIFARE	MIFARE higher baud rate	
Baud rate		106 kbit/s	212 kbit/s	424 kbit/s
Bit length		$\frac{128}{13.56MHz} \approx 9.44\mu s$	$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
Reader/Writer to PN532	Modulation	100% ASK	100% ASK	100% ASK
	Bit coding	Modified Miller coding	Modified Miller coding	Modified Miller coding
PN532 to Reader/Writer	Modulation	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	Subcarrier frequency	13.56 MHz ₁₆	13.56 MHz ₁₆	13.56 MHz ₁₆
	Bit coding	Manchester coding	BPSK	BPSK

7.1.5.2 FeliCa Card operating mode

With appropriate firmware, the PN532 can handle the FeliCa protocol.

The following diagram describes the communication at the physical level. [Table 11](#) describes the physical parameters.

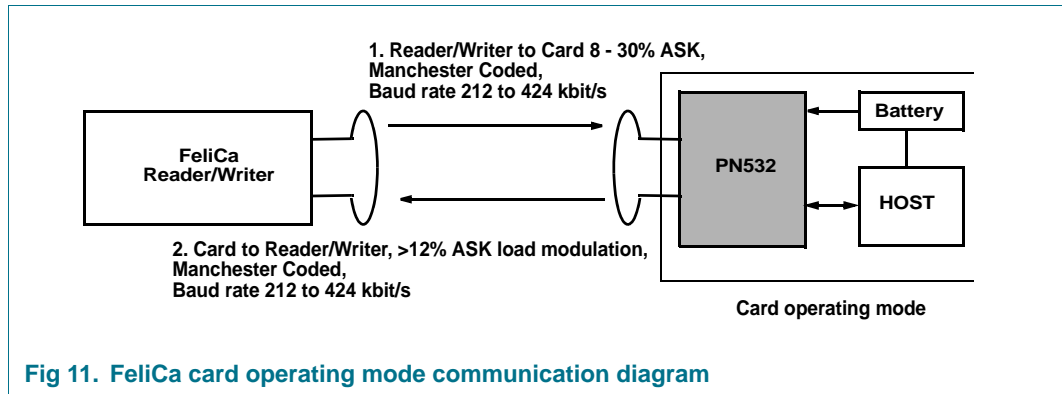


Fig 11. FeliCa card operating mode communication diagram

Table 11. Communication overview for FeliCa Card operating mode

Communication scheme		FeliCa	FeliCa higher baud rate
Baud rate		212 kbit/s	424 kbit/s
Bit length		$\frac{64}{13.56MHz} \approx 4.72\mu s$	$\frac{32}{13.56MHz} \approx 2.36\mu s$
Reader/Writer to PN532	Modulation	8 - 30% ASK	8 - 30% ASK
	Bit coding	Manchester coding	Manchester coding
PN532 to Reader/Writer	Modulation	>12% ASK	>12% ASK
	Bit coding	Manchester coding	Manchester coding

7.1.6 Overall CIU block diagram

The PN532 supports different contactless communication modes. The CIU supports the internal 80C51 for the different selected communication schemes such as Card Operation mode, Reader/Writer Operating mode or NFCIP-1 mode up to 424 kbit/s. The CIU generates bit- and byte-oriented framing and handles error detection according to these different contactless protocols.

Higher transfer speeds up to 3.39 Mbit/s can be handled by the digital part of the CIU. To modulate and demodulate the data an external circuit has to be connected to the communication interface pins SIGIN/SIGOUT.

Remark: The size and tuning of the antenna have an important impact on the achievable operating distance.

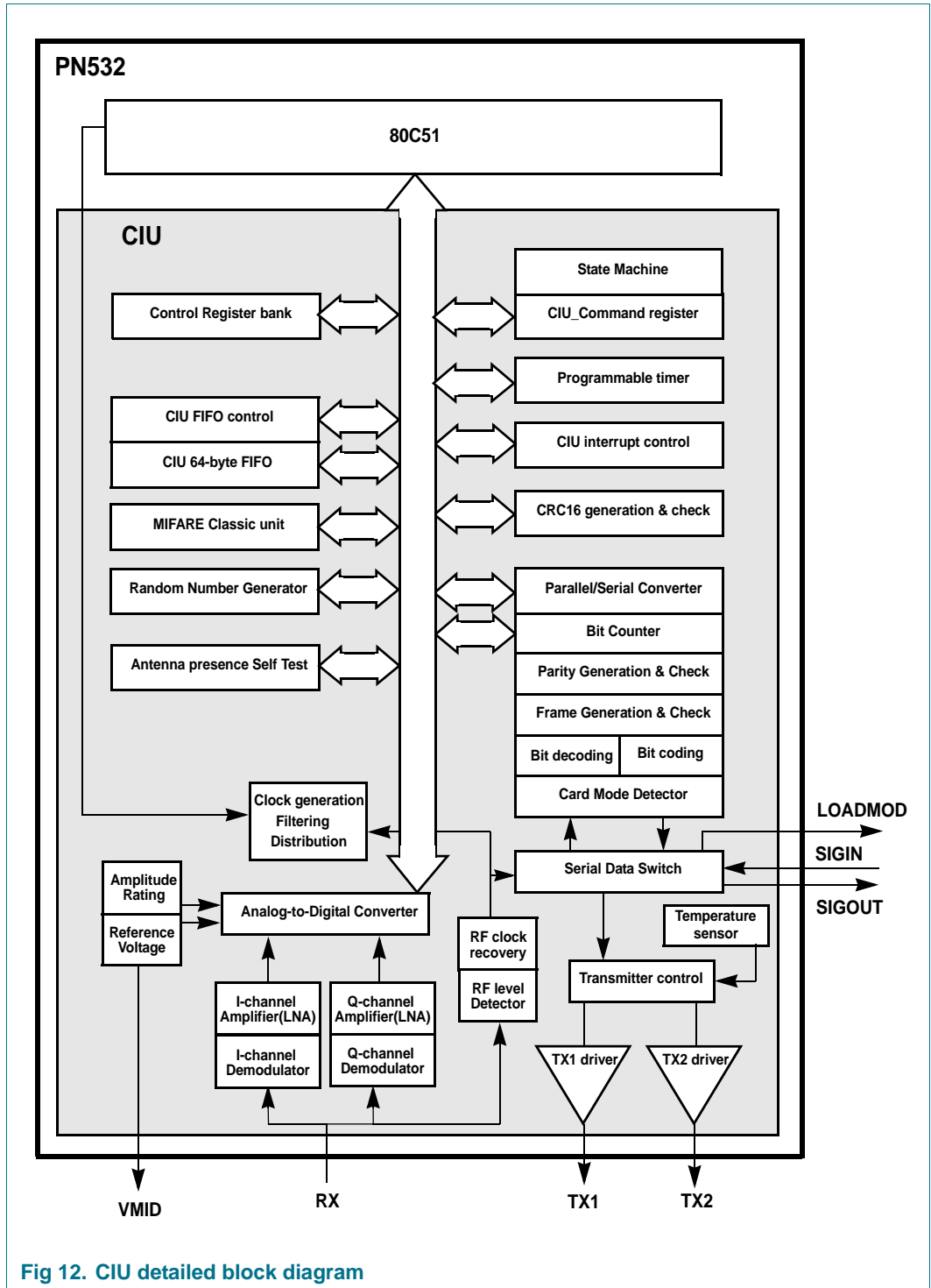


Fig 12. CIU detailed block diagram

8. Limiting values

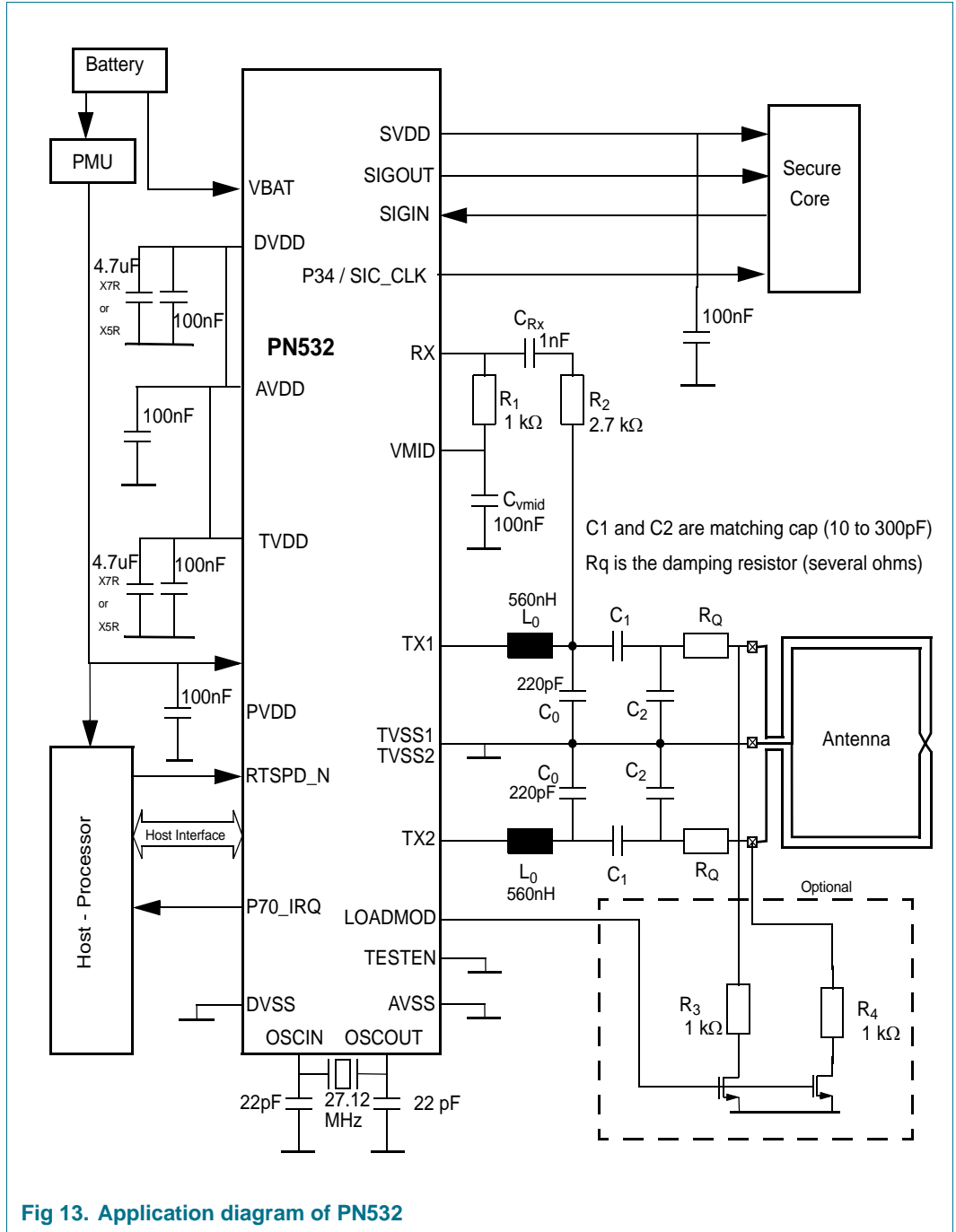
Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{VDD}	Supply Voltage		-0.5	4	V
V_{BAT}	Power Supply Voltage		-0.5	6.0	V
P_{tot}	Total power dissipation		-	500	mW
I_{TVDD}	Maximum current in TVDD		[1]	150	mA
I_{SVDD}	Maximum current in SVDD switch		-	30	mA
V_{ESD}	Electrostatic discharge voltage				
V_{ESDH}	ESD Susceptibility (Human Body model)	1500 Ω , 100pF; EIA/JESD22-A114-D	-	± 2.0	kV
V_{ESDM}	ESD Susceptibility (Machine model)	0.75 mH, 200 pF; EIA/JESD22-A115-A	-	200	V
V_{ESDC}	ESD Susceptibility (Charge Device model)	Field induced model; EIA/JESC22-C101-C	-	± 1.0	kV
T_{stg}	Storage temperature		-55	150	$^{\circ}\text{C}$
T_j	Junction temperature		-40	125	$^{\circ}\text{C}$

[1] The antenna should be tuned not to exceed this current limit (the detuning effect when coupling with another device must be taken into account)

9. Application information



In the example the 27.12MHz quartz is a TAS-3225A, SMD

10. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm

SOT618-1

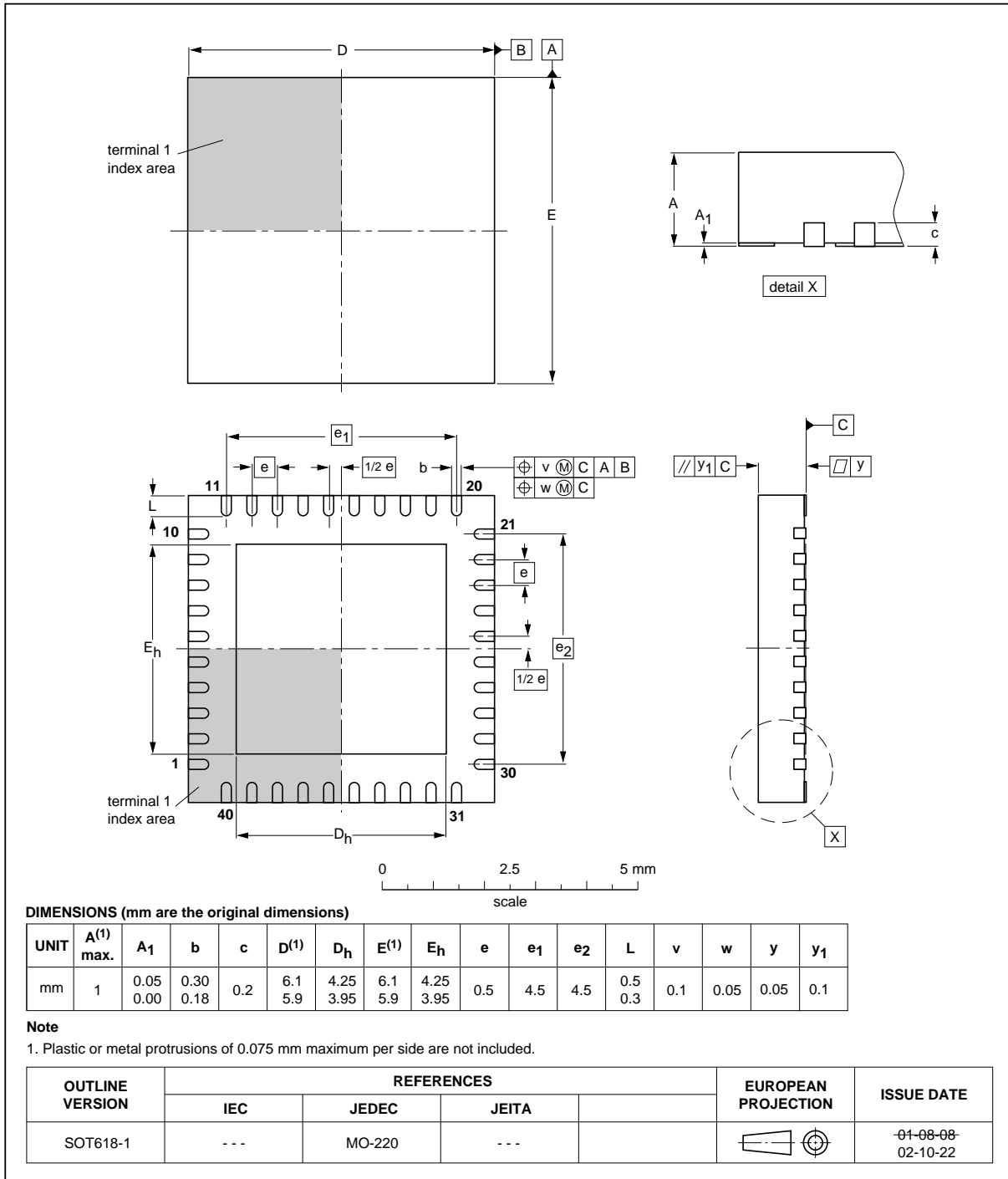


Fig 14. Package outline HVQFN40 (SOT618-1)

This package is MSL level 2.

11. Abbreviations

Table 13. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
BPSK	Bit Phase Shift Keying
CRC	Cyclic Redundancy Check
ECMA	European Computer Manufacturers Association organization
HPD	Hard Power Down
HSU	High Speed UART
Initiator	Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
LDO	Low Drop-Out regulator
MSL	Moisture Sensitivity Level
NFCIP	NFC Interface and Protocol
NFC-WI	NFC Wired Interface to connect NFC front end to a SIC
PCD	Proximity Coupling Device. Definition for a Card Reader/ Writer according to the ISO/IEC 14443 Specification
PICC	Proximity Cards. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification
SIC	Secure Integrated Circuit (can be a Smart Card IC, a Secure Access Module (SAM),...)
SPI	Serial Parallel Interface
SPD	Soft Power Down mode
Target	Responds to initiator command either using load modulation scheme (RF field generated by Initiator) or using modulation of self-generated RF field (no RF field generated by initiator during target answer).
UART	Universal Asynchronous Receive Transmit

12. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN532_C1_SDS v.3.2	20120920	Product short data sheet	-	PN532_SDS_120131
Modifications:	<ul style="list-style-type: none"> • Section 5 "Ordering information": updated • Section 13.4 "Licenses": updated 			
PN532_SDS_120131	20111201	Product short data sheet	-	PN532_SDS_120130
Modifications:	<ul style="list-style-type: none"> • Section 5 "Ordering information": updated 			
PN532_SDS_120130	20111110	Product short data sheet	-	120112
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • General update 			
120112	20060112	Short form data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

14. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

13.4 Licenses

Purchase of NXP ICs with NFC technology

Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards.

Purchase of NXP ICs with ISO/IEC 14443 type B functionality



RATP/Innovatron Technology

This NXP Semiconductors IC is ISO/IEC 14443 Type B software enabled and is licensed under Innovatron's Contactless Card patents license for ISO/IEC 14443 B.

The license includes the right to use the IC in systems and/or end-user equipment.

13.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

MIFARE — is a trademark of NXP B.V.

15. Contents

1	General description	1
2	Features and benefits	2
3	Applications	3
4	Quick reference data	3
5	Ordering information	4
6	Block diagram	5
7	Functional description	6
7.1	Contactless Interface Unit (CIU)	6
7.1.1	Feature list	7
7.1.2	Simplified block diagram	8
7.1.3	Reader/Writer modes	9
7.1.3.1	ISO/IEC 14443A Reader/Writer	9
7.1.3.2	FeliCa Reader/Writer	11
7.1.3.3	ISO/IEC 14443B Reader/Writer	12
7.1.4	ISO/IEC 18092, ECMA 340 NFCIP-1 operating mode	13
7.1.4.1	ACTIVE Communication mode	14
7.1.4.2	PASSIVE Communication mode	15
7.1.4.3	NFCIP-1 framing and coding	16
7.1.4.4	NFCIP-1 protocol support	16
7.1.5	Card operating modes	17
7.1.5.1	ISO/IEC 14443A/MIFARE card operating mode	17
7.1.5.2	FeliCa Card operating mode	18
7.1.6	Overall CIU block diagram	18
8	Limiting values	20
9	Application information	21
10	Package outline	22
11	Abbreviations	23
12	Revision history	24
13	Legal information	25
13.1	Data sheet status	25
13.2	Definitions	25
13.3	Disclaimers	25
13.4	Licenses	26
13.5	Trademarks	26
14	Contact information	26
15	Contents	27

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 September 2012
120132