

PMR280UN

N-channel μ TrenchMOS™ ultra low level FET

Rev. 01 — 5 March 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Surface mounted package
- Low on-state resistance
- Footprint 63% smaller than SOT23
- Low threshold voltage.

1.3 Applications

- Driver circuits
- Switching in portable appliances.

1.4 Quick reference data

- $V_{DS} \leq 20$ V
- $I_D \leq 0.98$ A
- $P_{tot} \leq 0.53$ W
- $R_{DS(on)} \leq 340$ m Ω .

2. Pinning information

Table 1: Pinning - SOT416 (SC-75), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MBK090</p>	<p>MBB076</p>
2	source (s)		
3	drain (d)		

SOT416 (SC-75)

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMR280UN	SC-75	Plastic surface mounted package; 3 leads	SOT416



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4. Limiting values

Table 3: Limiting values

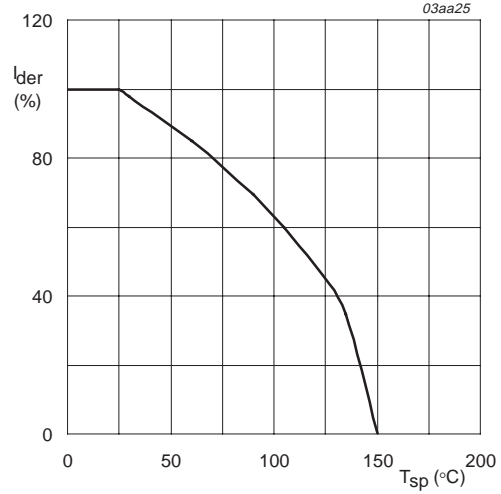
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage (DC)		-	± 8	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2 and 3	-	0.98	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2	-	0.62	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	1.97	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	0.53	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	0.44	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	0.88	A



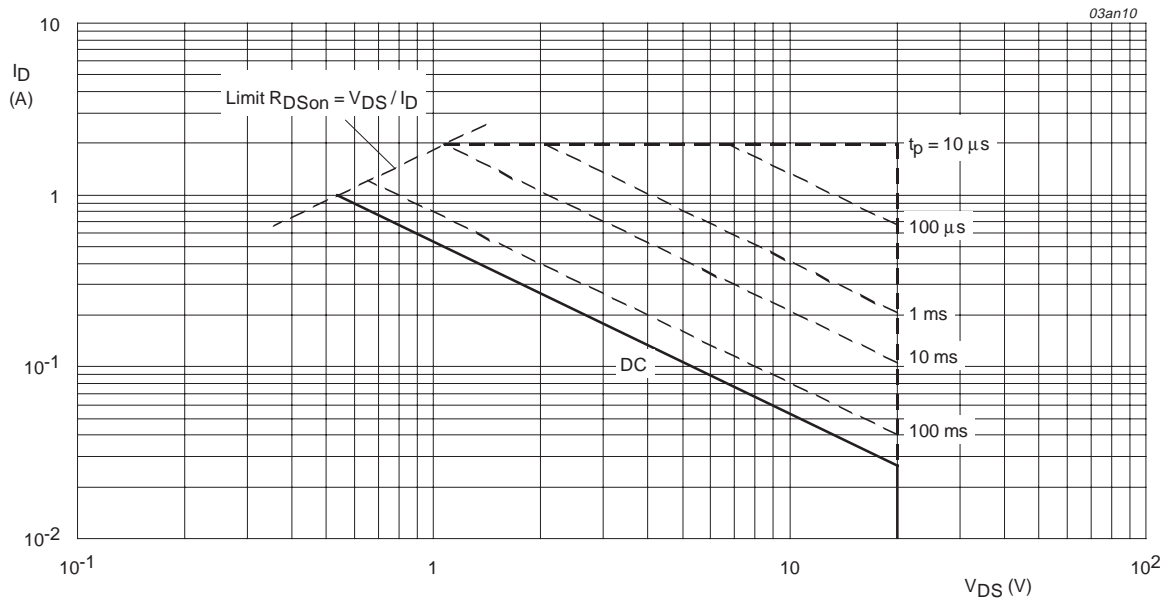
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse; V_{GS} = 4.5 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	235	K/W

5.1 Transient thermal impedance

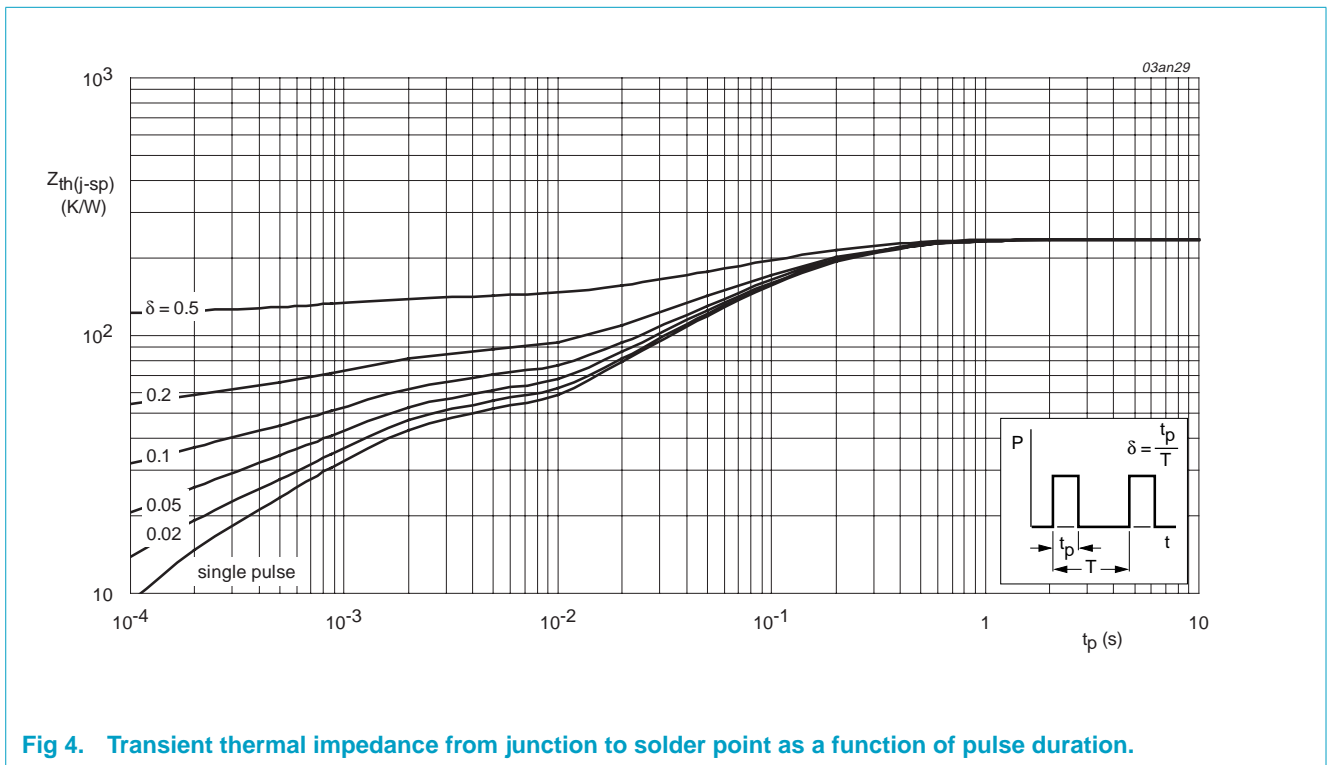


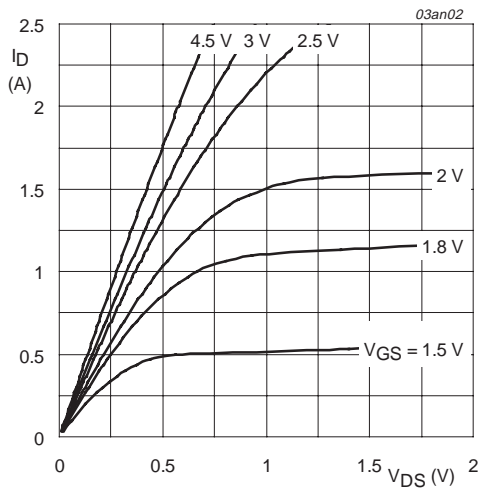
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

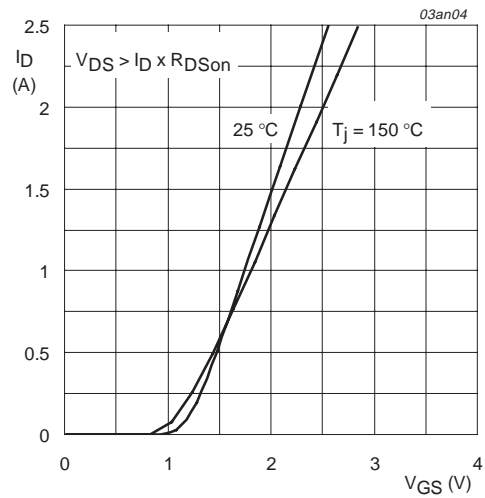
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 1\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	20	-	-	V
		$T_j = -55\text{ °C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	0.45	0.7	1	V
		$T_j = 150\text{ °C}$	0.25	-	-	V
		$T_j = -55\text{ °C}$	-	-	1.2	V
I_{DSS}	drain-source leakage current	$V_{DS} = 20\ \text{V}$; $V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 150\text{ °C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 8\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 0.2\ \text{A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	280	340	m Ω
		$T_j = 150\text{ °C}$	-	448	544	m Ω
		$V_{GS} = 2.5\ \text{V}$; $I_D = 0.1\ \text{A}$; Figure 7 and 8	-	360	430	m Ω
		$V_{GS} = 1.8\ \text{V}$; $I_D = 0.075\ \text{A}$; Figure 7 and 8	-	460	660	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 1\ \text{A}$; $V_{DD} = 10\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; Figure 13	-	0.89	-	nC
Q_{gs}	gate-source charge		-	0.13	-	nC
Q_{gd}	gate-drain (Miller) charge		-	0.18	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 20\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	45	-	pF
C_{oss}	output capacitance		-	11	-	pF
C_{rss}	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\ \text{V}$; $R_L = 10\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_G = 6\ \Omega$	-	4.5	-	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	18.5	-	ns
t_f	fall time		-	5	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 0.3\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.83	1.2	V



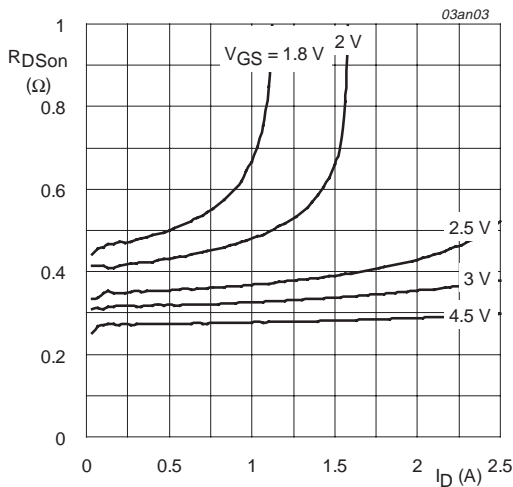
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



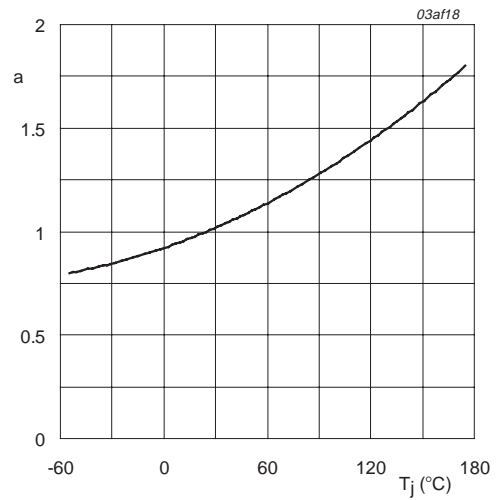
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



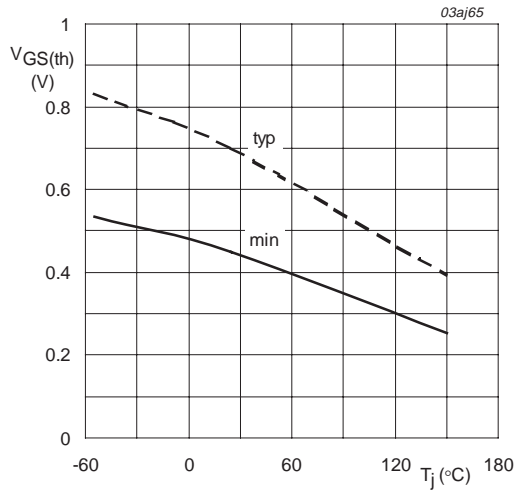
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



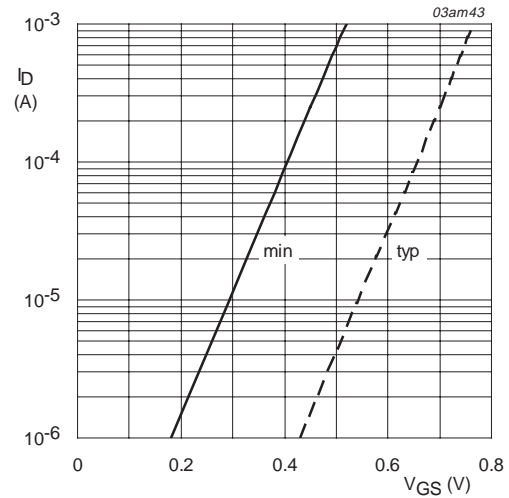
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



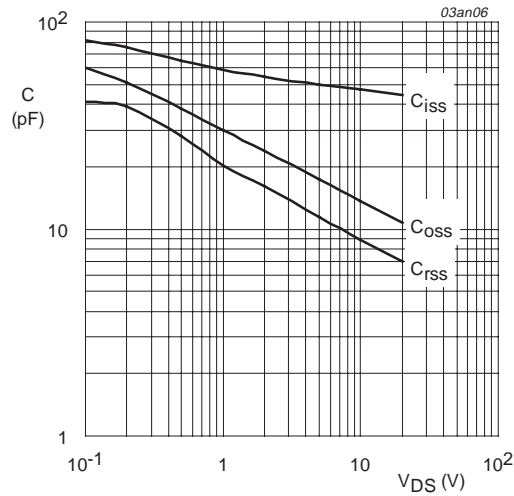
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



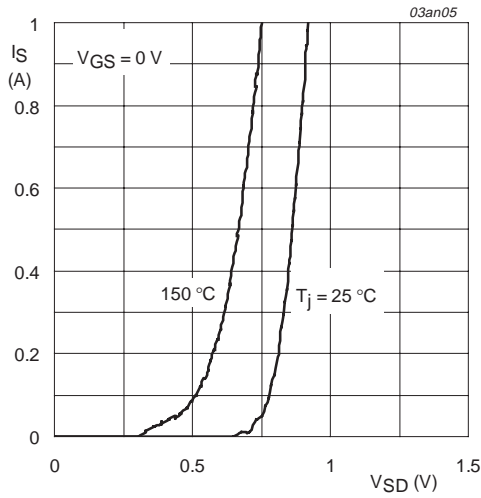
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



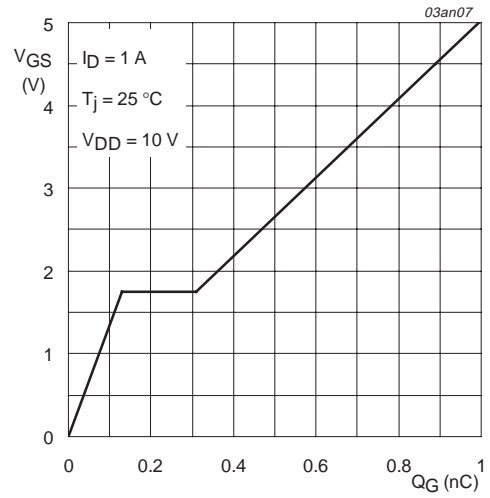
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 1\text{ A}$; $V_{DD} = 10\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic surface mounted package; 3 leads

SOT416

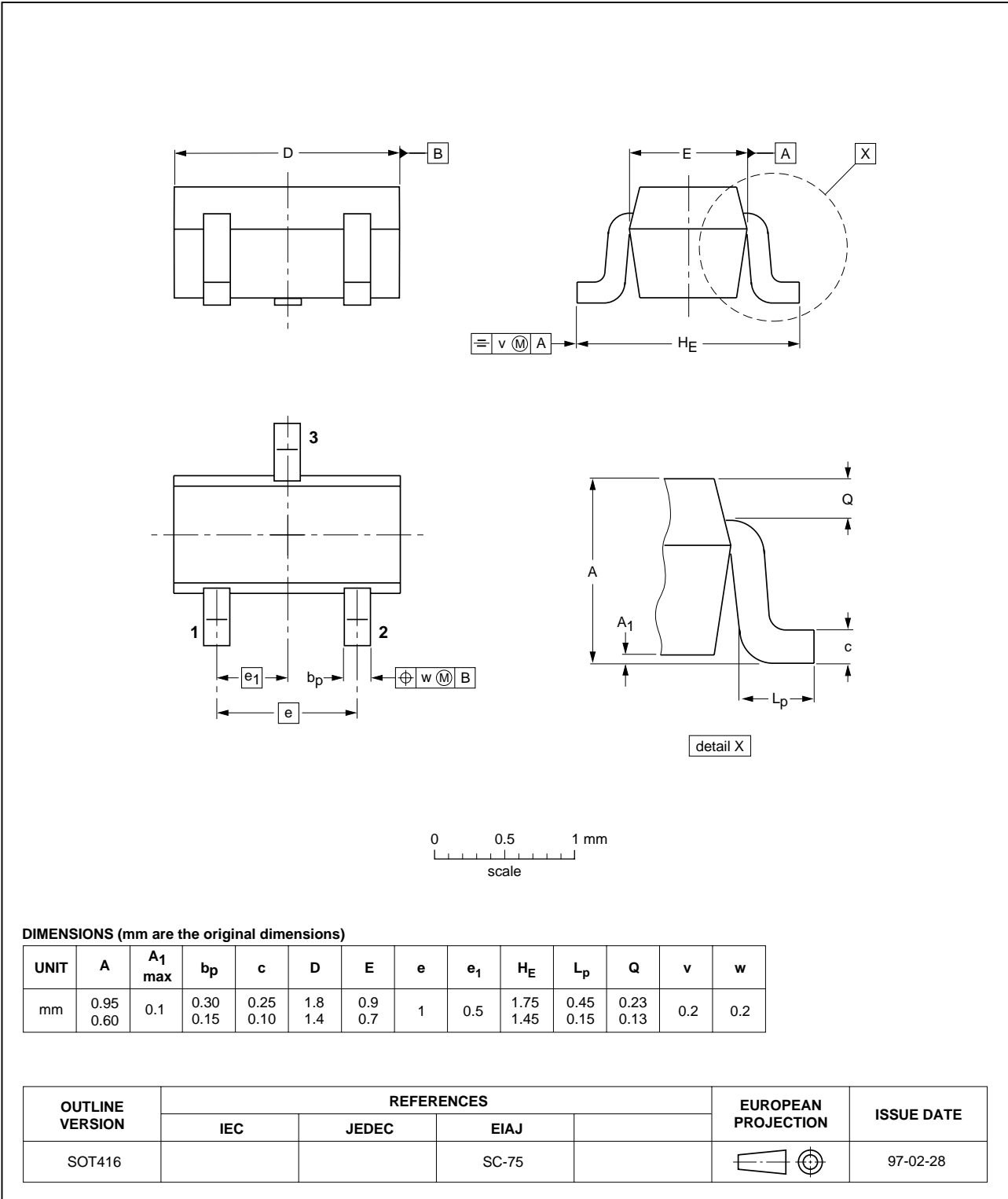
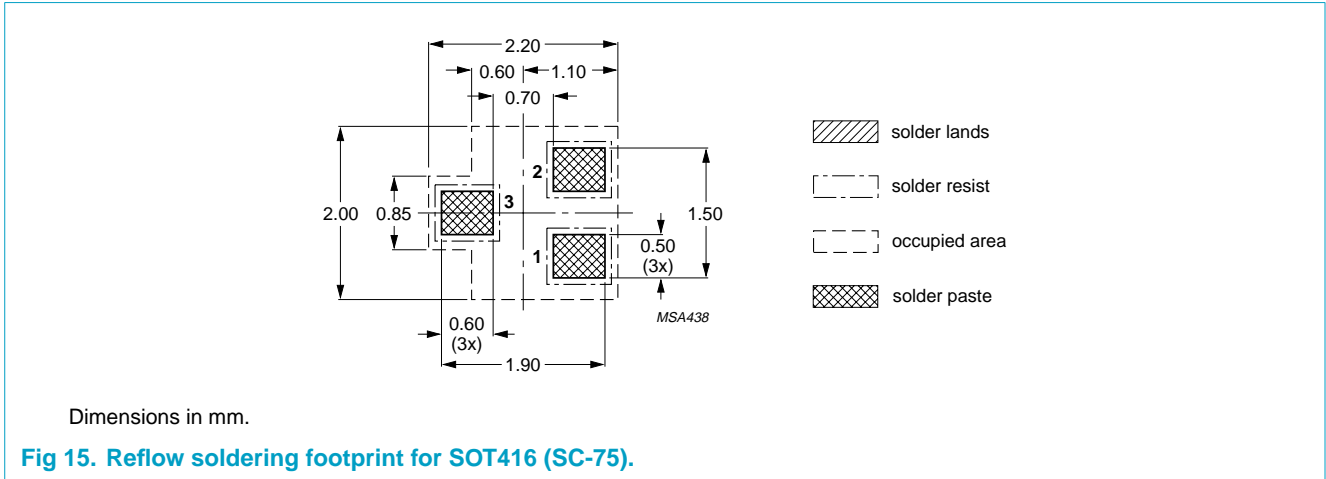


Fig 14. SOT416 (SC-75).

8. Soldering



9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040305	-	Product data (9397 750 12662)

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	1
4	Limiting values	2
5	Thermal characteristics	4
5.1	Transient thermal impedance	4
6	Characteristics	5
7	Package outline	9
8	Soldering	10
9	Revision history	10
10	Data sheet status	11
11	Definitions	11
12	Disclaimers	11
13	Trademarks	11

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