PIC16(L)F183XX

PIC16(L)F183XX Memory Programming Specification

1.0 OVERVIEW

The PIC16(L)F183XX Memory Programming Specification describes the method for programming the 8-bit PIC16(L)F183XX family of microcontrollers. The programming specification describes the programming commands, programming algorithms and electrical specifications which are necessary for programming. Part-specific information can be found in the Appendix sections (Appendix B to Appendix E). Each appendix contains individual part numbers, device identification and checksum values, pinout and packaging information and Configuration Words. Table 1-1 below lists specific part numbers.

TABLE 1-1: DEVICE APPENDIX LOCATION

Device	Appendix
PIC16(L)F18313	Appendix B
PIC16(L)F18323	Appendix B
PIC16(L)F18324	Appendix C
PIC16(L)F18325	Appendix D
PIC16(L)F18326	Appendix E
PIC16(L)F18344	Appendix C
PIC16(L)F18345	Appendix D
PIC16(L)F18346	Appendix E

1.1 Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming (ICSP) interface. Data can be programmed into the Program Flash Memory, EEPROM and the Configuration Words.

1.2 Write and/or Erase Selection

Erasing or writing is selected according to the command used to begin operation (see Table 3-1). The terms are defined in Table 1-2 and are detailed below.

TABLE 1-2: PROGRAMMING TERMS

Term	Definition
Programmed Cell	A memory cell with a logic '0'
Erased Cell	A memory cell with a logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic Erase and/ or Write

1.2.1 ERASING MEMORY

Memory is erased by row or in bulk, where 'bulk' includes many subsets of the total memory space. The duration of the erase is always determined internally. All Bulk ICSP Erase commands have minimum VDD requirements, which prevent breach of code protection by ensuring sufficient VDD voltages.

1.2.2 WRITING MEMORY

Memory is written one row at a time. Multiple load data for NVM commands are used to fill the row data latches. The duration of the write can be determined either internally or externally.

1.2.3 MULTI-WORD PROGRAMMING INTERFACE

Program Flash memory panels include up to a 32-word (one row) programming interface. The row to be programmed must first be erased either with a Bulk Erase or a Row Erase.

1.3 Hardware Requirements

1.3.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for VDD and one for the MCLR/VPP pin.

1.3.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP mode, the device can be programmed using a single VDD source in the operating range. The MCLR/VPP pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP Programming

The LVP bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a ‘1’ (enabled) from the factory. The LVP bit may only be programmed to ‘0’ by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to VIHH. Once the LVP bit is programmed to a ‘0’, only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

> **Note 1:** The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR/VPP pin.
>
> **2:** While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

1.4 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in Table 1-3. For pin locations and packaging information please refer to Table B-2 through Table E-2.

TABLE 1-3: PIN DESCRIPTIONS DURING PROGRAMMING

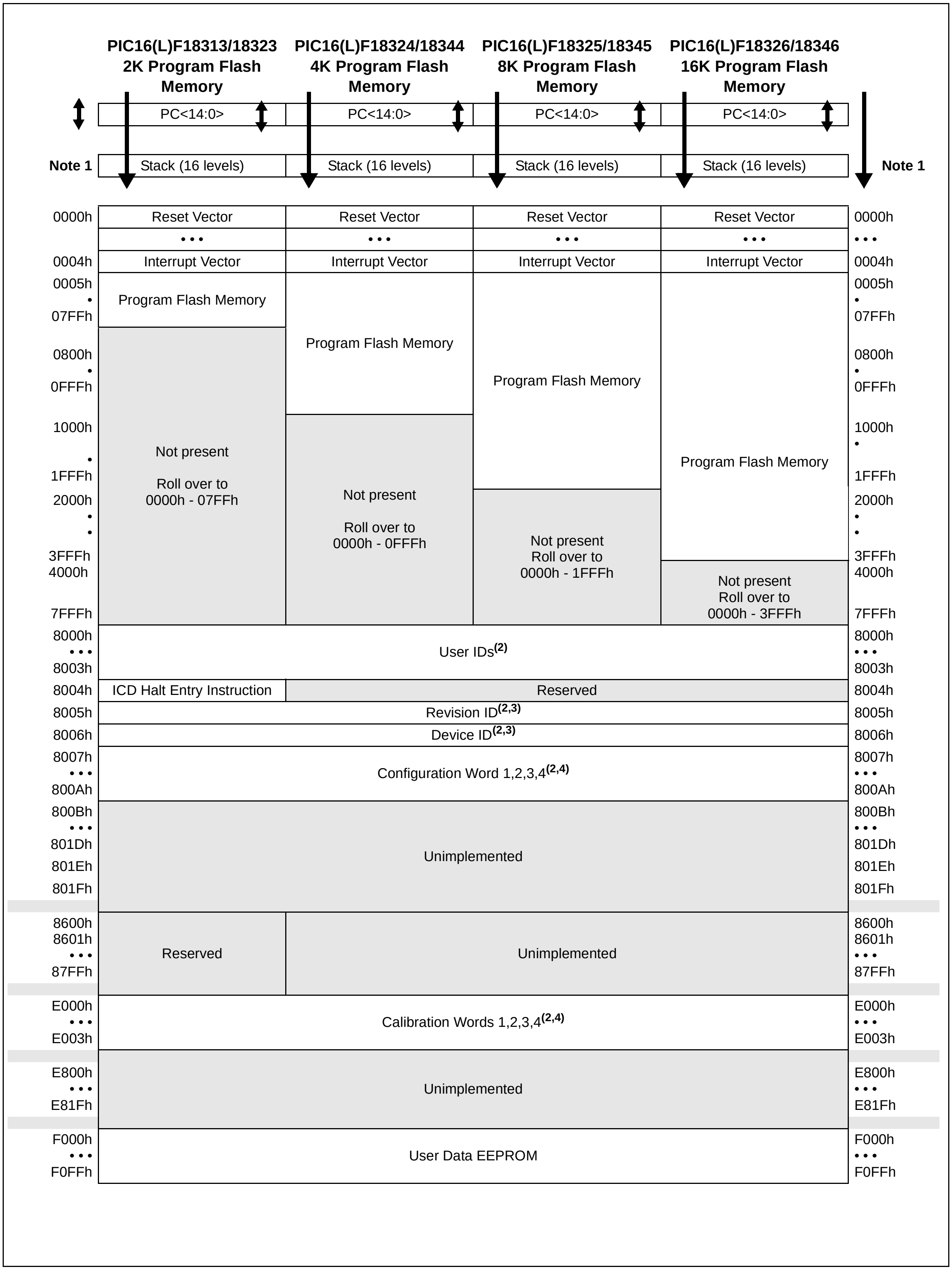
Pin Name	During Programming		
	Function	Pin Type	Pin Description
ICSPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ICSPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
MCLR/VPP	Program/Verify mode	P(1)	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current.

2.0 MEMORY MAP

FIGURE 2-1: PROGRAM MEMORY MAPPING



2.1 User ID Location

A user may store identification information (User ID) in four designated locations. The User ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

2.2 Device/Revision ID

The 14-bit device ID word is located at 8006h and the 14-bit revision ID is located at 8005h. These locations are read-only and cannot be erased or modified.

REGISTER 2-1: DEVICEID: DEVICE ID REGISTER(1)

R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEV<13:0>													
bit 13													bit 0

Legend:		
R = Readable bit		
'0' = Bit is cleared	'1' = Bit is set	x = Bit is unknown

bit 13-0 **DEV<13:0>:** Device ID bits
Refer to Table B-1 through Table E-1 to determine what these bits will read on each device. A value of 3FFFh or 0000h is invalid.

Note 1: This location cannot be written.

REGISTER 2-2: REVISIONID: REVISION ID REGISTER(1)

R	R	R	R	R	R	R	R	R	R	R	R	R	R
REV<13:0>													
bit 13													bit 0

Legend:		
R = Readable bit		
'0' = Bit is cleared	'1' = Bit is set	x = Bit is unknown

bit 13-0 **REV<13:0>:** Revision ID bits
These bits are used to identify the device revision.

Note 1: This location cannot be written.

2.3 Configuration Words

The devices have several Configuration Words starting at address 8007h. The individual bits within these Configuration Words are critical to the correct operation of the system. Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, these important Configuration bits should be considered:

1. **LVP: Low-Voltage Programming Enable bit**

- `1 = ON` – Low-Voltage Programming is enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
- `0 = OFF` – HV on $\overline{MCLR}/V_{PP}$ must be used for programming.

It is important to note that the LVP bit cannot be written (to `0`) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the configuration state. For more information, see **Section 3.1.2 “Low-Voltage Programming (LVP) Mode”**.

2. **$\overline{CPD}$: Data NVM Memory Code Protection bit**

- `1 = OFF` – Data NVM code protection disabled
- `0 = ON` – Data NVM code protection enabled

3: **$\overline{CP}$: User NVM Program Memory Code Protection bit**

- `1 = OFF` – User NVM code protection disabled
- `0 = ON` – User NVM code protection enabled

For more information on code protection, see **Section 3.3 “Code Protection”**.

2.4 Calibration Words

The internal calibration values are factory calibrated and stored in the Calibration Word locations. Calibration words are located beginning at address E000h.

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

3.0 PROGRAMMING ALGORITHMS

3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

3.1.1 HIGH-VOLTAGE PROGRAM/VERIFY MODE ENTRY AND EXIT

There are two different modes of entering Program/Verify mode via high voltage:

- VPP – First Entry mode
- VDD – First Entry mode

3.1.1.1 VPP – First Entry Mode

To enter Program/Verify mode via the VPP-first method, the following sequence must be followed:

3. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
4. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
5. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-First entry prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Word has $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the power-up time is disabled ($\overline{\text{PWRTE}}$ = 0), the internal oscillator is selected (RSTOSC = HFINTOSC or LFINTOSC), and RA0 and RA1 are driven by the user application, the device will execute code. Since this may prevent entry, VPP-First Entry mode is strongly recommended. See the timing diagram in Figure 3-20.

3.1.1.2 VDD – First Entry Mode

To enter Program/Verify mode via the VDD-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to VIHH.

The VDD-First Entry mode is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 3-19.

3.1.1.3 Program/Verify Mode Exit

To exit Program/Verify mode, take $\overline{\text{MCLR}}$ to VDD or lower (VIL). VDD-First Entry mode should use VDD-Last Exit mode (see Figure 3-19). VPP-First Entry mode should use VPP-Last Exit mode (see Figure 3-20).

3.1.2 LOW-VOLTAGE PROGRAMMING (LVP) MODE

The Low-Voltage Programming mode allows the devices to be programmed using VDD only, without high voltage. When the LVP bit of the Configuration Word 3 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to VIL;
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK. 32 clocks are required to match the sequence pattern, and a 33rd clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 3-24 and Figure 3-25.

Exiting Program/Verify mode is done by no longer driving $\overline{MCLR}$ to VIL (see Figure 3-24 and Figure 3-25).

Note:	To enter LVP mode, the LSb of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

3.1.3 PROGRAM/VERIFY COMMANDS

These devices implement ten programming commands, each six bits in length. The commands are summarized in Table 3-1. The commands are used to erase and program the device. The commands load and use the Program Counter (PC).

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay, 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 3-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data for NVM	J[(1)]	0	0	0	1	0	02h/22h	0, data (14), 0
Read Data from NVM	J[(1)]	0	0	1	0	0	04h/24h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	PC = PC + 1
Load PC Address	x	1	1	1	0	1	1Dh	0, data (22), 0
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Memory	x	0	0	1	0	1	05h	Internally Timed

Note 1: When J = 1, the Program Counter is automatically incremented by 1 (PC +1) and does not require an 'Increment Address' command to move the PC to the next address. When J = 0, the Program Counter is not incremented, therefore either a 'Load PC address' or 'Increment Address' command is required to move the PC to the next address.

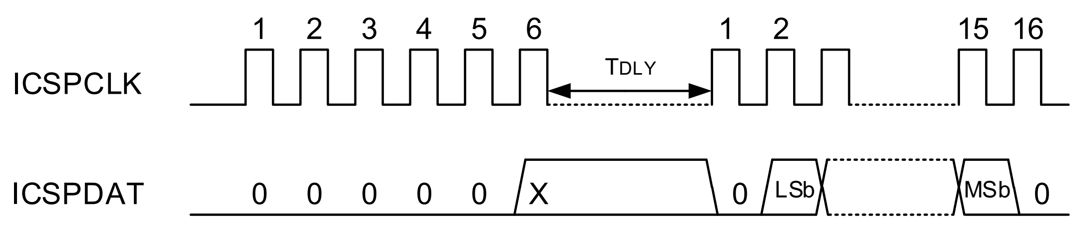
3.1.3.1 Load Configuration

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 3-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or the Begin Externally Timed Programming command.

> **Note:** Externally-timed writes are not supported for Configuration and Calibration bits. Any externally-timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 3-1: LOAD CONFIGURATION



3.1.3.2 Load Data for NVM

The Load Data for NVM command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 3-2).

One data word is latched into the Write Data register corresponding to the current Program Counter's LSbs. Depending on the value of bit 5 of the command, the PC may or may not be incremented (see Table 3-1).

The Load Data for NVM command can also be used to load data for data EEPROM. After the 8-bit data word is loaded, the remaining six bits of the 14-bit word will be '0's (see Figure 3-3).

FIGURE 3-2: LOAD DATA FOR NVM PROGRAM FLASH MEMORY

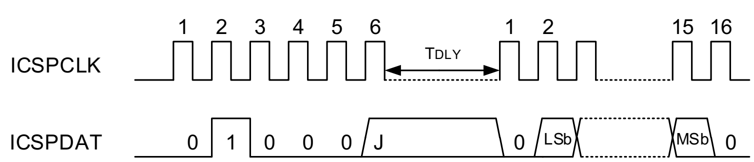
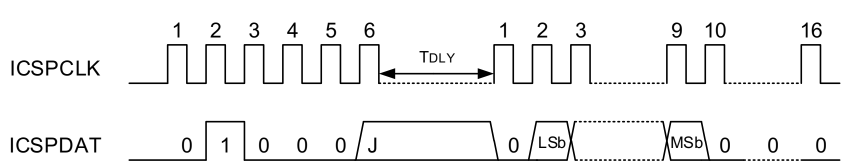


FIGURE 3-3: LOAD DATA FOR NVM EEPROM



3.1.3.3 Read Data from NVM

The Read Data from NVM command will transmit data bits out of the current PC address, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 3-4 and Figure 3-5). Depending on the value of bit 5 of the command, the PC may or may not be incremented (see Table 3-1).

FIGURE 3-4: READ DATA FROM NVM PROGRAM FLASH MEMORY

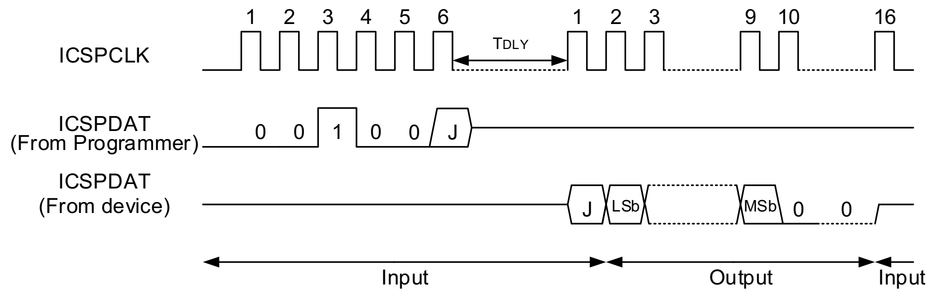
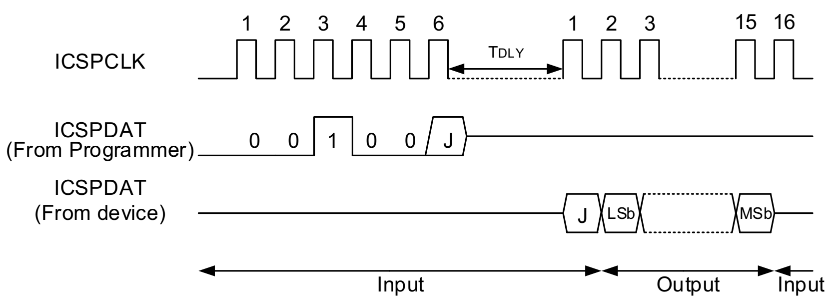


FIGURE 3-5: READ DATA FROM NVM EEPROM

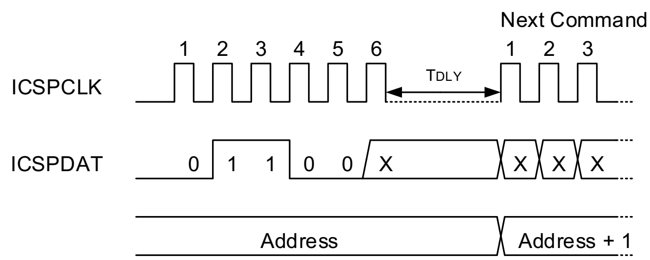


3.1.3.4 Increment Address

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must exit Program/Verify mode and re-enter it. Instead of using multiple Increment Address commands to get to a certain address, the user may choose to use the Load PC Address command.

If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h (see Figure 3-6).

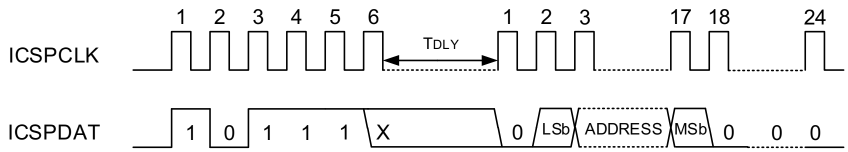
FIGURE 3-6: INCREMENT ADDRESS



3.1.3.5 Load PC Address

The PC value is set using the supplied data. The address implies the memory panel (Program Flash Memory or EEPROM) to be accessed. If the memory panel has fewer than 16 address bits, the MSbs are ignored (see Figure 3-7).

FIGURE 3-7: LOAD PC ADDRESS

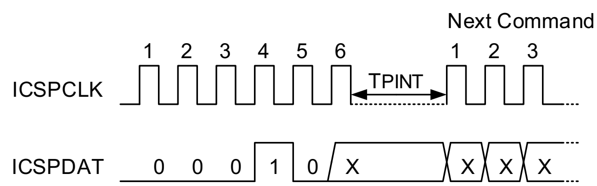


3.1.3.6 Begin Internally Timed Programming

A Load Configuration or Load Data for NVM command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, in order for the programming to complete. End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed (see Figure 3-8).

FIGURE 3-8: BEGIN INTERNALLY TIMED PROGRAMMING

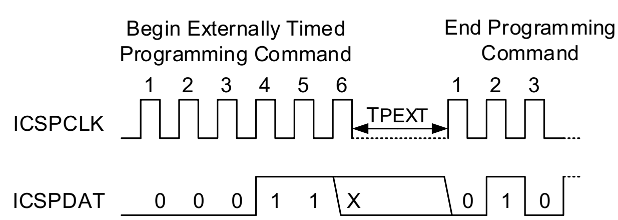


3.1.3.7 Begin Externally Timed Programming

A Load Configuration or Load Data for NVM command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 3-9).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 3-9: BEGIN EXTERNALLY TIMED PROGRAMMING

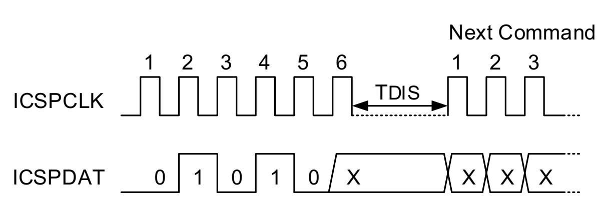


3.1.3.8 End Programming

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 3-10).

FIGURE 3-10: END PROGRAMMING



3.1.3.9 Bulk Erase Memory

The Bulk Erase Memory command performs different functions dependent on the current state of the address.The Bulk Erase command affects specific portions of the memory depending on the initial value of the Program Counter. Whenever a Bulk Erase command is executed, the device will address the regions listed in Table 3-2 and proceed in the order shown. The specific order shown is designed to ensure the integrity of the device code protection.

TABLE 3-2: BULK ERASE

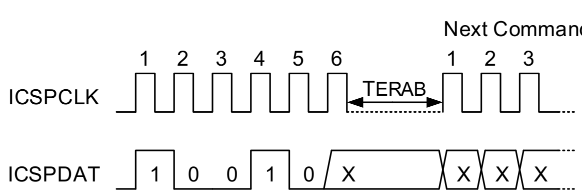
Address	Area(s) Erased[1]	
	$\overline{CP}$ = 1 and $\overline{CPD}$ = 1 (both disabled)	**$\overline{CP}$ = 0 or $\overline{CPD}$ = 0 (either enabled)**
0000h-7FFFh	Program Memory Configuration Words[2]	Program Memory EEPROM Configuration Words[2]
8000h-83FFh	Program Memory User ID Locations Configuration Words[2]	Program Memory EEPROM User ID Locations Configuration Words[2]
8400h-84FFh[4]	Program Memory User ID Locations	Program Memory EEPROM User ID Locations
8500h-85FFh[4]	Program Memory	Program Memory EEPROM
E800h-EFFFh	Program Memory EEPROM User ID Locations Configuration Words[2]	Program Memory EEPROM User ID Locations Configuration Words[2]
F000h-FFFFh	EEPROM	EEPROM

Note 1: Based on the address, memory areas will be erased in the shown order.

2: Configuration Word 4 will be erased and the current protection state may be removed; this operation is performed last.

After receiving the Bulk Erase Memory command, the erase will not complete until the time interval, T_{ERAB}, has expired (see Figure 3-11).

FIGURE 3-11: BULK ERASE MEMORY

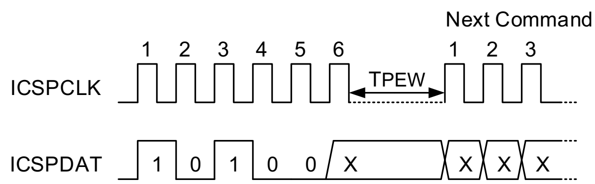


3.1.3.10 Row Erase Memory

The Row Erase Memory command will erase an individual row. When Program Flash memory write and erase operations are done on a row basis, the row size (number of 14-bit words) for the erase operation is 32, and the row size (number of 14-bit latches) for the write operation is 32. When EEPROM write and erase operations are done on a row basis, the row size (number of 8-bit words) for erase operations is 1, and the row size (number of 8-bit latches) is also 1. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-800Ah, the Row Erase Program Memory command will only erase the User ID locations regardless of the setting of the $\overline{\text{CP}}$ Configuration bit.

The Flash memory row defined by the current PC will be erased. The user must wait TPEW for erasing to complete in Program Flash Memory and EEPROM rows, or TPEWCC for Configuration or Calibration data (see Table 3-4). An End Programming command is not required (see Figure 3-12).

FIGURE 3-12: ROW ERASE MEMORY



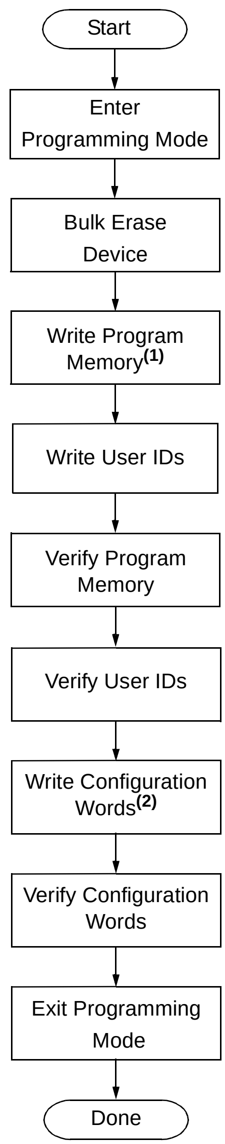
3.2 Programming Algorithms

The devices use internal latches to temporarily store the 14-bit words used for programming. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which memory row is written. Writes cannot cross a physical row boundary. For example, attempting to write from address 0002h-0021h in a 32-latch device will result in data being written to 0020h-003Fh.

If more than the maximum number of latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. Figure 3-13 through Figure 3-18 show the recommended flowcharts for programming.

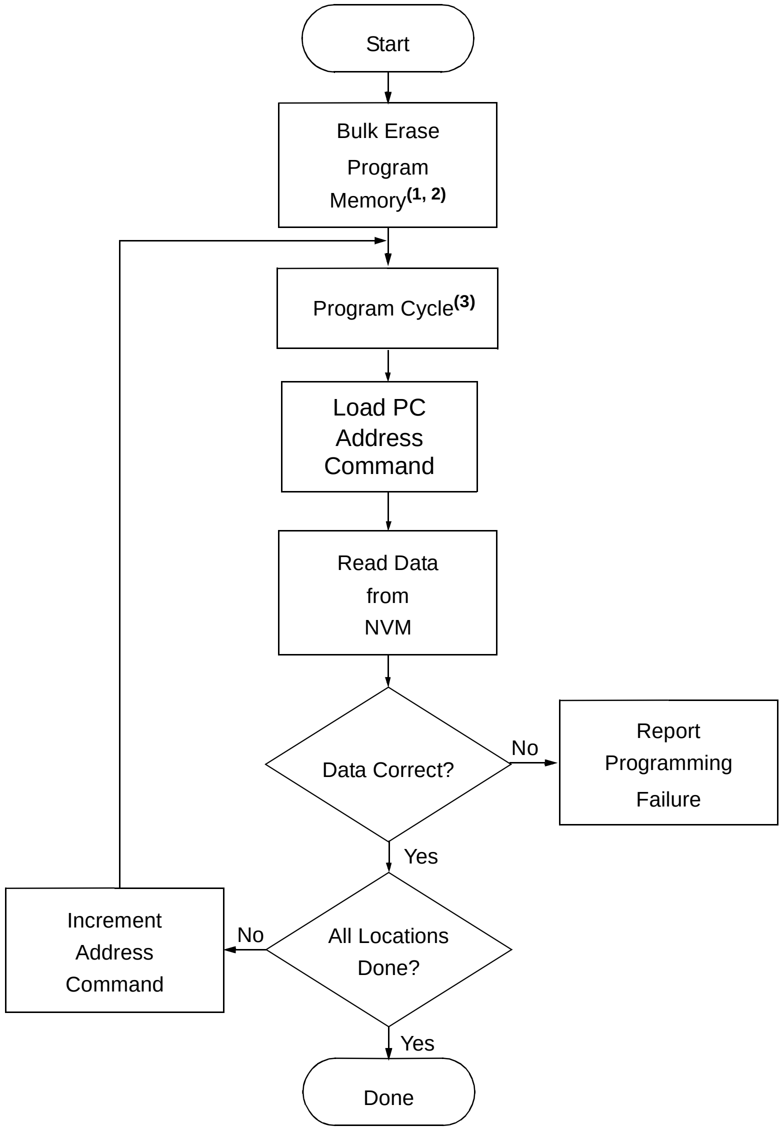
FIGURE 3-13: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See Figure 3-14.

2: See Figure 3-17.

FIGURE 3-14: PROGRAM MEMORY FLOWCHART

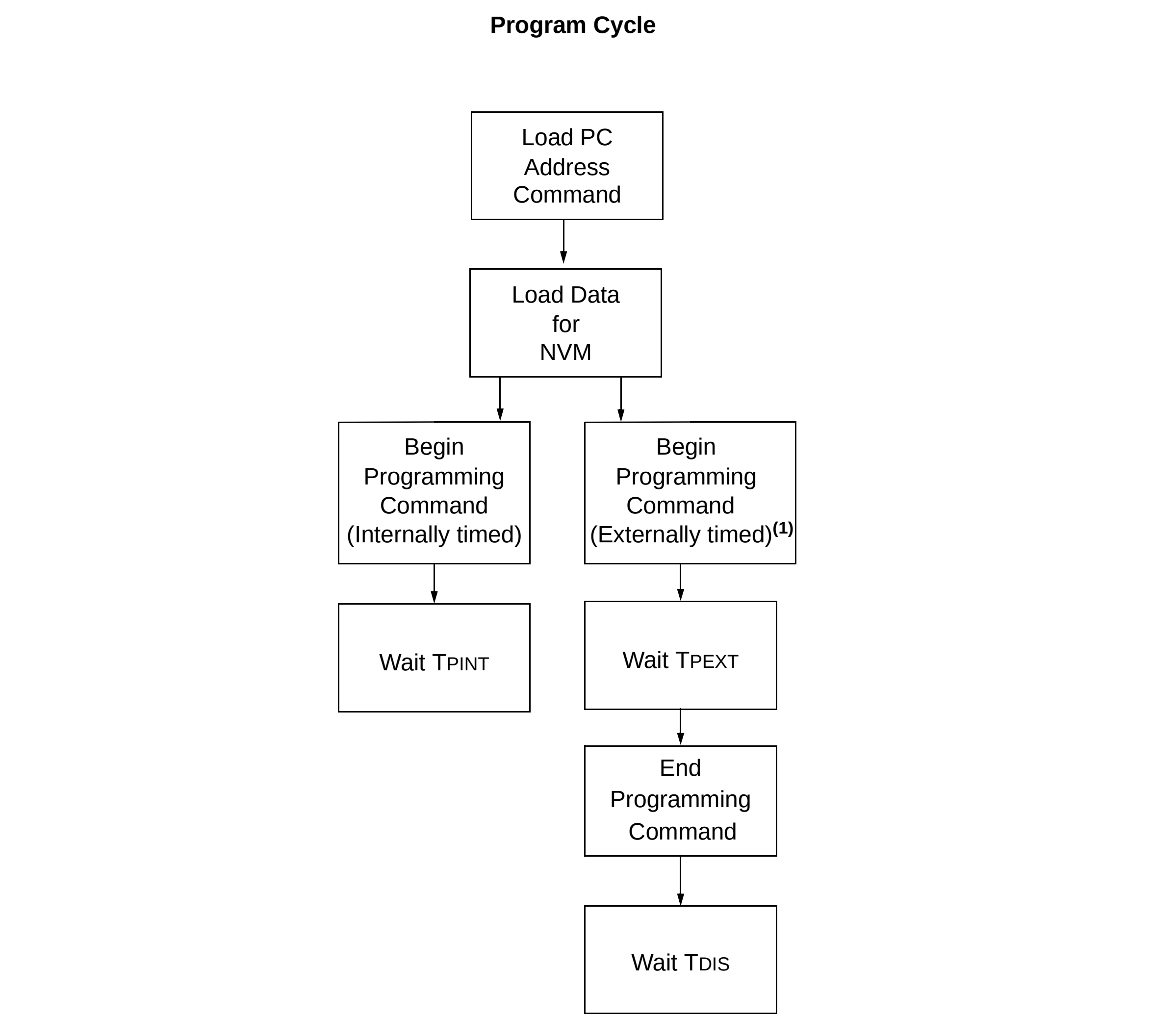


Note 1: This step is optional if the device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 3-18.

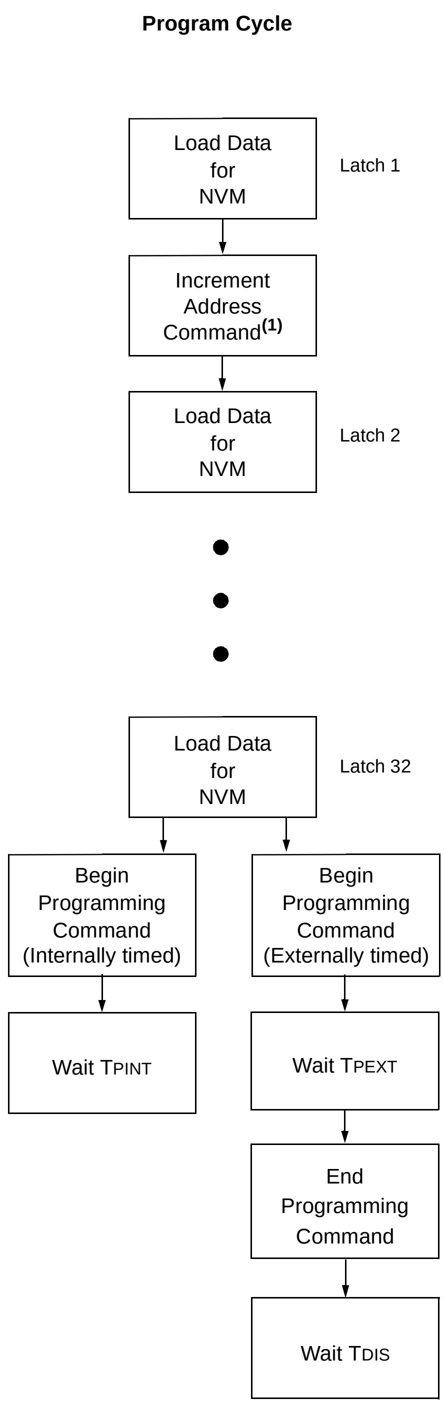
3: See Figure 3-15 or Figure 3-16.

FIGURE 3-15: ONE-WORD PROGRAM CYCLE



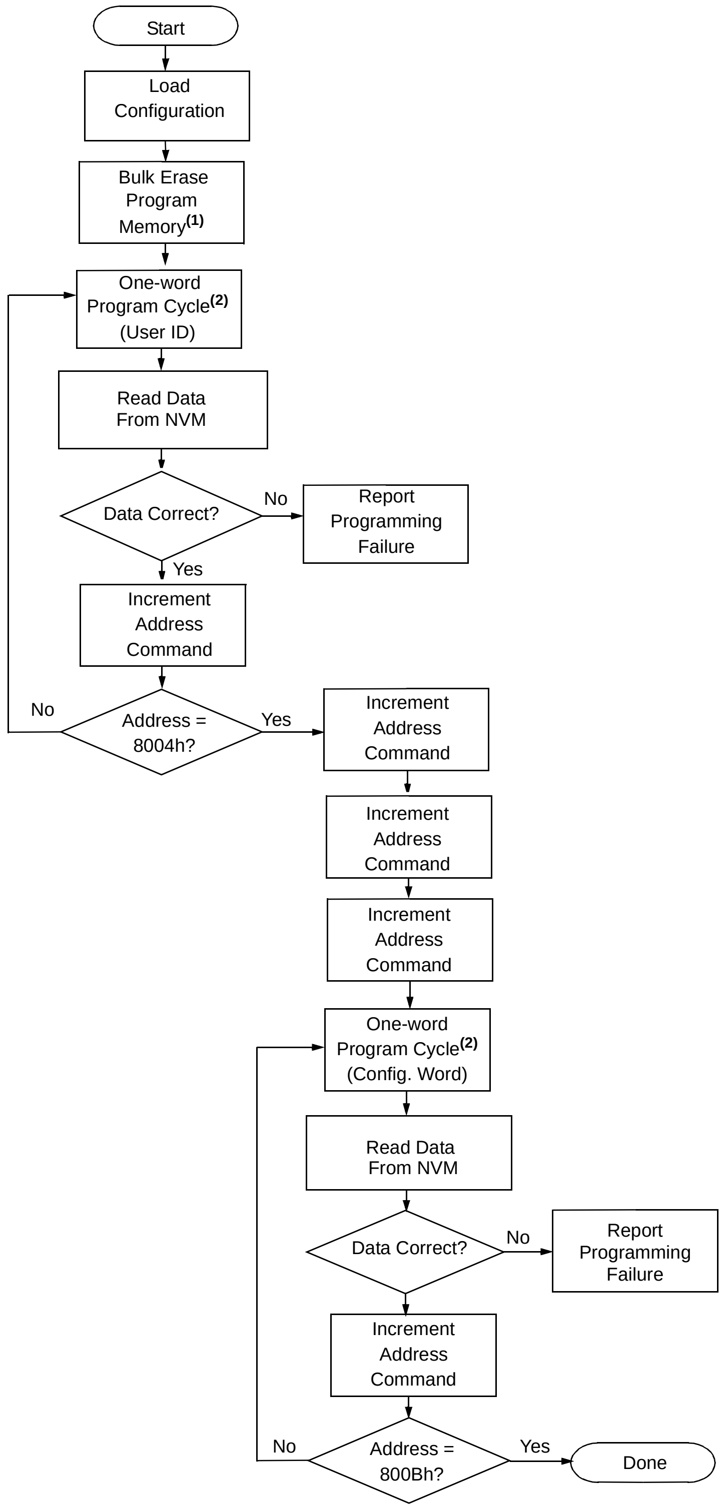
Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 3-16: MULTIPLE-WORD PROGRAM CYCLE



Note 1: This command is only necessary if the ‘Load Data for NVM’ command = 02h; when the ‘Load Data for NVM’ command = 22h, the PC automatically increases by one. See Table 3-2 for more information.

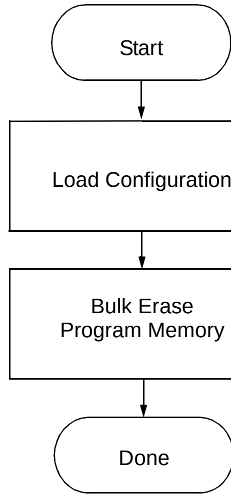
FIGURE 3-17: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if the device is erased or not previously programmed.

2: See Figure 3-15.

FIGURE 3-18: ERASE FLOWCHART



Note: This sequence does not erase the Calibration Words.

3.3 Code Protection

Code protection is controlled using the $\overline{\text{CP}}$ bit. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh). Program memory can still be programmed and read during program execution.

The User ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

3.3.1 PROGRAM MEMORY

Code protection is enabled by programming the $\overline{\text{CP}}$ bit to '0'.

The only way to disable code protection is to use the Bulk Erase Memory command.

3.3.2 DATA EEPROM

Data EEPROM protection is enabled by programming the $\overline{\text{CPD}}$ bit to '0'.

The only way to disable code protection is to use the Bulk Erase Memory command.

3.4 Hex File Usage

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. For example, if the Configuration Word 1 is stored at 8007h, in the hex file this will be referenced as 1000Eh-1000Fh. The PIC16(L)F183XX family allows direct addressing for the data EEPROM, so the EEPROM data will appear at address 0xF000 in the hex file.

3.4.1 CONFIGURATION WORD

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and User ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and User ID information should be included.

3.4.2 DEVICE ID

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID against the value read from the part. On a mismatch condition, the programmer should generate a warning message.

3.4.3 CHECKSUM COMPUTATION

The checksum is calculated by two different methods dependent on the setting of the $\overline{\text{CP}}$ Configuration bit.

3.4.3.1 Program Code Protection Disabled

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location (e.g., 0FFFh). Any Carry bits exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

3.4.3.2 Program Code Protection Enabled

The code protected checksums located in Tables B1 through E1 are calculated with the unprotected checksum located in the User ID memory locations. When using MPLAB® X IDE, the unprotected checksum can be automatically calculated and inserted into the User ID locations by selecting 'Project Properties' under the 'File' tab. A new window will appear. In the 'Categories' section, click on the 'Building' selection, then add a check to the 'Insert unprotected checksum in User ID memory' check box. The user can also choose to manually write the unprotected checksum into the User ID locations. Each nibble of the unprotected checksum is stored in the Least Significant nibble of each of the four User ID locations. The Most Significant checksum nibble is stored in the User ID at location 8000h, the second Most Significant nibble is stored at location 8001h, and so forth for the remaining nibbles and ID locations.

The checksum of a code-protected device is computed in the following manner: the Least Significant nibble of each User ID is used to create a 16-bit value. The Least Significant nibble of User ID location 8000h is the Most Significant nibble of the 16-bit value. The Least Significant nibble of User ID location 8001h is the second Most Significant nibble, and so forth for the remaining User IDs and 16-bit value nibbles. The resulting 16-bit value is summed with the Configuration Words. All unimplemented Configuration bits are masked to '0'.

3.5 Electrical Specifications

Refer to device specific data sheet for absolute maximum ratings.

TABLE 3-3: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
	Programming Supply Voltages and Currents					
VDD	Supply Voltage (VDDMIN[(2)], VDDMAX) — PIC16LF183XX	1.80 2.50	—	3.60 3.60	V V	FOSC ≤ 16 MHz FOSC > 16 MHz
	Supply Voltage (VDDMIN[(2)], VDDMAX) — PIC16F183XX	2.30 2.50	—	5.50 5.50	V V	FOSC ≤ 16 MHz FOSC > 16 MHz
VPEW	Read/Write and Row Erase operations	VDDMIN	—	VDDMAX	V	
VBE	Bulk Erase operations	2.7	—	VDDMAX	V	
IDDI	Current on VDD, Idle	—	—	1.0	mA	
IDDP	Current on VDD, Programming	—	—	3.0	mA	
	VPP					
IPP	Current on $\overline{\text{MCLR}}$/VPP	—	—	600	μA	
VIHH	High voltage on $\overline{\text{MCLR}}$/VPP for Program/Verify mode entry	8.0	—	9.0	V	
TVHHR	$\overline{\text{MCLR}}$ rise time (VIL to VIHH) for Program/Verify mode entry	—	—	1.0	μs	
	I/O pins					
VIH	(ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}$/VPP) input high level	0.8 VDD	—	—	V	
VIL	(ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}$/VPP) input low level	—	—	0.2 VDD	V	
VOH	ICSPDAT output high level	VDD-0.7 VDD-0.7 VDD-0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 1 mA, VDD = 1.8V
VOL	ICSPDAT output low level	—	—	VSS+0.6 VSS+0.6 VSS+0.6	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 1 mA, VDD = 1.8V
VBOR	Brown-out Reset Voltage: BORV = 0 (high trip)	—	2.70	—	V	PIC16(L)F183XX
	BORV = 1 (low trip)	— —	2.45 1.90	— —	V V	PIC16F183XX PIC16LF183XX
	Programming Mode Entry and Exit					
TENTS	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or $\overline{\text{MCLR}}$↑	100	—	—	ns	
TENTH	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or $\overline{\text{MCLR}}$↑	250	—	—	μs	
	Serial Program/Verify					
TCKL	Clock Low Pulse Width	100	—	—	ns	
TCKH	Clock High Pulse Width	100	—	—	ns	
TDS	Data in setup time before clock↓	100	—	—	ns	
TDH	Data in hold time after clock↓	100	—	—	ns	
TCO	Clock↑ to data out valid (during a Read Data command)	0	—	80	ns	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

2: Bulk-erased devices default to brown-out enabled. VDDMIN is 2.85 volts when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

TABLE 3-3: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE (CONTINUED)

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
TLZD	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	
TDLY	Data input not driven to next clock input (delay required between command/data or command/ command)	1.0	—	—	μs	
TERAB	Bulk Erase cycle time	—	—	5	ms	
TERAR	Row Erase cycle time	—	—	2.5	ms	
TPINT	Internally timed programming operation time	— —	— —	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	**Note 1**
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.
2: Bulk-erased devices default to brown-out enabled. VDDMIN is 2.85 volts when performing low-voltage programming on a bulk-erased device, to ensure that the device is not held in Brown-out Reset.

TABLE 3-4: FLASH MEMORY CHARACTERISTICS

Program Flash Memory Characteristics		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Sym.	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
	Program Flash Memory					
EP	Cell Endurance	10k	—	—	E/W	Temperature during programming
	VDD for Read	VDD(MIN)	—	VDD(MAX)	V	
	Voltage on $\overline{\text{MCLR}}$/VPP during Erase/Program	7.9	—	9.0	V	
	VDD for Bulk Erase	VBORMAX	—	VDD(MAX)	V	At BOR = 2.45V At VDD = VDD(MIN)
VPEW	VDD for Write or Row Erase	VDD(MIN)	—	VDD(MAX)	V	
IDDPGM	Current on VDD during Erase/ Write	—	—	5.0	mA	
TPEW	Erase/Write cycle time	—	—	2.8	ms	All except Configuration and Calibration bits
TPEWCC	Erase/Write cycle time, configuration and calibration bits	—	2 x TPEW	—	ms	
TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

† Data in ‘Typ.’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3.5.1 AC TIMING DIAGRAMS

FIGURE 3-19: PROGRAMMING ENTRY AND EXIT MODES – VDD FIRST AND LAST

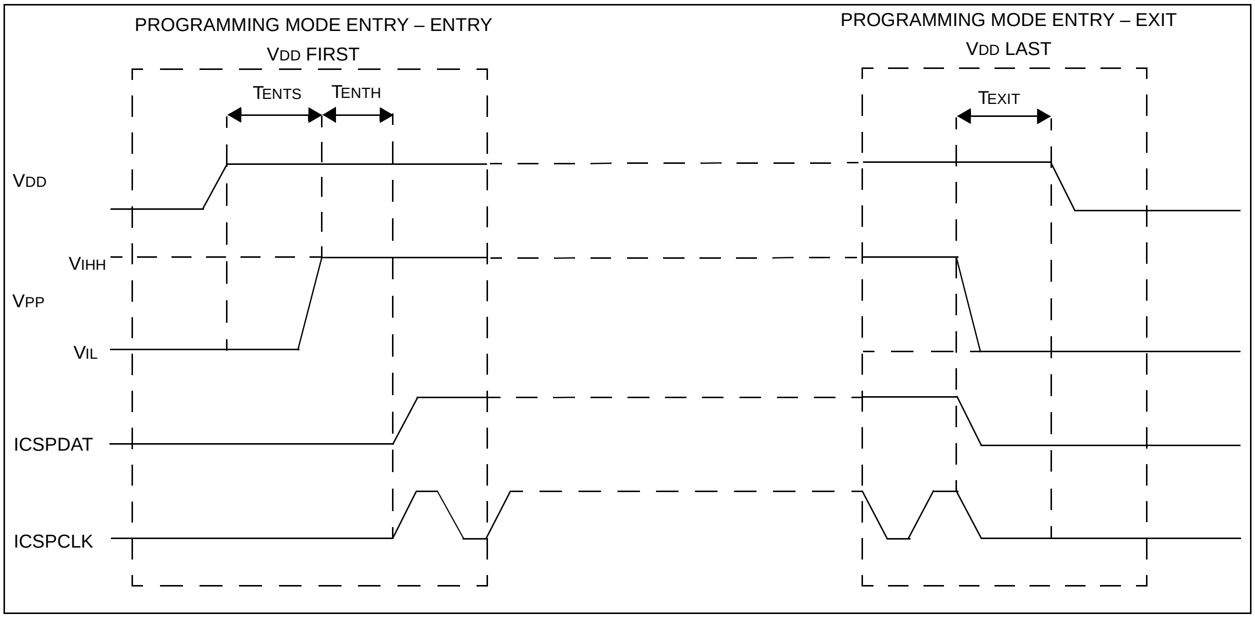


FIGURE 3-20: PROGRAMMING ENTRY AND EXIT MODES – VPP FIRST AND LAST

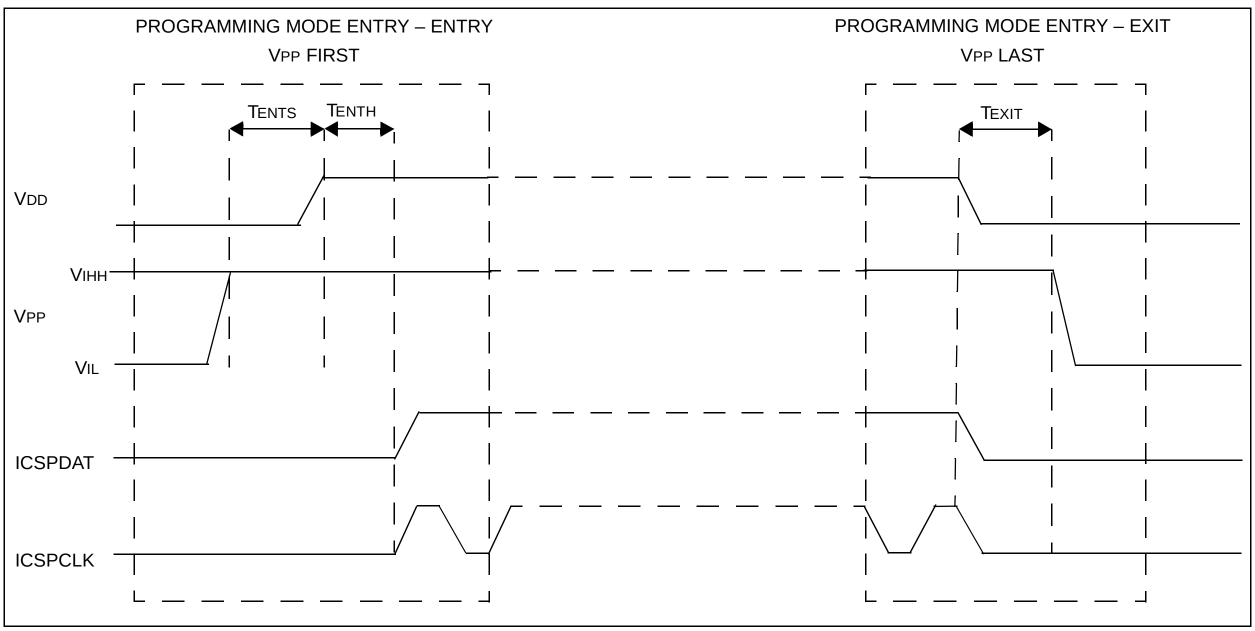


FIGURE 3-21: CLOCK AND DATA TIMING

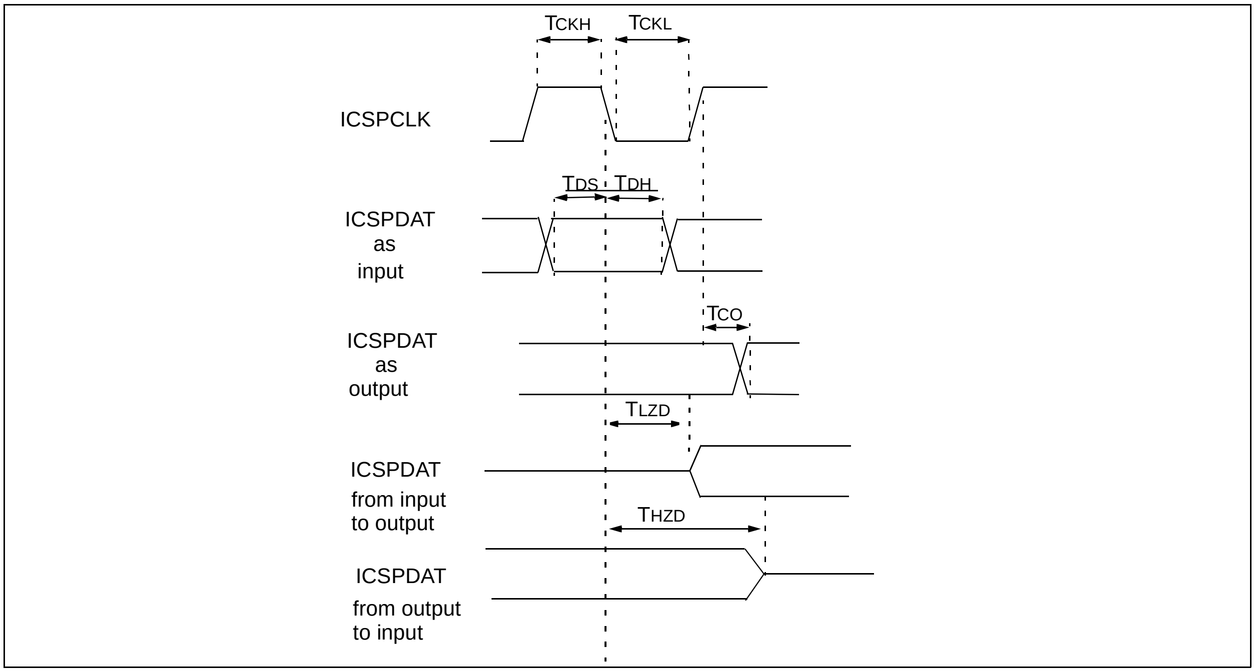


FIGURE 3-22: WRITE COMMAND – PAYLOAD TIMING

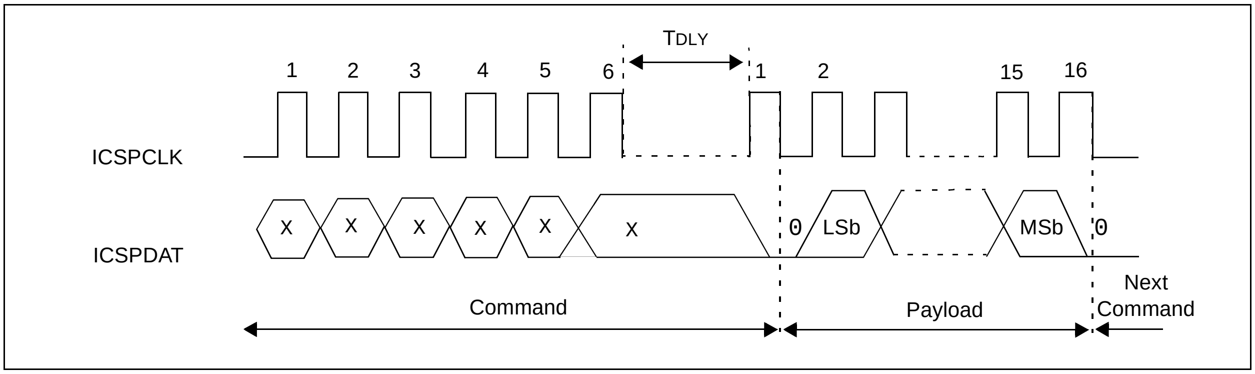


FIGURE 3-23: READ COMMAND – PAYLOAD TIMING

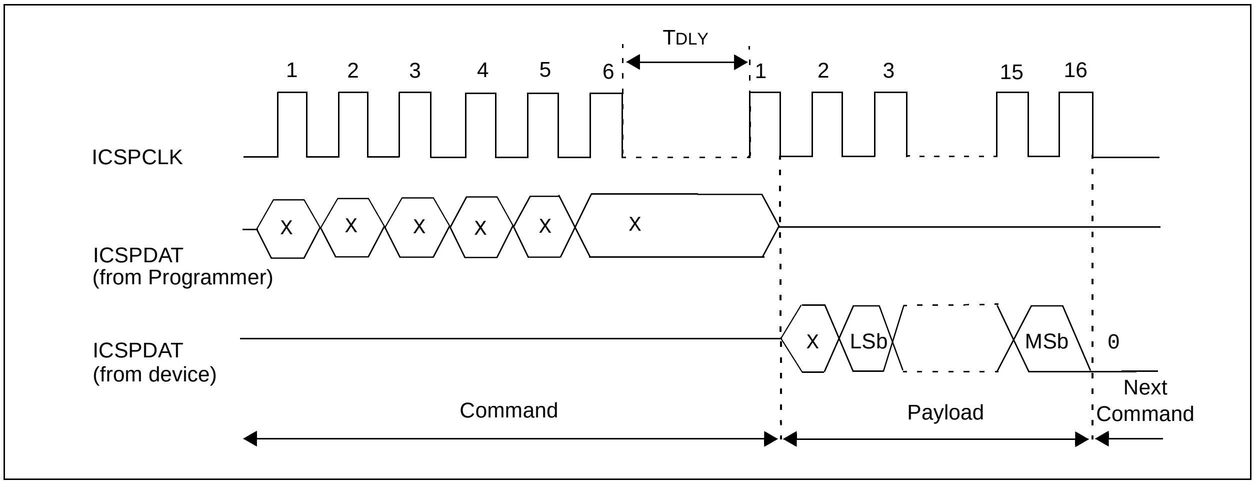


FIGURE 3-24: LVP ENTRY (POWERING-UP)

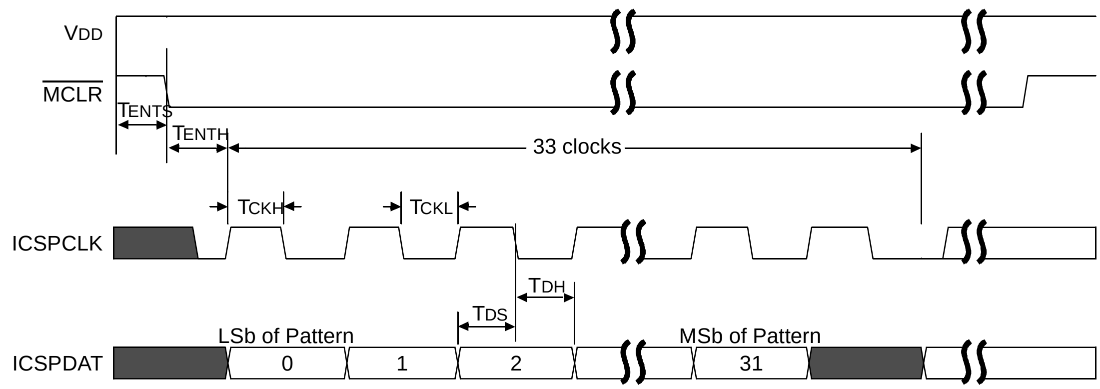
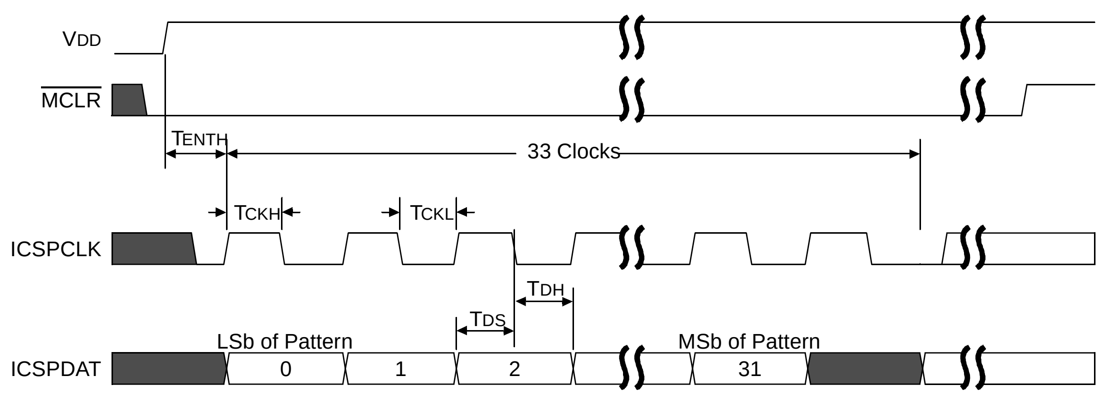


FIGURE 3-25: LVP ENTRY (POWERED)



Note: Sequence matching can start with no edge on $\overline{\text{MCLR}}$ first.

APPENDIX A: REVISION HISTORY

Revision A (03/2014)

Initial release of this document.

Revision B (04/2014)

Updated Device IDs for the PIC16(L)F18313 and PIC16(L)F18323 devices in Table B-1; Updated Tables C-2 and D-2; Updated Registers B-1 and C-1; Other minor corrections.

Revision C (04/2015)

Updated Table 1-1 and Table 3-1; Updated Figure 3-1 to Figure 3-12; Added new Appendix B; Other minor corrections.

Revision D (01/2016)

Updated Figure 2-1, 3.1.3.10 Section, Table 3-4. Updated Appendix B, C and D; Added Appendix E; Other minor corrections.

APPENDIX B: PIC16(L)F18313 AND PIC16(L)F18323 DEVICE ID, CHECKSUMS AND PINOUT DESCRIPTIONS

TABLE B-1: DEVICE IDs AND CHECKSUMS

Device	Device ID	Config. 1		Config. 2		Config. 3		Config. 4			Checksum			
											Unprotected		Code-Protected[(1)]	
		Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Unprotected Word (HEX)	Protected Word (HEX)	Mask (HEX)	Blank (HEX)	00AAh First and Last (HEX)	Blank (HEX)	00AAh First and Last (HEX)
PIC16F18313	3066	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	7C6C	FDC2	00D7	822D
PIC16LF18313	3068	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	7C6C	FDC2	00D7	822D
PIC16F18323	3067	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	7C6C	FDC2	00D7	822D
PIC16LF18323	3069	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	7C6C	FDC2	00D7	822D

Note 1: The protected checksum values listed assume that the unprotected checksum value has been stored in the User ID memory locations and used in the final calculations (see **Section 3.4.3.2 "Program Code Protection Enabled"** for details).

TABLE B-2: PROGRAMMING PIN LOCATIONS BY PACKAGE TYPE

Device	Package	Package Code	Package Drawing Number[(1)]	V_{DD}	V_{SS}	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
				PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC16(L)F18313	8-pin PDIP	(P)	C04-018	1	8	4	RA3	6	RA1	7	RA0
	8-pin SOIC (3.9 mm)	(SN)	C04-057	1	8	4	RA3	6	RA1	7	RA0
	8-pin UDFN (3x3)	(RF)	C04-254	1	8	4	RA3	6	RA1	7	RA0
PIC16(L)F18323	14-pin PDIP	(P)	C04-005	1	14	4	RA3	12	RA1	13	RA0
	14-pin SOIC (3.9 mm)	(SL)	C04-065	1	14	4	RA3	12	RA1	13	RA0
	14-pin TSSOP	(ST)	C04-087	1	14	4	RA3	12	RA1	13	RA0
	16-pin UQFN (4x4)	(JQ)	C04-257	16	13	3	RA3	11	RA1	12	RA0

Note 1: The most current package drawings can be found in the Microchip Packaging Specification, DS00049, found at http://www.microchip.com/packaging. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

REGISTER B-1: ADDRESS 8007h: CONFIGURATION WORD 1

R/P-1	U-1	R/P-1	U-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1
FCMEN	—	CSWEN	—	—	$\overline{\text{CLKOUTEN}}$	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **FCMEN**: Fail-Safe Clock Monitor Enable bit
1 = ON FSCM timer enabled
0 = OFF FSCM timer disabled

bit 12 **Unimplemented**: Read as '1'

bit 11 **CSWEN**: Clock Switch Enable bit
1 = ON Writing to NOSC and NDIV is allowed
0 = OFF The NOSC and NDIV bits cannot be changed by user software

bit 10-9 **Unimplemented**: Read as '1'

bit 8 **$\overline{\text{CLKOUTEN}}$**: Clock Out Enable bit
If FEXTOSC = EC (high, mid or low) or Not Enabled:
  1 = OFF CLKOUT function is disabled; I/O or oscillator function on OSC2
  0 = ON CLKOUT function is enabled; FOSC/4 clock appears at OSC2
Otherwise:
  This bit is ignored.

bit 7 **Unimplemented**: Read as '1'

bit 6-4 **RSTOSC<2:0>**: Power-Up Default Value for COSC bits
This value is the Reset default value for COSC, and selects the oscillator first used by user software
111 = EXT1X EXTOSC operating per FEXTOSC bits
110 = HFINT1 HFINTOSC (1 MHz)
101 = Reserved
100 = LFINT LFINTOSC
011 = SOSC SOSC (32.768 kHz)
010 = Reserved
001 = EXT4X EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
000 = HFINT32 HFINTOSC with 2x PLL (32 MHz)

bit 3 **Unimplemented**: Read as '1'

bit 2-0 **FEXTOSC<2:0>**:FEXTOSC External Oscillator Mode Selection bits
111 = ECH EC (External Clock) above 8 MHz
110 = ECM EC (External Clock) for 100 kHz to 8 MHz
101 = ECL EC (External Clock) below 100 kHz
100 = OFF Oscillator not enabled
011 = Unimplemented
010 = HS HS (Crystal oscillator) above 8 MHz
001 = XT HT (Crystal oscillator) above 100 kHz, below 8 MHz
000 = LP LP (Crystal oscillator) optimized for 32.768 kHz

REGISTER B-2: ADDRESS 8008h: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{DEBUG}}$(2)	STVREN	PPS1WAY	—	BORV(1)	—	BOREN1	BOREN0	$\overline{\text{LPBOREN}}$(3)	—	WDTE1	WDTE0	$\overline{\text{PWRTE}}$	MCLRE
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **$\overline{\text{DEBUG}}$**: Debugger Enable bit(2)
1 = OFF Background debugger disabled; ICSPCLK and ICSPDAT are general purpose I/O pins
0 = ON Background debugger enabled; ICSPCLK and ICSPDAT are dedicated to the debugger

bit 12 **STVREN**: Stack Overflow/Underflow Reset Enable bit
1 = ON Stack Overflow or Underflow will cause a Reset
0 = OFF Stack Overflow or Underflow will not cause a Reset

bit 11 **PPS1WAY**: PPSLOCK One-Way Set Enable bit
1 = ON The PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
0 = OFF The PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

bit 10 **Unimplemented**: Read as '1'

bit 9 **BORV**: Brown-out Reset Voltage Selection bit(1)
1 = LOW Brown-out Reset voltage (V_{BOR}) set to 1.9V on LF, and 2.45V on F devices
0 = HIGH Brown-out Reset voltage (V_{BOR}) set to 2.7V
The higher voltage setting is recommended for operation at or above 16 MHz.

bit 8 **Unimplemented**: Read as '1'

bit 7-6 **BOREN<1:0>**: Brown-out Reset Enable bits
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit
11 = ON Brown-out Reset is enabled; SBOREN bit is ignored
10 = SLEEP Brown-out Reset is enabled while running, disabled in Sleep; SBOREN bit is ignored
01 = SBOREN Brown-out Reset is enabled according to SBOREN
00 = OFF Brown-out Reset is disabled

bit 5 **$\overline{\text{LPBOREN}}$**: Low-Power BOR Enable bit(3)

PIC16LF18313/18323

1 = OFF ULPBOR is disabled
0 = ON ULPBOR is enabled

PIC16F18313/18323

Reserved - bit must be set to '1'.

bit 4 **Unimplemented**: Read as '1'

bit 3-2 **WDTE<1:0>**: Watchdog Timer Enable bit
11 = ON WDT is enabled; SWDTEN is ignored
10 = SLEEP WDT is enabled while running and disabled in Sleep/Idle; SWDTEN is ignored
01 = SWDTEN WDT is controlled by the SWDTEN bit in the WDTCON register
00 = OFF WDT is disabled; SWDTEN is ignored

bit 1 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = OFF PWRT is disabled
0 = ON PWRT is enabled

bit 0 **MCLRE**: Master Clear ($\overline{\text{MCLR}}$) Enable bit
If LVP = 1:
RA3 pin function is $\overline{\text{MCLR}}$.
If LVP = 0:
1 = ON $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0 = OFF $\overline{\text{MCLR}}$ pin function is port-defined function

Note 1: See V_{BOR} parameter for specific trip point voltages.
2: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.
3: Low-Power BOR is only available on the PIC16LF18313/18323 devices.

REGISTER B-3: ADDRESS 8009h: CONFIGURATION WORD 3

R/P-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
LVP(1)	—	—	—	—	—	—	—	—	—	—	—	WRT1	WRT0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **LVP**: Low-Voltage Programming Enable bit(1)
- `1` = `ON` Low-Voltage Programming is enabled. $\overline{MCLR}$/VPP pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
- `0` = `OFF` HV on $\overline{MCLR}$/VPP must be used for programming.

bit 12-2 **Unimplemented**: Read as '`1`'

bit 1-0 **WRT<1:0>**: User NVM Self-Write Protection bits
- `11` = `OFF` Write protection off
- `10` = `BOOT` 0000h to 01FFh write-protected, 0200h to 07FFh may be modified
- `01` = `HALF` 0000h to 03FFh write-protected, 0400h to 07FFh may be modified
- `00` = `ALL` 0000h to 07FFh write-protected, no addresses may be modified

WRT applies only to the self-write feature of the device; writing through ICSP™ is never protected.

Note 1: The LVP bit cannot be programmed to '`0`' when Programming mode is entered via LVP.

REGISTER B-4: ADDRESS 800Ah: CONFIGURATION WORD 4

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	—	—	—	—	$\overline{CPD}$	$\overline{CP}$
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	

bit 13-2 **Unimplemented:** Read as '`1`'

bit 1 **$\overline{CPD}$:** Data EEPROM Memory Code Protection bit
- `1 = OFF` - Data EEPROM code protection disabled
- `0 = ON` - Data EEPROM code protection enabled

bit 0 **$\overline{CP}$:** Program Memory Code Protection bit
- `1 = OFF` - Program Memory code protection disabled
- `0 = ON` - Program Memory code protection enabled

APPENDIX C: PIC16(L)F18324 AND PIC16(L)F18344 DEVICE ID, CHECKSUMS AND PINOUT DESCRIPTIONS

TABLE C-1: DEVICE IDs AND CHECKSUMS

Device	Device ID	Config 1		Config 2		Config 3		Config 4			Checksum			
											Unprotected		Code-Protected(1)	
		Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Unprotected Word (HEX)	Protected Word (HEX)	Mask (HEX)	Blank (HEX)	00AAh First and Last (HEX)	Blank (HEX)	00AAh First and Last (HEX)
PIC16F18324	303A	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	746C	F5C2	F8D7	7A2D
PIC16LF18324	303C	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	746C	F5C2	F8D7	7A2D
PIC16F18344	303B	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	746C	F5C2	F8D7	7A2D
PIC16LF18344	303D	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	746C	F5C2	F8D7	7A2D

Note 1: The protected checksum values listed assume that the unprotected checksum value has been stored in the User ID memory locations and used in the final calculations (see **Section 3.4.3.2 "Program Code Protection Enabled"** for details).

TABLE C-2: PROGRAMMING PIN LOCATIONS BY PACKAGE TYPE

Device	Package Type	Package Code	Package Drawing Number(1)	VDD	VSS	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
				PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC16(L)F18324	14-pin PDIP	(P)	C04-005	1	14	4	RA3	12	RA1	13	RA0
	14-pin SOIC	(SL)	C04-065	1	14	4	RA3	12	RA1	13	RA0
	14-pin TSSOP	(ST)	C04-087	1	14	4	RA3	12	RA1	13	RA0
	16-pin UQFN (4x4)	(JQ)	C04-257	16	13	3	RA3	11	RA1	12	RA0
PIC16(L)F18344	20-pin PDIP	(P)	C04-019	1	20	4	RA3	18	RA1	19	RA0
	20-pin SOIC	(SO)	C04-094	1	20	4	RA3	18	RA1	19	RA0
	20-pin SSOP	(SS)	C04-072	1	20	4	RA3	18	RA1	19	RA0
	20-pin UQFN (4x4)	(GZ)	C04-255	18	17	1	RA3	15	RA1	16	RA0

Note 1: The most current package drawings can be found in the Microchip Packaging Specification, DS00049, found at http://www.microchip.com/packaging. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

REGISTER C-1: ADDRESS 8007h: CONFIGURATION WORD 1

R/P-1	U-1	R/P-1	U-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1
FCMEN	—	CSWEN	—	—	$\overline{\text{CLKOUTEN}}$	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **FCMEN**: Fail-Safe Clock Monitor Enable bit
1 = ON FSCM timer enabled
0 = OFF FSCM timer disabled

bit 12 **Unimplemented**: Read as '1'

bit 11 **CSWEN**: Clock Switch Enable bit
1 = ON Writing to NOSC and NDIV is allowed
0 = OFF The NOSC and NDIV bits cannot be changed by user software

bit 10-9 **Unimplemented**: Read as '1'

bit 8 **$\overline{\text{CLKOUTEN}}$**: Clock Out Enable bit
If FEXTOSC = EC (high, mid or low) or Not Enabled:
1 = OFF CLKOUT function is disabled; I/O or oscillator function on OSC2
0 = ON CLKOUT function is enabled; FOSC/4 clock appears at OSC2
Otherwise:
This bit is ignored.

bit 7 **Unimplemented**: Read as '1'

bit 6-4 **RSTOSC<2:0>**: Power-Up Default Value for COSC bits
This value is the Reset default value for COSC, and selects the oscillator first used by user software
111 = EXT1X EXTOSC operating per FEXTOSC bits
110 = HFINT1 HFINTOSC (1 MHz)
101 = Reserved
100 = LFINT LFINTOSC
011 = SOSC SOSC (32.768 kHz)
010 = Reserved
001 = EXT4X EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
000 = HFINT32 HFINTOSC with 2x PLL (32 MHz)

bit 3 **Unimplemented**: Read as '1'

bit 2-0 **FEXTOSC<2:0>**:FEXTOSC External Oscillator Mode Selection bits
111 = ECH EC (External Clock) above 8 MHz
110 = ECM EC (External Clock) for 100 kHz to 8 MHz
101 = ECL EC (External Clock) below 100 kHz
100 = OFF Oscillator not enabled
011 = Unimplemented
010 = HS HS (Crystal oscillator) above 8 MHz
001 = XT HT (Crystal oscillator) above 100 kHz, below 8 MHz
000 = LP LP (Crystal oscillator) optimized for 32.768 kHz

REGISTER C-2: ADDRESS 8008h: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{DEBUG}}$(2)	STVREN	PPS1WAY	—	BORV(1)	—	BOREN1	BOREN0	$\overline{\text{LPBOREN}}$(3)	—	WDTE1	WDTE0	$\overline{\text{PWRTE}}$	MCLRE
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **$\overline{\text{DEBUG}}$**: Debugger Enable bit(2)
1 = OFF Background debugger disabled; ICSPCLK and ICSPDAT are general purpose I/O pins
0 = ON Background debugger enabled; ICSPCLK and ICSPDAT are dedicated to the debugger

bit 12 **STVREN**: Stack Overflow/Underflow Reset Enable bit
1 = ON Stack Overflow or Underflow will cause a Reset
0 = OFF Stack Overflow or Underflow will not cause a Reset

bit 11 **PPS1WAY**: PPSLOCK One-Way Set Enable bit
1 = ON The PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
0 = OFF The PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

bit 10 **Unimplemented**: Read as ‘1’

bit 9 **BORV**: Brown-out Reset Voltage Selection bit(1)
1 = LOW Brown-out Reset voltage (V_{BOR}) set to 1.9V on LF, and 2.45V on F devices
0 = HIGH Brown-out Reset voltage (V_{BOR}) set to 2.7V
The higher voltage setting is recommended for operation at or above 16 MHz.

bit 8 **Unimplemented**: Read as ‘1’

bit 7-6 **BOREN<1:0>**: Brown-out Reset Enable bits
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit
11 = ON Brown-out Reset is enabled; SBOREN bit is ignored
10 = SLEEP Brown-out Reset is enabled while running, disabled in Sleep; SBOREN bit is ignored
01 = SBOREN Brown-out Reset is enabled according to SBOREN
00 = OFF Brown-out Reset is disabled

bit 5 **$\overline{\text{LPBOREN}}$**: Low-Power BOR Enable bit(3)

PIC16LF18324/344

1 = OFF ULPBOR is disabled
0 = ON ULPBOR is enabled

PIC16F18324/344

Reserved - bit must be set to ‘1’.

bit 4 **Unimplemented**: Read as ‘1’

bit 3-2 **WDTE<1:0>**: Watchdog Timer Enable bit
11 = ON WDT is enabled; SWDTEN is ignored
10 = SLEEP WDT is enabled while running and disabled in Sleep/Idle; SWDTEN is ignored
01 = SWDTEN WDT is controlled by the SWDTEN bit in the WDTCON register
00 = OFF WDT is disabled; SWDTEN is ignored

bit 1 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = OFF PWRT is disabled
0 = ON PWRT is enabled

bit 0 **MCLRE**: Master Clear ($\overline{\text{MCLR}}$) Enable bit
If LVP = 1:
RA3 pin function is $\overline{\text{MCLR}}$.
If LVP = 0:
1 = ON $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0 = OFF $\overline{\text{MCLR}}$ pin function is port-defined function

Note 1: See V_{BOR} parameter for specific trip point voltages.
2: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a ‘1’.
3: Low-power BOR is only available on the PIC16LF18324/18344 devices.

REGISTER C-3: ADDRESS 8009h: CONFIGURATION WORD 3

R/P-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
LVP[1]	—	—	—	—	—	—	—	—	—	—	—	WRT1	WRT0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **LVP**: Low-Voltage Programming Enable bit[1]
- `1` = `ON` Low-Voltage Programming is enabled. $\overline{MCLR}/V_{PP}$ pin function is $\overline{MCLR}$. MCLRE Configuration bit is ignored.
- `0` = `OFF` HV on $\overline{MCLR}/V_{PP}$ must be used for programming.

bit 12-2 **Unimplemented**: Read as '`1`'

bit 1-0 **WRT<1:0>**:User NVM Self-Write Protection bits
- `11` = `OFF` Write protection off
- `10` = `BOOT` 0000h to 01FFh write-protected, 0200h to 0FFFh may be modified
- `01` = `HALF` 0000h to 07FFh write-protected, 0800h to 0FFFh may be modified
- `00` = `ALL` 0000h to 0FFFh write-protected, no addresses may be modified

WRT applies only to the self-write feature of the device; writing through ICSP™ is never protected.

Note 1: The LVP bit cannot be programmed to '`0`' when Programming mode is entered via LVP.

REGISTER C-4: ADDRESS 800Ah: CONFIGURATION WORD 4

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	—	—	—	—	$\overline{CPD}$	$\overline{CP}$
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	

bit 13-2 **Unimplemented:** Read as '`1`'

bit 1 **$\overline{CPD}$:** EEPROM Memory Code Protection bit
- `1 = OFF` - EEPROM code protection disabled
- `0 = ON` - EEPROM code protection enabled

bit 0 **$\overline{CP}$:** Program Memory Code Protection bit
- `1 = OFF` - Program Memory code protection disabled
- `0 = ON` - Program Memory code protection enabled

APPENDIX D: PIC16(L)F18325 AND PIC16(L)F18345 DEVICE ID, CHECKSUMS AND PINOUT DESCRIPTIONS

TABLE D-1: DEVICE IDs AND CHECKSUMS

Device	Device ID	Config 1		Config 2		Config 3		Config 4			Checksum			
											Unprotected		Code-Protected(1)	
		Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Unprotected Word (HEX)	Protected Word (HEX)	Mask (HEX)	Blank (HEX)	00AAh First and Last (HEX)	Blank (HEX)	00AAh First and Last (HEX)
PIC16F18325	303E	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	646C	E5C2	E8D7	6A2D
PIC16LF18325	3040	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	646C	E5C2	E8D7	6A2D
PIC16F18345	303F	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	646C	E5C2	E8D7	6A2D
PIC16LF18345	3041	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	646C	E5C2	E8D7	6A2D

Note 1: The protected checksum values listed assume that the unprotected checksum value has been stored in the User ID memory locations and used in the final calculations (see **Section 3.4.3.2 "Program Code Protection Enabled"** for details).

TABLE D-2: PROGRAMMING PIN LOCATIONS BY PACKAGE TYPE

Device	Package Type	Package Code	Package Drawing Number(1)	VDD	VSS	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
				PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC16(L)F18325	14-pin PDIP	(P)	C04-005	1	14	4	RA3	12	RA1	13	RA0
	14-pin SOIC	(SL)	C04-065	1	14	4	RA3	12	RA1	13	RA0
	14-pin TSSOP	(ST)	C04-087	1	14	4	RA3	12	RA1	13	RA0
	16-pin UQFN (4x4)	(JQ)	C04-257	16	13	3	RA3	11	RA1	12	RA0
PIC16(L)F18345	20-pin PDIP	(P)	C04-019	1	20	4	RA3	18	RA1	19	RA0
	20-pin SOIC	(SO)	C04-094	1	20	4	RA3	18	RA1	19	RA0
	20-pin SSOP	(SS)	C04-072	1	20	4	RA3	18	RA1	19	RA0
	20-pin UQFN (4x4)	(GZ)	C04-255	18	17	1	RA3	15	RA1	16	RA0

Note 1: The most current package drawings can be found in the Microchip Packaging Specification, DS00049, found at http://www.microchip.com/packaging. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

REGISTER D-1: ADDRESS 8007h: CONFIGURATION WORD 1

R/P-1	U-1	R/P-1	U-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1
FCMEN	—	CSWEN	—	—	$\overline{\text{CLKOUTEN}}$	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **FCMEN**: Fail-Safe Clock Monitor Enable bit
1 = ON FSCM timer enabled
0 = OFF FSCM timer disabled

bit 12 **Unimplemented**: Read as ‘1’

bit 11 **CSWEN**: Clock Switch Enable bit
1 = ON Writing to NOSC and NDIV is allowed
0 = OFF The NOSC and NDIV bits cannot be changed by user software

bit 10-9 **Unimplemented**: Read as ‘1’

bit 8 $\overline{\textbf{CLKOUTEN}}$: Clock Out Enable bit
If FEXTOSC = EC (high, mid or low) or Not Enabled:
1 = OFF CLKOUT function is disabled; I/O or oscillator function on OSC2
0 = ON CLKOUT function is enabled; FOSC/4 clock appears at OSC2
Otherwise:
This bit is ignored.

bit 7 **Unimplemented**: Read as ‘1’

bit 6-4 **RSTOSC<2:0>**: Power-Up Default Value for COSC bits
This value is the Reset default value for COSC, and selects the oscillator first used by user software
111 = EXT1X EXTOSC operating per FEXTOSC bits
110 = HFINT1 HFINTOSC (1 MHz)
101 = Reserved
100 = LFINT LFINTOSC
011 = SOSC SOSC (32.768 kHz)
010 = Reserved
001 = EXT4X EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
000 = HFINT32 HFINTOSC with 2x PLL (32 MHz)

bit 3 **Unimplemented**: Read as ‘1’

bit 2-0 **FEXTOSC<2:0>**:FEXTOSC External Oscillator Mode Selection bits
111 = ECH EC (External Clock) above 8 MHz
110 = ECM EC (External Clock) for 100 kHz to 8 MHz
101 = ECL EC (External Clock) below 100 kHz
100 = OFF Oscillator not enabled
011 = Unimplemented
010 = HS HS (Crystal oscillator) above 8 MHz
001 = XT HT (Crystal oscillator) above 100 kHz, below 8 MHz
000 = LP LP (Crystal oscillator) optimized for 32.768 kHz

REGISTER D-2: ADDRESS 8008h: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{DEBUG}}$(2)	STVREN	PPS1WAY	—	BORV(1)	—	BOREN1	BOREN0	$\overline{\text{LPBOREN}}$(3)	—	WDTE1	WDTE0	$\overline{\text{PWRTE}}$	MCLRE
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **$\overline{\text{DEBUG}}$**: Debugger Enable bit(2)
1 = OFF Background debugger disabled
0 = ON Background debugger enabled

bit 12 **STVREN**: Stack Overflow/Underflow Reset Enable bit
1 = ON Stack Overflow or Underflow will cause a Reset
0 = OFF Stack Overflow or Underflow will not cause a Reset

bit 11 **PPS1WAY**: PPSLOCK One-Way Set Enable bit
1 = ON The PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
0 = OFF The PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

bit 10 **Unimplemented**: Read as '1'

bit 9 **BORV**: Brown-out Reset Voltage Selection bit(1)
1 = LOW Brown-out Reset voltage (V_{BOR}) set to 1.9V on LF, and 2.45V on F devices
0 = HIGH Brown-out Reset voltage (V_{BOR}) set to 2.7V
The higher voltage setting is recommended for operation at or above 16 MHz.

bit 8 **Unimplemented**: Read as '1'

bit 7-6 **BOREN<1:0>**: Brown-out Reset Enable bits
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit
11 = ON Brown-out Reset is enabled; SBOREN bit is ignored
10 = SLEEP Brown-out Reset is enabled while running, disabled in Sleep; SBOREN bit is ignored
01 = SBOREN Brown-out Reset is enabled according to SBOREN
00 = OFF Brown-out Reset is disabled

bit 5 **$\overline{\text{LPBOREN}}$**: Low-Power BOR Enable bit (3)

PIC16LF18325/18345

1 = OFF ULPBOR is disabled
0 = ON ULPBOR is enabled

PIC16F18325/345

Reserved - bit must be set to '1'.

bit 4 **Unimplemented**: Read as '1'

bit 3-2 **WDTE<1:0>**: Watchdog Timer Enable bit
11 = ON WDT is enabled; SWDTEN is ignored
10 = SLEEP WDT is enabled while running and disabled in Sleep/Idle; SWDTEN is ignored
01 = SWDTEN WDT is controlled by the SWDTEN bit in the WDTCON register
00 = OFF WDT is disabled; SWDTEN is ignored

bit 1 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = OFF PWRT is disabled
0 = ON PWRT is enabled

bit 0 **MCLRE**: Master Clear ($\overline{\text{MCLR}}$) Enable bit
If LVP = 1:
RA3 pin function is $\overline{\text{MCLR}}$.
If LVP = 0:
1 = ON $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0 = OFF $\overline{\text{MCLR}}$ pin function is port-defined function

Note 1: See V_{BOR} parameter for specific trip point voltages.
2: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers.For normal device operation, this bit should be maintained as a '1'.
3: Low-Power BOR is only available on the PIC16LF18325/18345 devices.

REGISTER D-3: ADDRESS 8009h: CONFIGURATION WORD 3

R/P-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
LVP(1)	—	—	—	—	—	—	—	—	—	—	—	WRT1	WRT0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **LVP**: Low-Voltage Programming Enable bit(1)
1 = ON Low-Voltage Programming is enabled. $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$. MCLRE Configuration bit is ignored.
0 = OFF HV on $\overline{\text{MCLR}}$/VPP must be used for programming.

bit 12-2 **Unimplemented**: Read as '1'

bit 1-0 **WRT<1:0>**:User NVM Self-Write Protection bits
11 = OFF Write protection off
10 = BOOT 0000h to 01FFh write-protected, 0200h to 1FFFh may be modified
01 = HALF 0000h to 0FFFh write-protected, 1000h to 1FFFh may be modified
00 = ALL 0000h to 1FFFh write-protected, no addresses may be modified
WRT applies only to the self-write feature of the device; writing through ICSP™ is never protected.

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

REGISTER D-4: ADDRESS 800Ah: CONFIGURATION WORD 4

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	—	—	—	—	$\overline{\text{CPD}}$	$\overline{\text{CP}}$
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	

bit 13-2 **Unimplemented:** Read as '1'

bit 1 **$\overline{\text{CPD}}$:** EEPROM Memory Code Protection bit
1 = OFF - EEPROM code protection disabled
0 = ON - EEPROM code protection enabled

bit 0 **$\overline{\text{CP}}$:** Program Memory Code Protection bit
1 = OFF - Program Memory code protection disabled
0 = ON - Program Memory code protection enabled

APPENDIX E: PIC16(L)F18326 AND PIC16(L)F18346 DEVICE ID, CHECKSUMS AND PINOUT DESCRIPTIONS

TABLE E-1: DEVICE IDs AND CHECKSUMS

Device	Device ID	Config 1		Config 2		Config 3		Config 4			Checksum			
											Unprotected		Code-Protected[1]	
		Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Word (HEX)	Mask (HEX)	Unprotected Word (HEX)	Protected Word (HEX)	Mask (HEX)	Blank (HEX)	00AAh First and Last (HEX)	Blank (HEX)	00AAh First and Last (HEX)
PIC16F18326	30A4	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	446C	C5C2	C8D7	4A2D
PIC16LF18326	30A6	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	446C	C5C2	C8D7	4A2D
PIC16F18346	30A5	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	446C	C5C2	C8D7	4A2D
PIC16LF18346	30A7	3FFF	2977	3FFF	3AEF	3FFF	2003	3FFF	3FFE	0003	446C	C5C2	C8D7	4A2D

Note 1: The protected checksum values listed assume that the unprotected checksum value has been stored in the User ID memory locations and used in the final calculations (see **Section 3.4.3.2 "Program Code Protection Enabled"** for details).

TABLE E-2: PROGRAMMING PIN LOCATIONS BY PACKAGE TYPE

Device	Package Type	Package Code	Package Drawing Number[1]	VDD	Vss	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
				PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC16(L)F18326	14-pin PDIP	(P)	C04-005	1	14	4	RA3	12	RA1	13	RA0
	14-pin SOIC	(SL)	C04-065	1	14	4	RA3	12	RA1	13	RA0
	14-pin TSSOP	(ST)	C04-087	1	14	4	RA3	12	RA1	13	RA0
	16-pin UQFN (4x4)	(JQ)	C04-257	16	13	3	RA3	11	RA1	12	RA0
PIC16(L)F18346	20-pin PDIP	(P)	C04-019	1	20	4	RA3	18	RA1	19	RA0
	20-pin SOIC	(SO)	C04-094	1	20	4	RA3	18	RA1	19	RA0
	20-pin SSOP	(SS)	C04-072	1	20	4	RA3	18	RA1	19	RA0
	20-pin UQFN (4x4)	(GZ)	C04-255	18	17	1	RA3	15	RA1	16	RA0

Note 1: The most current package drawings can be found in the Microchip Packaging Specification, DS00049, found at http://www.microchip.com/packaging. The drawing numbers listed above do not include the current revision designator which is added at the end of the number.

REGISTER E-1: ADDRESS 8007h: CONFIGURATION WORD 1

R/P-1	U-1	R/P-1	U-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1
FCMEN	—	CSWEN	—	—	$\overline{\text{CLKOUTEN}}$	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **FCMEN**: Fail-Safe Clock Monitor Enable bit
1 = ON FSCM timer enabled
0 = OFF FSCM timer disabled

bit 12 **Unimplemented**: Read as ‘1’

bit 11 **CSWEN**: Clock Switch Enable bit
1 = ON Writing to NOSC and NDIV is allowed
0 = OFF The NOSC and NDIV bits cannot be changed by user software

bit 10-9 **Unimplemented**: Read as ‘1’

bit 8 **$\overline{\text{CLKOUTEN}}$**: Clock Out Enable bit
If FEXTOSC = EC (high, mid or low) or Not Enabled:
1 = OFF CLKOUT function is disabled; I/O or oscillator function on OSC2
0 = ON CLKOUT function is enabled; FOSC/4 clock appears at OSC2
Otherwise:
This bit is ignored.

bit 7 **Unimplemented**: Read as ‘1’

bit 6-4 **RSTOSC<2:0>**: Power-Up Default Value for COSC bits
This value is the Reset default value for COSC, and selects the oscillator first used by user software
111 = EXT1X EXTOSC operating per FEXTOSC bits
110 = HFINT1 HFINTOSC (1 MHz)
101 = Reserved
100 = LFINT LFINTOSC
011 = SOSC SOSC (32.768 kHz)
010 = Reserved
001 = EXT4X EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
000 = HFINT32 HFINTOSC with 2x PLL (32 MHz)

bit 3 **Unimplemented**: Read as ‘1’

bit 2-0 **FEXTOSC<2:0>**:FEXTOSC External Oscillator Mode Selection bits
111 = ECH EC (External Clock) above 8 MHz
110 = ECM EC (External Clock) for 100 kHz to 8 MHz
101 = ECL EC (External Clock) below 100 kHz
100 = OFF Oscillator not enabled
011 = Unimplemented
010 = HS HS (Crystal oscillator) above 8 MHz
001 = XT HT (Crystal oscillator) above 100 kHz, below 8 MHz
000 = LP LP (Crystal oscillator) optimized for 32.768 kHz

REGISTER E-2: ADDRESS 8008h: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	U-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{DEBUG}}$(2)	STVREN	PPS1WAY	—	BORV(1)	—	BOREN1	BOREN0	$\overline{\text{LPBOREN}}$(3)	—	WDTE1	WDTE0	$\overline{\text{PWRTE}}$	MCLRE
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **$\overline{\text{DEBUG}}$**: Debugger Enable bit(2)
1 = OFF Background debugger disabled
0 = ON Background debugger enabled

bit 12 **STVREN**: Stack Overflow/Underflow Reset Enable bit
1 = ON Stack Overflow or Underflow will cause a Reset
0 = OFF Stack Overflow or Underflow will not cause a Reset

bit 11 **PPS1WAY**: PPSLOCK One-Way Set Enable bit
1 = ON The PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
0 = OFF The PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

bit 10 **Unimplemented**: Read as ‘1’

bit 9 **BORV**: Brown-out Reset Voltage Selection bit(1)
1 = LOW Brown-out Reset voltage (VBOR) set to 1.9V on LF, and 2.45V on F devices
0 = HIGH Brown-out Reset voltage (VBOR) set to 2.7V
The higher voltage setting is recommended for operation at or above 16 MHz.

bit 8 **Unimplemented**: Read as ‘1’

bit 7-6 **BOREN<1:0>**: Brown-out Reset Enable bits
When enabled, Brown-out Reset Voltage (VBOR) is set by the BORV bit
11 = ON Brown-out Reset is enabled; SBOREN bit is ignored
10 = SLEEP Brown-out Reset is enabled while running, disabled in Sleep; SBOREN bit is ignored
01 = SBOREN Brown-out Reset is enabled according to SBOREN
00 = OFF Brown-out Reset is disabled

bit 5 **$\overline{\text{LPBOREN}}$**: Low-Power BOR Enable bit (3)

PIC16LF18326/18346

1 = OFF ULPBOR is disabled
0 = ON ULPBOR is enabled

PIC16F18326/346

Reserved - bit must be set to ‘1’.

bit 4 **Unimplemented**: Read as ‘1’

bit 3-2 **WDTE<1:0>**: Watchdog Timer Enable bit
11 = ON WDT is enabled; SWDTEN is ignored
10 = SLEEP WDT is enabled while running and disabled in Sleep/Idle; SWDTEN is ignored
01 = SWDTEN WDT is controlled by the SWDTEN bit in the WDTCON register
00 = OFF WDT is disabled; SWDTEN is ignored

bit 1 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = OFF PWRT is disabled
0 = ON PWRT is enabled

bit 0 **MCLRE**: Master Clear ($\overline{\text{MCLR}}$) Enable bit
If LVP = 1:
RA3 pin function is $\overline{\text{MCLR}}$.
If LVP = 0:
1 = ON $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0 = OFF MCLR pin function is port-defined function

Note 1: See VBOR parameter for specific trip point voltages.
2: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers.For normal device operation, this bit should be maintained as a ‘1’.
3: Low-Power BOR is only available on the PIC16LF18326/18346 devices.

REGISTER E-3: ADDRESS 8009h: CONFIGURATION WORD 3

R/P-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
LVP(1)	—	—	—	—	—	—	—	—	—	—	—	WRT1	WRT0
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	n = Value when blank or after Bulk Erase

bit 13 **LVP**: Low-Voltage Programming Enable bit(1)
- `1` = `ON` Low-Voltage Programming is enabled. $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$. MCLRE Configuration bit is ignored.
- `0` = `OFF` HV on $\overline{\text{MCLR}}$/VPP must be used for programming.

bit 12-2 **Unimplemented**: Read as '`1`'

bit 1-0 **WRT<1:0>**:User NVM Self-Write Protection bits
- `11` = `OFF` Write protection off
- `10` = `BOOT` 0000h to 01FFh write-protected, 0200h to 1FFFh may be modified
- `01` = `HALF` 0000h to 0FFFh write-protected, 1000h to 1FFFh may be modified
- `00` = `ALL` 0000h to 1FFFh write-protected, no addresses may be modified

WRT applies only to the self-write feature of the device; writing through ICSP™ is never protected.

Note 1: The LVP bit cannot be programmed to '`0`' when Programming mode is entered via LVP.

REGISTER E-4: ADDRESS 800Ah: CONFIGURATION WORD 4

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	—	—	—	—	$\overline{\text{CPD}}$	$\overline{\text{CP}}$
bit 13													bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	

bit 13-2 **Unimplemented:** Read as '`1`'

bit 1 **$\overline{\text{CPD}}$:** EEPROM Memory Code Protection bit
- `1 = OFF` - EEPROM code protection disabled
- `0 = ON` - EEPROM code protection enabled

bit 0 **$\overline{\text{CP}}$:** Program Memory Code Protection bit
- `1 = OFF` - Program Memory code protection disabled
- `0 = ON` - Program Memory code protection enabled

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

ISO/TS 16949

Trademarks

ISBN: 978-1-5224-0167-4

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15