



PIC12(L)F1612/16(L)F161X

PIC12(L)F1612/16(L)F161X Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC12F1612
- PIC12LF1612
- PIC16F1613
- PIC16LF1613
- PIC16F1614
- PIC16LF1614
- PIC16F1615
- PIC16LF1615
- PIC16F1618
- PIC16LF1618
- PIC16F1619
- PIC16LF1619

1.0 OVERVIEW

The devices can be programmed using either the high-voltage In-Circuit Serial Programming™ (ICSP™) method or the low-voltage ICSP™ method.

1.1 Hardware Requirements

1.1.1 HIGH-VOLTAGE ICSP PROGRAMMING

In High-Voltage ICSP™ mode, these devices require two programmable power supplies: one for VDD and one for the MCLR/VPP pin.

1.1.2 LOW-VOLTAGE ICSP PROGRAMMING

In Low-Voltage ICSP™ mode, these devices can be programmed using a single VDD source in the operating range. The MCLR/VPP pin does not have to be brought to a different voltage, but can instead be left at the normal operating voltage.

1.1.2.1 Single-Supply ICSP Programming

The LVP bit in Configuration Word 2 enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled) from the factory. The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the MCLR/VPP pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and only the High-Voltage ICSP mode can be used to program the device.

Note 1: The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the MCLR/VPP pin.

2: While in Low-Voltage ICSP mode, MCLR is always enabled, regardless of the MCLRE bit, and the port pin can no longer be used as a general purpose input.

PIC12(L)F1612/16(L)F161X

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in [Table 1-1](#).

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

| Pin Name | During Programming | | |
|-------------------------------------|---------------------|------------------|--|
| | Function | Pin Type | Pin Description |
| ICSPCLK | ICSPCLK | I | Clock Input – Schmitt Trigger Input |
| ICSPDAT | ICSPDAT | I/O | Data Input/Output – Schmitt Trigger Input |
| $\overline{\text{MCLR}}/\text{VPP}$ | Program/Verify mode | P ⁽¹⁾ | Program Mode Select/Programming Power Supply |
| VDD | VDD | P | Power Supply |
| VSS | VSS | P | Ground |

Legend: I = Input, O = Output, P = Power

Note 1: The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to $\overline{\text{MCLR}}$ input. Since the $\overline{\text{MCLR}}$ is used for a level source, $\overline{\text{MCLR}}$ does not draw any significant current.

PIC12(L)F1612/16(L)F161X

2.0 DEVICE PINOUTS

The pin diagrams are shown in [Figure 2-1](#) through [Figure 2-6](#). The pins that are required for programming are listed in [Table 1-1](#) and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 8-PIN PDIP, SOIC, DFN, UDFN

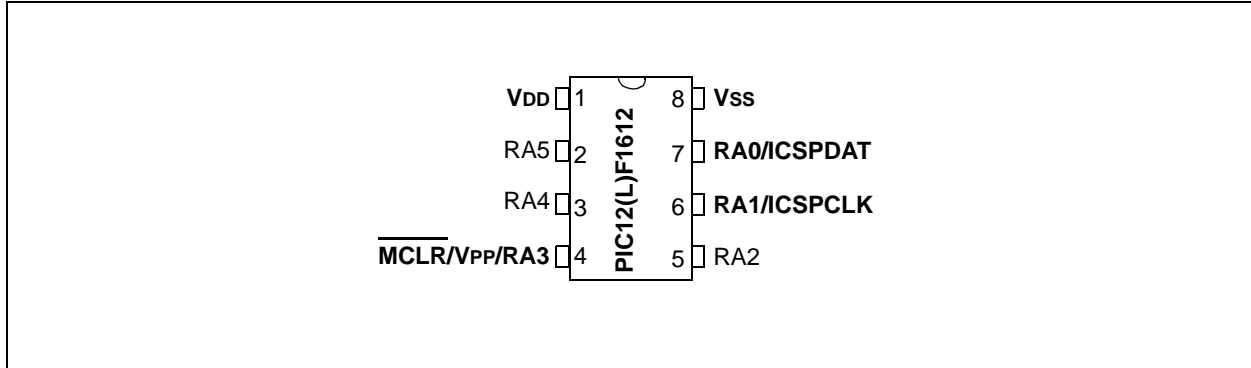


FIGURE 2-2: 14-PIN PDIP, SOIC, TSSOP

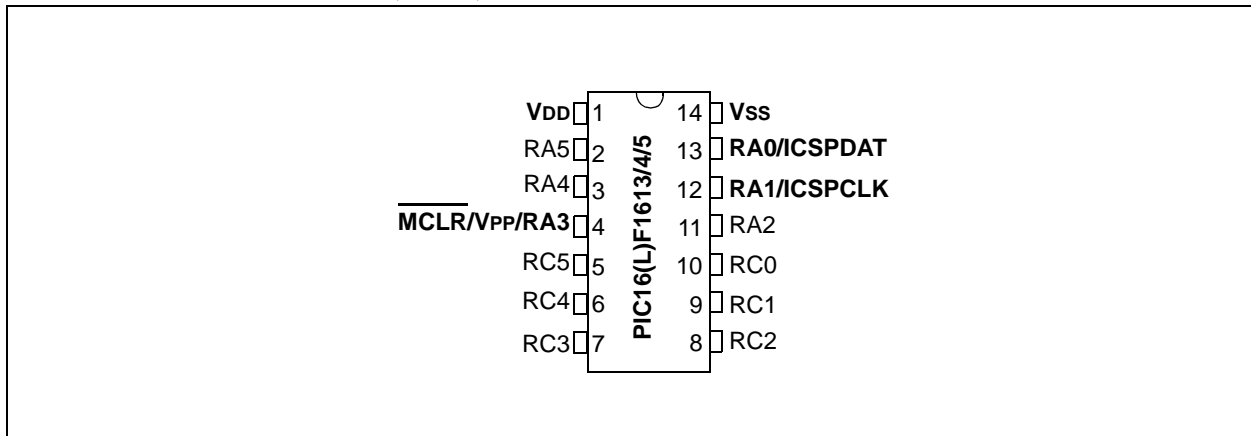
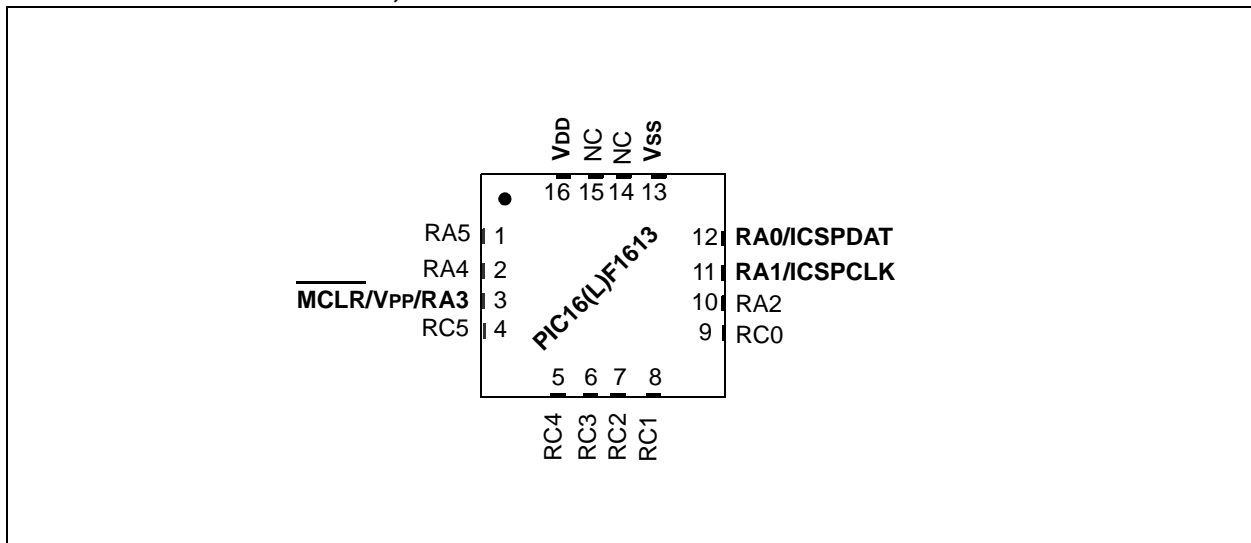


FIGURE 2-3: 16-PIN QFN, UQFN



PIC12(L)F1612/16(L)F161X

FIGURE 2-4: 16-PIN QFN

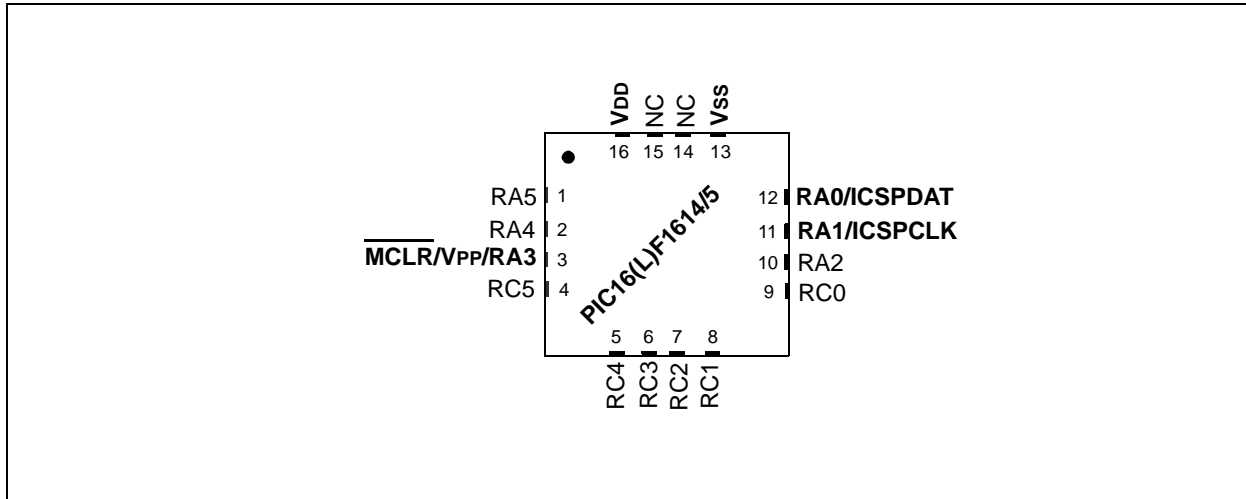
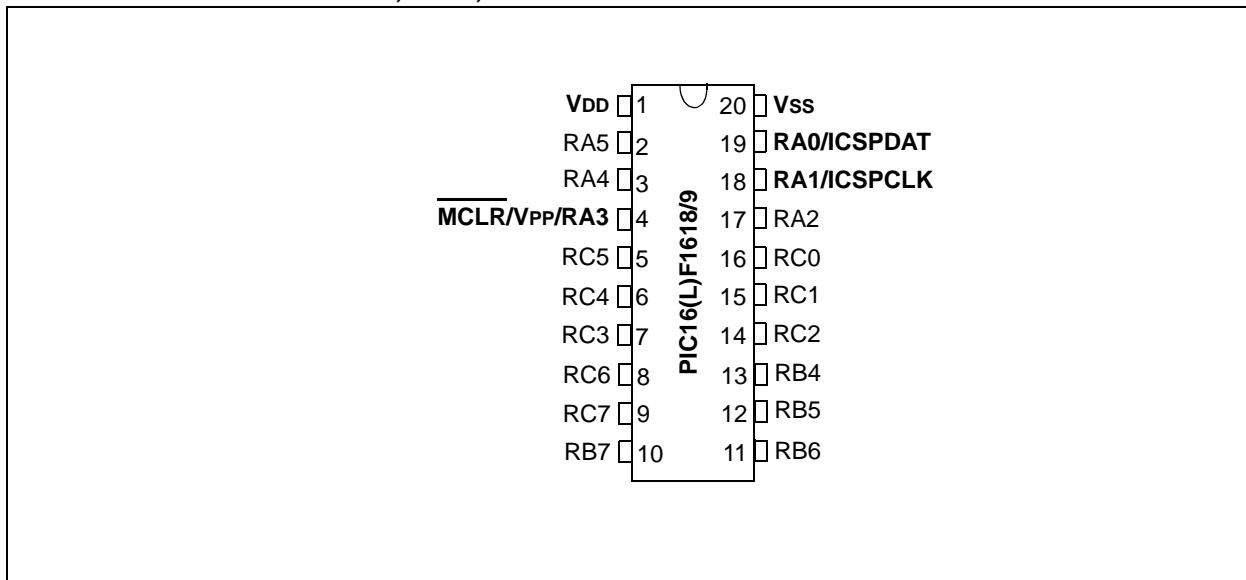
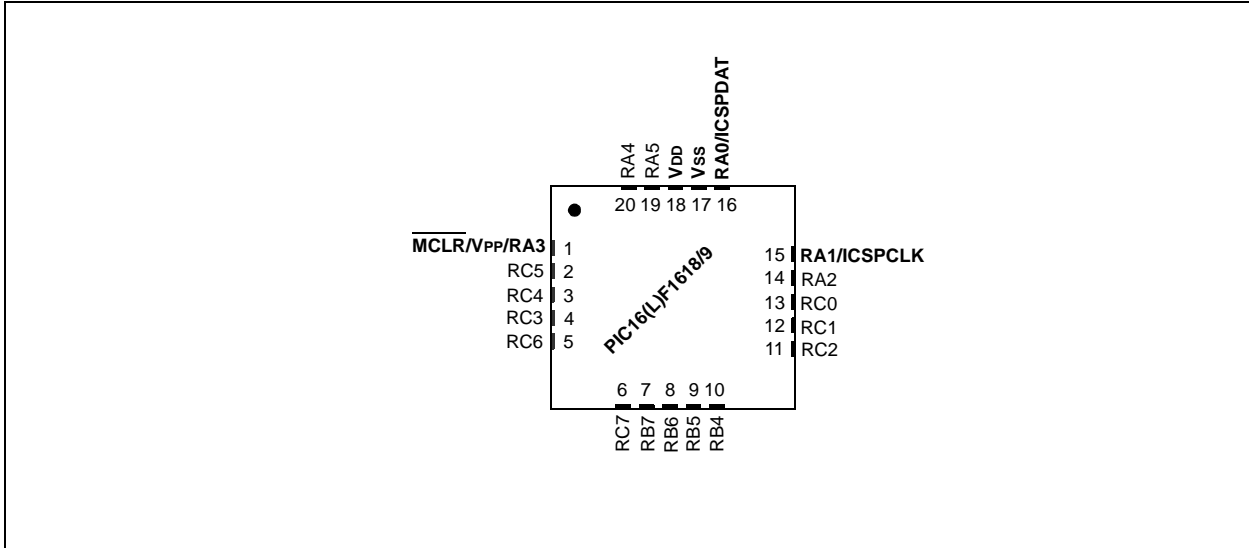


FIGURE 2-5: 20-PIN PDIP, SOIC, SSOP



PIC12(L)F1612/16(L)F161X

FIGURE 2-6: 20-PIN QFN

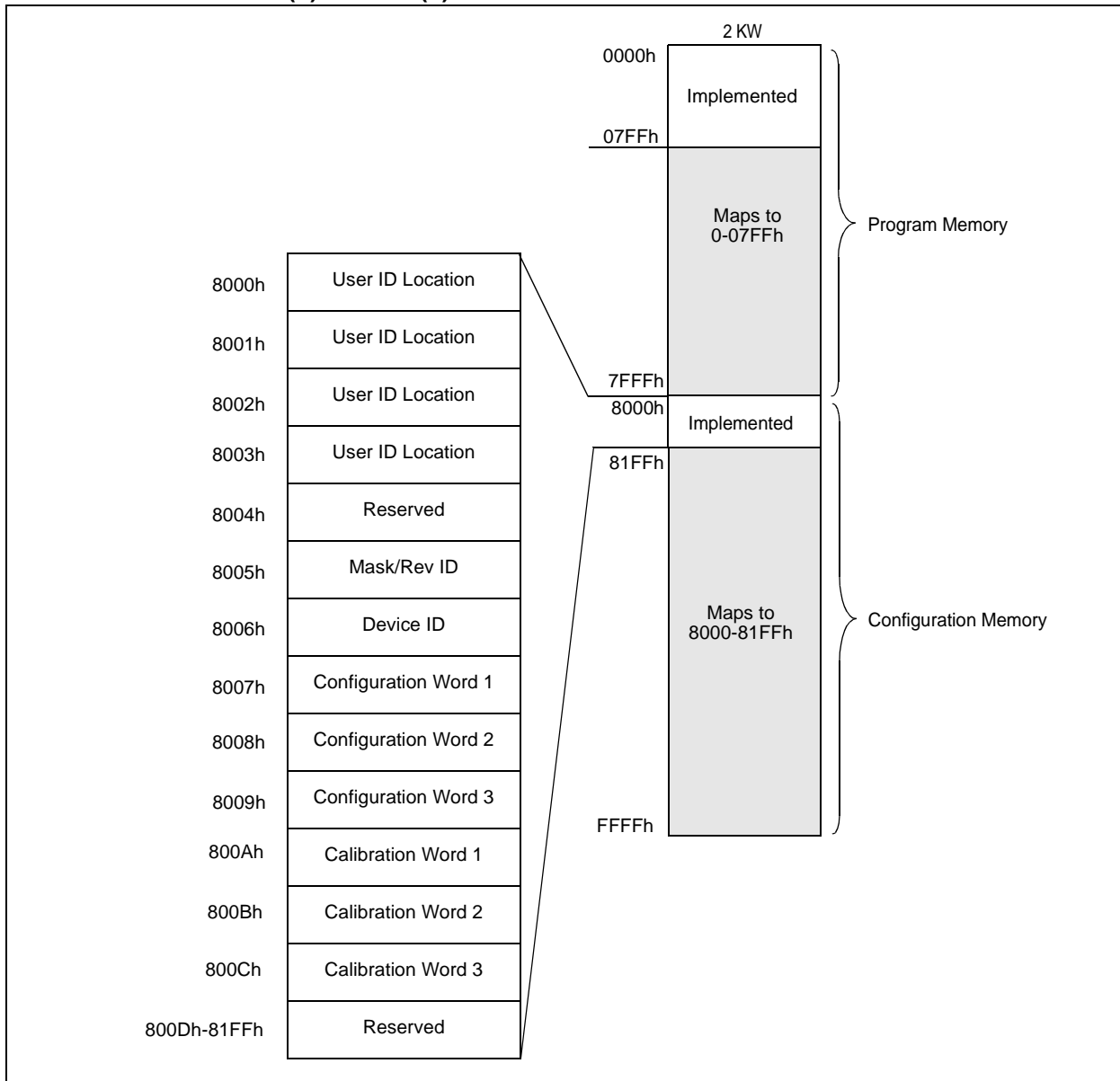


PIC12(L)F1612/16(L)F161X

3.0 MEMORY MAP

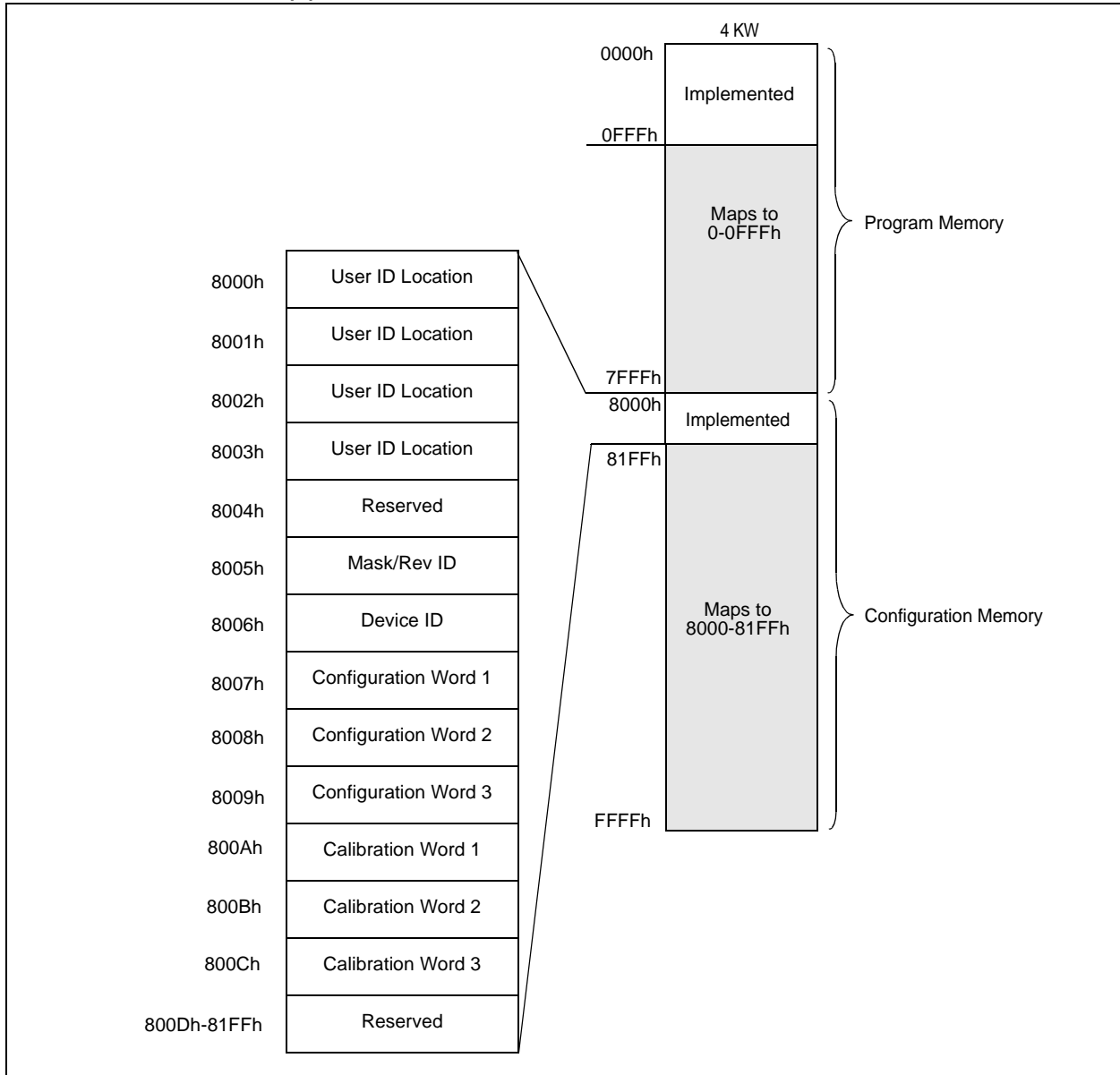
The memory is broken into two sections: program memory and configuration memory.

FIGURE 3-1: PIC12(L)F1612/16(L)F1613 PROGRAM MEMORY MAPPING



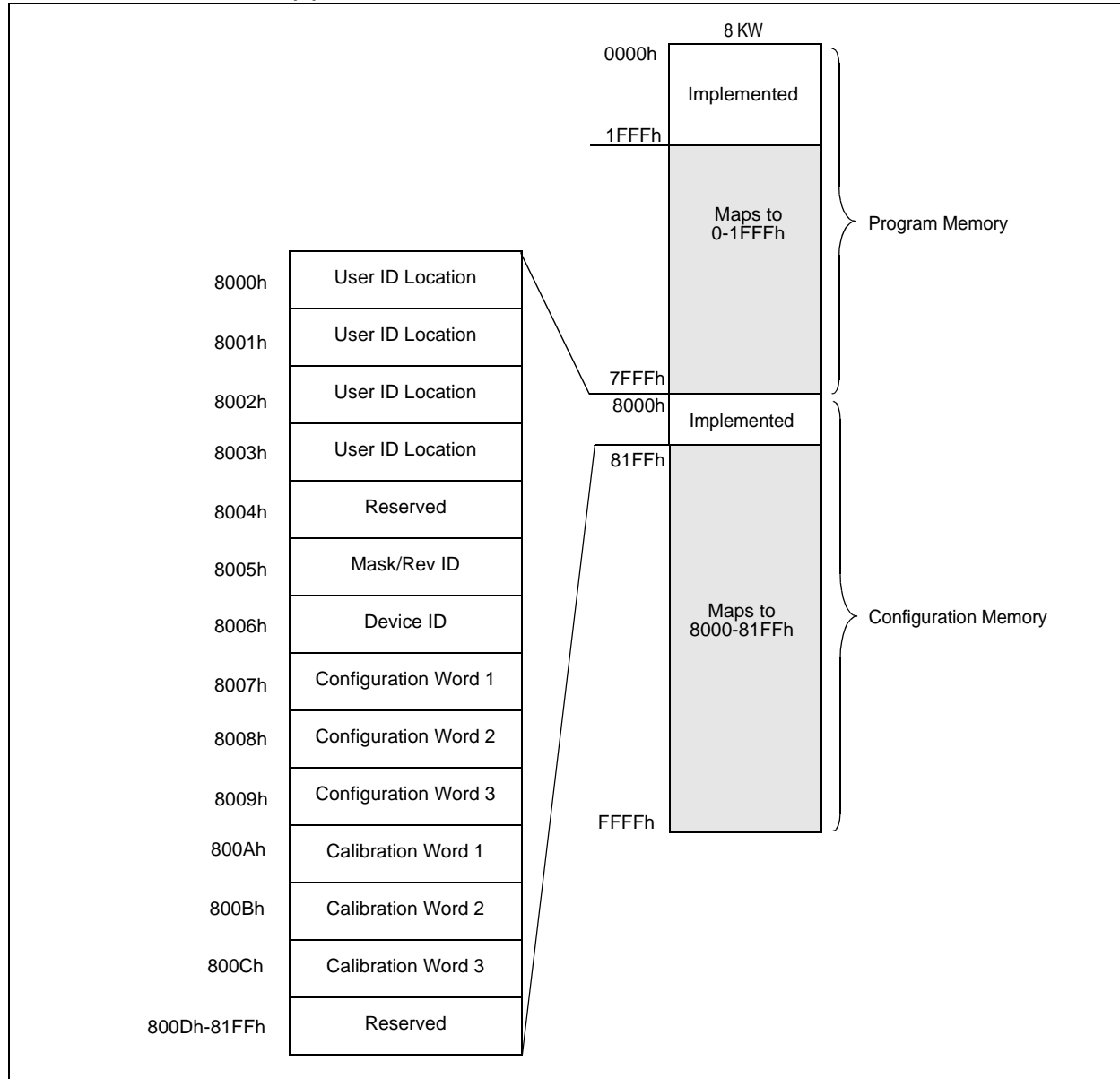
PIC12(L)F1612/16(L)F161X

FIGURE 3-2: PIC16(L)F1614/8 PROGRAM MEMORY MAPPING



PIC12(L)F1612/16(L)F161X

FIGURE 3-3: PIC16(L)F1615/9 PROGRAM MEMORY MAPPING



PIC12(L)F1612/16(L)F161X

3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note: MPLAB® IDE only displays the seven Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the seven LSbs be used if MPLAB® IDE is the primary tool used to read these addresses.

3.2 Revision ID

The revision ID word is located at 8005h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: REVISION ID: REVISION ID REGISTER⁽¹⁾

| | | | | | |
|--------|---|---------|---------|---------|---------|
| R | R | R | R | R | R |
| 1 | 0 | MJRREV5 | MJRREV4 | MJRREV3 | MJRREV2 |
| bit 13 | | | | | bit 8 |

| | | | | | | | |
|---------|---------|--------|--------|--------|--------|--------|--------|
| R | R | R | R | R | R | R | R |
| MJRREV1 | MJRREV0 | MNREV5 | MNREV4 | MNREV3 | MNREV2 | MNREV1 | MNREV0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit P = Programmable bit '1' = Bit is set '0' = Bit is cleared
-n = Value at POR W = Writable bit U = Unimplemented bit, read as '0' x = Bit is unknown

bit 13 **Reserved:** Read as '1'
bit 12 **Reserved:** Read as '0'
bit 11-6 **MJRREV<5:0>:** Major Revision ID bits
bit 5-0 **MNREV<5:0>:** Minor Revision ID bits

Note 1: This location cannot be written.

PIC12(L)F1612/16(L)F161X

3.3 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-2: DEVICE ID: DEVICE ID REGISTER⁽¹⁾

| | | | | | |
|--------|---|-------|-------|------|-------|
| R | R | R | R | R | R |
| 1 | 1 | DEV11 | DEV10 | DEV9 | DEV8 |
| bit 13 | | | | | bit 8 |

| | | | | | | | |
|-------|------|------|------|------|------|------|-------|
| R | R | R | R | R | R | R | R |
| DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | DEV2 | DEV1 | DEV0 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | | |
|-------------------|----------------------|---------------------------------------|----------------------|
| R = Readable bit | P = Programmable bit | '1' = Bit is set | '0' = Bit is cleared |
| -n = Value at POR | W = Writable bit | U = Unimplemented bit, read as '0' | x = Bit is unknown |

bit 13 **Reserved:** Read as '1'
bit 12 **Reserved:** Read as '1'
bit 11-0 **DEV<11:0>:** Device ID bits
 These bits are used to identify the part number.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

| DEVICE | DEVICE ID VALUES | |
|-------------|-------------------|-------------------|
| | DEV | REV |
| PIC12F1612 | 11 0000 0101 1000 | 10 xxxx xxxx xxxx |
| PIC12LF1612 | 11 0000 0101 1001 | 10 xxxx xxxx xxxx |
| PIC16F1613 | 11 0000 0100 1100 | 10 xxxx xxxx xxxx |
| PIC16LF1613 | 11 0000 0100 1101 | 10 xxxx xxxx xxxx |
| PIC16F1614 | 11 0000 0111 1000 | 10 xxxx xxxx xxxx |
| PIC16LF1614 | 11 0000 0111 1010 | 10 xxxx xxxx xxxx |
| PIC16F1615 | 11 0000 0111 1100 | 10 xxxx xxxx xxxx |
| PIC16LF1615 | 11 0000 0111 1110 | 10 xxxx xxxx xxxx |
| PIC16F1618 | 11 0000 0111 1001 | 10 xxxx xxxx xxxx |
| PIC16LF1618 | 11 0000 0111 1011 | 10 xxxx xxxx xxxx |
| PIC16F1619 | 11 0000 0111 1101 | 10 xxxx xxxx xxxx |
| PIC16LF1619 | 11 0000 0111 1111 | 10 xxxx xxxx xxxx |

3.4 Configuration Words

There are three Configuration Words, Configuration Word 1 (8007h), Configuration Word 2 (8008h) and Configuration Word 3 (8009h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

PIC12(L)F1612/16(L)F161X

3.5 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1, 2 and 3 (800Ah, 800Bh and 800Ch).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-3: CONFIGURATION WORD 1

| | | | | | |
|----------------------|---------------------|----------|-----------------------|-----------------------|------------------|
| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 |
| FCMEN ⁽⁴⁾ | IESO ⁽⁴⁾ | CLKOUTEN | BOREN1 ⁽¹⁾ | BOREN0 ⁽¹⁾ | — ⁽³⁾ |
| bit 13 | | | | | bit 8 |

| | | | | | | | |
|-------------------|-------|-------|-----|-----|----------------------|-------|-------|
| R/P-1 | R/P-1 | R/P-1 | U-1 | U-1 | R/P-1 | R/P-1 | R/P-1 |
| CP ⁽²⁾ | MCLRE | PWRTE | — | — | FOSC2 ⁽⁵⁾ | FOSC1 | FOSC0 |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-----------------------|----------------------|
| Legend: | W = Writable bit | '0' = Bit is cleared |
| R = Readable bit | '1' = Bit is set | x = Bit is unknown |
| -n = Value at POR | U = Unimplemented bit | P = Programmable Bit |

- bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit⁽⁴⁾
 1 = ON - Fail-Safe Clock Monitor is enabled
 0 = OFF - Fail-Safe Clock Monitor is disabled
- bit 12 **IESO:** Internal External Switchover bit⁽⁴⁾
 1 = ON - Internal/External Switchover (Two-Speed Start-up) mode is enabled
 0 = OFF - Internal/External Switchover mode is disabled
- bit 11 **CLKOUTEN:** Clock Out Enable bit
 1 = OFF - CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
 0 = ON - CLKOUT function is enabled on CLKOUT pin
- bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits⁽¹⁾
 11 = ON - Brown-out Reset enabled
 10 = SLEEP - Brown-out Reset enabled during operation and disabled in Sleep
 01 = SBODEN - Brown-out Reset controlled by SBOREN bit of the PCON register
 00 = OFF - Brown-out Reset disabled
- bit 8 **Unimplemented:** Read as '1'⁽³⁾
- bit 7 **CP:** Code Protection bit⁽²⁾
 1 = OFF - Program memory code protection is disabled
 0 = ON - Program memory code protection is enabled
- bit 6 **MCLRE:** MCLR/VPP Pin Function Select bit
 If LVP bit = 1 (ON):
 This bit is ignored.
 If LVP bit = 0 (OFF):
 1 = ON - MCLR/VPP pin function is MCLR; Weak pull-up enabled.
 0 = OFF - MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUA register.
- bit 5 **PWRTE:** Power-up Timer Enable bit⁽¹⁾
 1 = OFF - PWRT disabled
 0 = ON - PWRT enabled
- bit 4-3 **Unimplemented:** Read as '1'

- Note**
- 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 - 2: The entire program memory will be erased when the code protection is turned off.
 - 3: This bit should be maintained as '1' when programmed.
 - 4: These bits are only implemented on the PIC16(L)F1615/9. They act as **Unimplemented: Read as '1'** on all other parts in the family.
 - 5: This bit is forced to '1' on the PIC12(L)F1612 and PIC16(L)F1613/4/8.

PIC12(L)F1612/16(L)F161X

REGISTER 3-3: CONFIGURATION WORD 1 (CONTINUED)

| | | | |
|---------|--|--|--|
| bit 2-0 | FOSC<2:0> : Oscillator Selection bits | | |
| 111 | = ECH | - External Clock, High-Power mode: on CLKIN pin | |
| 110 | = ECM | - External Clock, Medium-Power mode: on CLKIN pin | |
| 101 | = ECL | - External Clock, Low-Power mode: on CLKIN pin | |
| 100 | = INTOSC | - I/O function on OSC1 pin | |
| 011 | = Reserved | | |
| 010 | = HS | - HS Oscillator, High-speed crystal/resonator connected between OSC1 and OSC2 pins | |
| 001 | = Reserved | | |
| 000 | = Reserved | | |

- Note**
- 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 - 2: The entire program memory will be erased when the code protection is turned off.
 - 3: This bit should be maintained as '1' when programmed.
 - 4: These bits are only implemented on the PIC16(L)F1615/9. They act as **Unimplemented: Read as '1'** on all other parts in the family.
 - 5: This bit is forced to '1' on the PIC12(L)F1612 and PIC16(L)F1613/4/8.

REGISTER 3-4: CONFIGURATION WORD 2

| | | | | | |
|--------------------|----------------------|-------|-------|--------|-------|
| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| LVP ⁽¹⁾ | DEBUG ⁽²⁾ | LPBOR | BORV | STVREN | PLLEN |
| bit 13 | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|------------------------|-------|-------|
| R/P-1 | U-1 | U-1 | U-1 | U-1 | R/P-1 | R/P-1 | R/P-1 |
| ZCD | — | — | — | — | PPS1WAY ⁽³⁾ | WRT1 | WRT0 |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-----------------------|----------------------|
| Legend: | W = Writable bit | '0' = Bit is cleared |
| R = Readable bit | '1' = Bit is set | x = Bit is unknown |
| -n = Value at POR | U = Unimplemented bit | P = Programmable Bit |

| | |
|---------|--|
| bit 13 | LVP : Low-Voltage Programming Enable bit ⁽¹⁾ |
| | 1 = ON - Low-voltage programming enabled |
| | 0 = OFF - High voltage on MCLR/VPP must be used for programming |
| bit 12 | DEBUG : Debugger mode ⁽²⁾ |
| | 1 = OFF - In-circuit debugger is disabled |
| | 0 = ON - In-circuit debugger is enabled |
| bit 11 | LPBOR : Low-Power BOR bit |
| | 1 = OFF - Low-Power BOR is disabled |
| | 0 = ON - Low-Power BOR is enabled |
| bit 10 | BORV : Brown-out Reset Voltage Selection bit |
| | 1 = LOW - Brown-out Reset Voltage (VBOR) set to 1.9V on LF devices, and 2.45V on F devices |
| | 0 = HIGH - Brown-out Reset Voltage (VBOR) set to 2.7V |
| bit 9 | STVREN : Stack Overflow/Underflow Reset Enable bit |
| | 1 = ON - Stack Overflow or Underflow will cause a Reset |
| | 0 = OFF - Stack Overflow or Underflow will not cause a Reset |
| bit 8 | PLLEN : PLL Enable bit |
| | 1 = ON - 4x PLL will be enabled for external clock, if FOSC = EC, or for INTOSC, if IRCF = 8 MHz or 16 MHz |
| | 0 = OFF - 4x PLL disabled |
| bit 7 | ZCD : ZCD Disable bit |
| | 1 = OFF - ZCD disabled. ZCD can be enabled by setting the ZCDSEN bit of ZCDCON |
| | 0 = ON - ZCD always enabled |
| bit 6-3 | Unimplemented : Read as '1' |

- Note**
- 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
 - 2: The Debug mode is controlled by the MPLAB[®] IDE.
 - 3: This bit is only implemented on the PIC16(L)F1614/5/8/9. It acts as **Unimplemented: Read as '1'** on all other parts in the family.

PIC12(L)F1612/16(L)F161X

REGISTER 3-4: CONFIGURATION WORD 2 (CONTINUED)

- bit 2 **PPS1WAY:** PPSLOCK bit, One-Way Set Enable bit⁽³⁾
 1 = ON - The PPSLOCK bit is permanently set after the first access sequence that sets it.
 0 = OFF - The PPSLOCK bit can be set and cleared as needed by the PPSLOCK access sequence.
- bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits
2 kW Flash memory (PIC12(L)F1612/16(L)F1613):
 11 = OFF - Write protection off
 10 = BOOT - 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
 01 = HALF - 000h to 3FFh write-protected, 400h to 7FFh may be modified by PMCON control
 00 = ALL - 000h to 7FFh write-protected, no addresses may be modified by PMCON control
4 kW Flash memory (PIC16(L)F1614/8):
 11 = OFF - Write protection off
 10 = BOOT - 000h to 1FFh write-protected, 200h to FFFh may be modified by PMCON control
 01 = HALF - 000h to 7FFh write-protected, 800h to FFFh may be modified by PMCON control
 00 = ALL - 000h to FFFh write-protected, no addresses may be modified by PMCON control
8 kW Flash memory (PIC16(L)F1615/9):
 11 = OFF - Write protection off
 10 = BOOT - 0000h to 01FFh write-protected, 0200h to 1FFF may be modified by PMCON control
 01 = HALF - 0000h to 0FFFh write-protected, 1000h to 1FFF may be modified by PMCON control
 00 = ALL - 0000h to 1FFFh write-protected, no addresses may be modified by PMCON control

- Note 1:** The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.
Note 2: The Debug mode is controlled by the MPLAB[®] IDE.
Note 3: This bit is only implemented on the PIC16(L)F1614/5/8/9. It acts as **Unimplemented: Read as '1'** on all other parts in the family.

REGISTER 3-5: CONFIGURATION WORD 3

| | | | | | |
|---------|---------|---------|---------|---------|---------|
| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| WDTCCS2 | WDTCCS1 | WDTCCS0 | WDTCWS2 | WDTCWS1 | WDTCWS0 |
| bit 13 | | | | | bit 8 |

| | | | | | | | |
|-------|-------|-------|--------|--------|--------|--------|--------|
| U-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| — | WDTE1 | WDTE1 | WDTCP4 | WDTCP3 | WDTCP2 | WDTCP1 | WDTCP0 |
| bit 7 | | | | | | | bit 0 |

| | | |
|-------------------|-----------------------|----------------------|
| Legend: | W = Writable bit | '0' = Bit is cleared |
| R = Readable bit | '1' = Bit is set | x = Bit is unknown |
| -n = Value at POR | U = Unimplemented bit | P = Programmable Bit |

- bit 13-11 **WDTCCS<2:0>:** WDT Input Clock Selector bit:
 000 = WDT reference clock is the 31.0 kHz LFINTOSC (default value)
 001 = WDT reference clock is the 31.25 kHz MFINTOSC output
 010 = Reserved
 ...
 110 = Reserved
 111 = SWC - Software Control, controlled by WDTCS bits
- bit 10-8 **WDTCWS<2:0>:** WDT Window Select bits:
 000 = WDTCWS125 - 12.5% window open time (87.5% delay time)
 001 = WDTCWS25 - 25% window open time (75% delay time)
 010 = WDTCWS375 - 37.5% window open time (62.5% delay time)
 011 = WDTCWS50 - 50% window open time (50% delay time)
 100 = WDTCWS625 - 62.5% window open time (37.5% delay time)
 101 = WDTCWS75 - 75% window open time (25% delay time)
 110 = WDTCWS100 - 100% window open time (Legacy WDT)
 111 = WDTCWSW - Software WDT window size control (controlled by WDTWS)

- bit 7 **Unimplemented:** Read as '1'
- Note 1:** Typical time-out based on 31 kHz clock.
Note 2: Software-controlled (WDTWS).

PIC12(L)F1612/16(L)F161X

REGISTER 3-5: CONFIGURATION WORD 3 (CONTINUED)

| | |
|---------|---|
| bit 6-5 | WDTE<1:0> : WDT Operating mode: |
| | 00 = OFF - WDT disabled, SWDTEN is ignored |
| | 01 = SWDTEN - WDT enabled/disabled by SWDTEN bit in WDTCOON |
| | 10 = NSLEEP - WDT enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN ignored |
| | 11 = ON - WDT enabled regardless of Sleep; SWDTEN is ignored |
| bit 4-0 | WDTCPSS<4:0> : WDT Period Select bits: |
| | 00000 = WDTCPSS0 - 1:32 (1 ms period) ⁽¹⁾ |
| | 00001 = WDTCPSS1 - 1:64 (2 ms period) ⁽¹⁾ |
| | 00010 = WDTCPSS2 - 1:128 (4 ms period) ⁽¹⁾ |
| | 00011 = WDTCPSS3 - 1:256 (8 ms period) ⁽¹⁾ |
| | 00100 = WDTCPSS4 - 1:512 (16 ms period) ⁽¹⁾ |
| | 00101 = WDTCPSS5 - 1:1024 (32 ms period) ⁽¹⁾ |
| | 00110 = WDTCPSS6 - 1:2048 (64 ms period) ⁽¹⁾ |
| | 00111 = WDTCPSS7 - 1:4096 (128 ms period) ⁽¹⁾ |
| | 01000 = WDTCPSS8 - 1:8192 (256 ms period) ⁽¹⁾ |
| | 01001 = WDTCPSS9 - 1:16384 (512 ms period) ⁽¹⁾ |
| | 01010 = WDTCPSSA - 1:32768 (1s period) ⁽¹⁾ |
| | 01011 = WDTCPSSB - 1:65536 (2s period) ⁽¹⁾ |
| | 01100 = WDTCPSSC - 1:131072 (4s period) ⁽¹⁾ |
| | 01101 = WDTCPSSD - 1:262144 (8s period) ⁽¹⁾ |
| | 01110 = WDTCPSE - 1:524288 (16s period) ⁽¹⁾ |
| | 01111 = WDTCPSSF - 1:1048576 (32s period) ⁽¹⁾ |
| | 10000 = WDTCPSS10 - 1:2097152 (64s period) ⁽¹⁾ |
| | 10001 = WDTCPSS11 - 1:4194304 (128s period) ⁽¹⁾ |
| | 10010 = WDTCPSS12 - 1:8388608 (256s period) ⁽¹⁾ |
| | 10011 = Reserved |
| | ... |
| | 11110 = Reserved |
| | 11111 = WDTCPSS1F - 1:65536 (2s period) ^{(1), (2)} |

Note 1: Typical time-out based on 31 kHz clock.

Note 2: Software-controlled (WDTSS).

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSB first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to V_{IH} .
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, the device will execute code when Configuration Word 1 has MCLR disabled ($\text{MCLRE} = 0$), the Power-up Timer is disabled ($\text{PWRTE} = 0$), the internal oscillator is selected ($\text{FOSC} = 100$), and ICSPCLK and ICSPDAT pins are driven by the user application. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in [Figure 8-2](#).

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to V_{IH} .

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in [Figure 8-1](#).

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (V_{IL}). See [Figure 8-3](#) and [Figure 8-4](#).

| |
|---|
| Note: In systems where the VDD and $\overline{\text{MCLR}}$ /VPP signals can be controlled independently, the VPP-last method of exit should be used to keep the device in Reset, thereby preventing any issues that may be caused by program execution. |
|---|

PIC12(L)F1612/16(L)F161X

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows devices to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see [Figure 8-8](#) and [Figure 8-9](#).

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to VIL. See [Figure 8-8](#) and [Figure 8-9](#).

| |
|---|
| Note: To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts. |
|---|

PIC12(L)F1612/16(L)F161X

4.3 Program/Verify Commands

The devices implement ten programming commands; each six bits in length. The commands are summarized in [Table 4-1](#). Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

| Command | Mapping | | | | | | Data/Note | |
|------------------------------------|----------------------|---|---|---|---|---|-----------|------------------|
| | Binary (MSb ... LSb) | | | | | | | Hex |
| Load Configuration | x | 0 | 0 | 0 | 0 | 0 | 00h | 0, data (14), 0 |
| Load Data For Program Memory | x | 0 | 0 | 0 | 1 | 0 | 02h | 0, data (14), 0 |
| Read Data From Program Memory | x | 0 | 0 | 1 | 0 | 0 | 04h | 0, data (14), 0 |
| Increment Address | x | 0 | 0 | 1 | 1 | 0 | 06h | — |
| Reset Address | x | 1 | 0 | 1 | 1 | 0 | 16h | — |
| Begin Internally Timed Programming | x | 0 | 1 | 0 | 0 | 0 | 08h | — |
| Begin Externally Timed Programming | x | 1 | 1 | 0 | 0 | 0 | 18h | — |
| End Externally Timed Programming | x | 0 | 1 | 0 | 1 | 0 | 0Ah | — |
| Bulk Erase Program Memory | x | 0 | 1 | 0 | 0 | 1 | 09h | Internally Timed |
| Row Erase Program Memory | x | 1 | 0 | 0 | 0 | 1 | 11h | Internally Timed |

4.3.1 LOAD CONFIGURATION

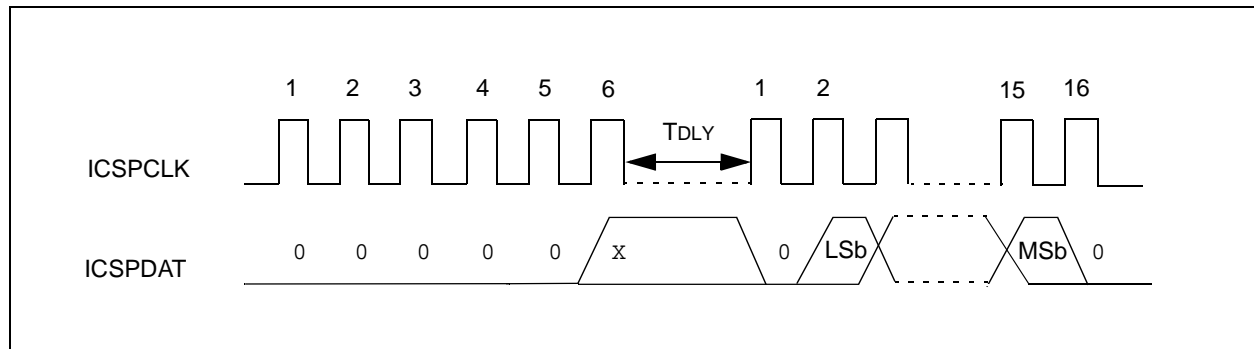
The Load Configuration command is used to access the configuration memory (user ID locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see [Figure 4-1](#)).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note: Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

FIGURE 4-1: LOAD CONFIGURATION

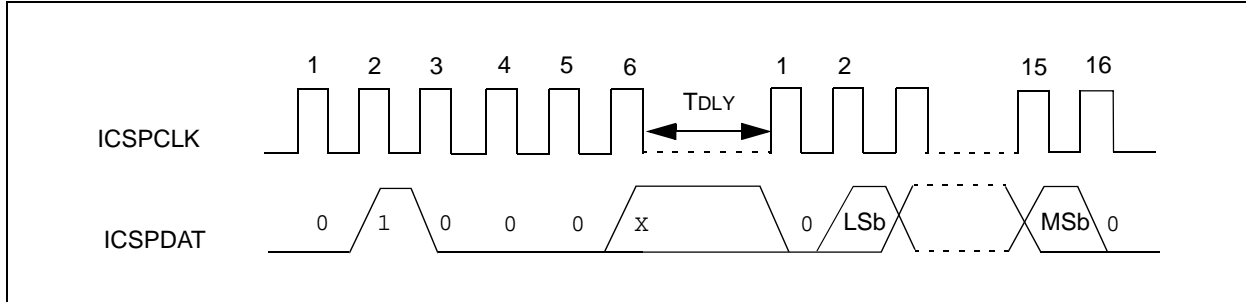


PIC12(L)F1612/16(L)F161X

4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see [Figure 4-2](#)).

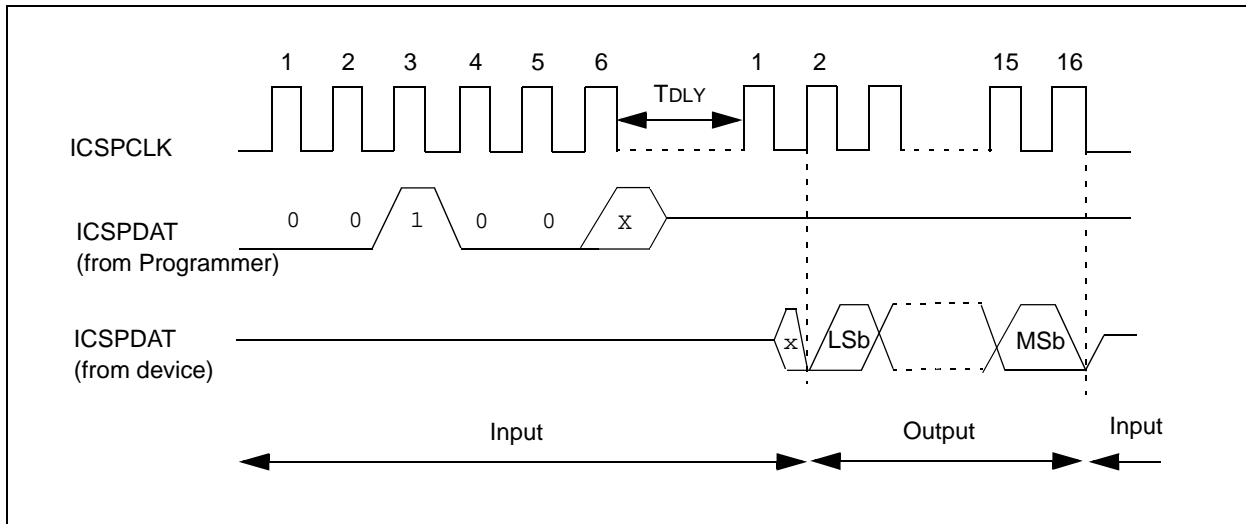
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected (\overline{CP}), the data will be read as zeros (see [Figure 4-3](#)).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY

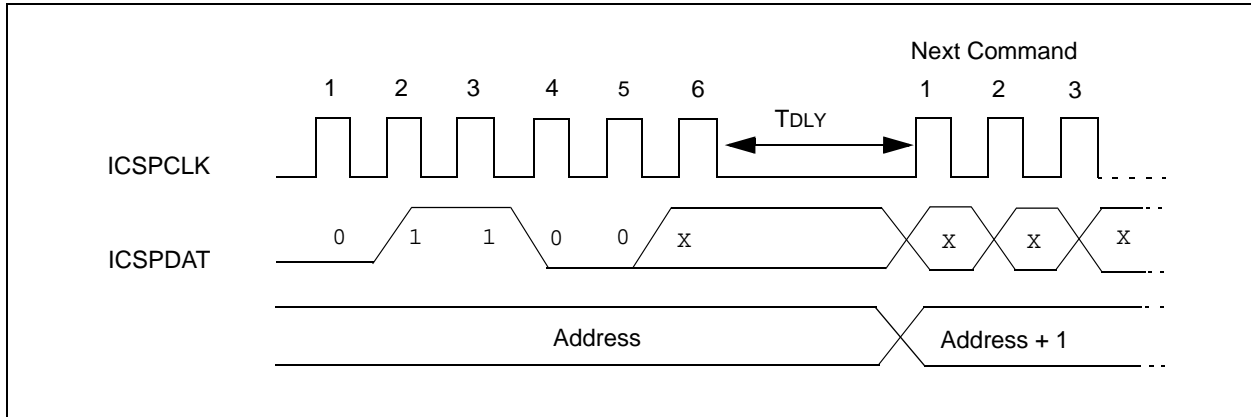


PIC12(L)F1612/16(L)F161X

4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 07FFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

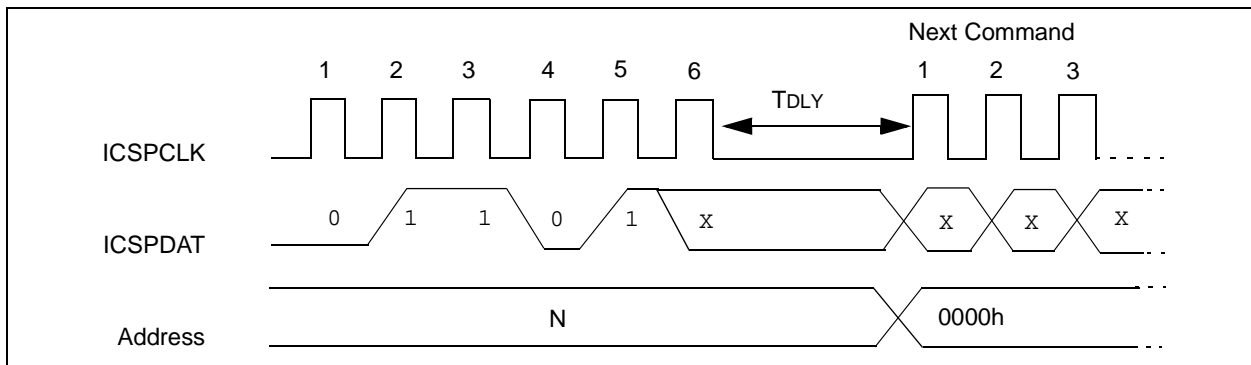
FIGURE 4-4: INCREMENT ADDRESS



4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-5: RESET ADDRESS



PIC12(L)F1612/16(L)F161X

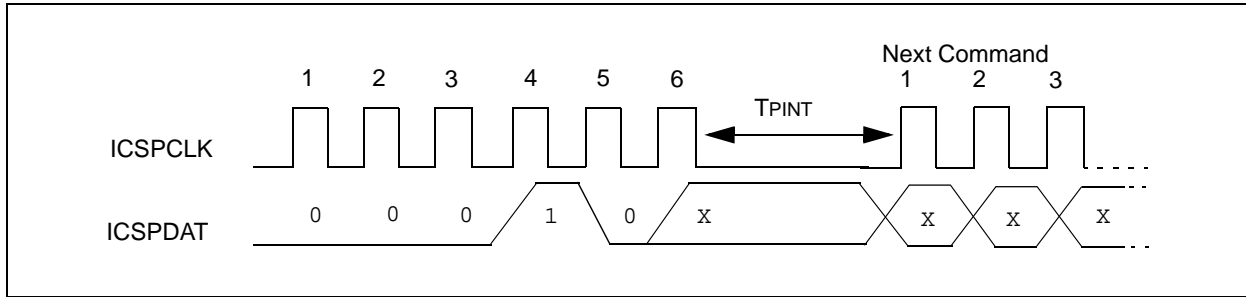
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, $TPINT$, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

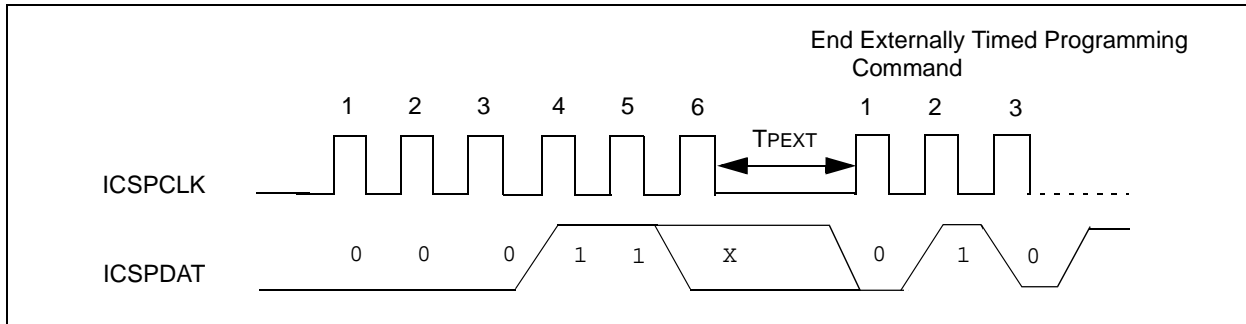


4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming the End Externally Timed Programming command must be sent in the specified time window defined by $TPEXT$ (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING



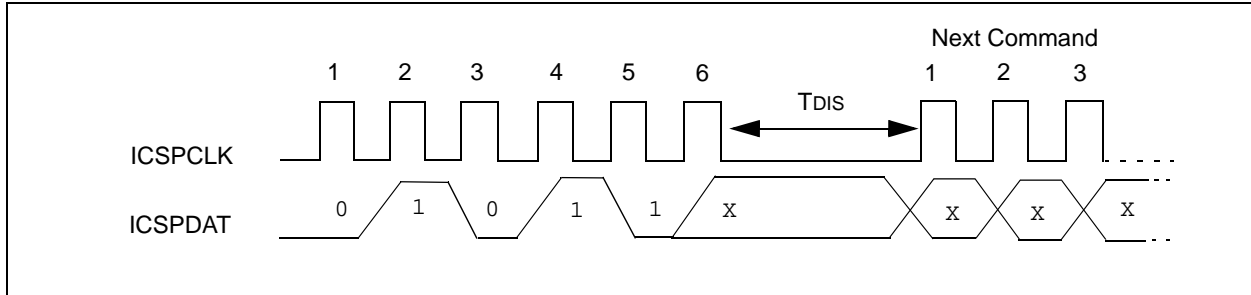
PIC12(L)F1612/16(L)F161X

4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-07FFh:

- Program Memory is erased
- Configuration Words are erased

Address 8000h-8009h:

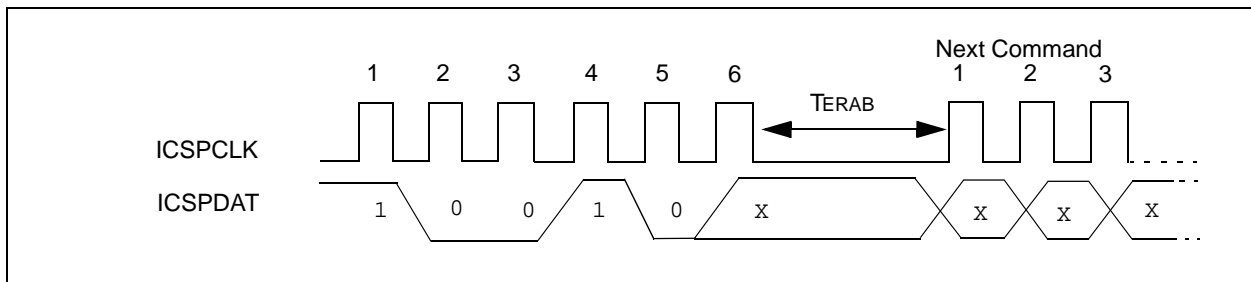
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8009h.

After receiving the Bulk Erase Program Memory command the erase will not complete until the time interval, TERAB, has expired.

Note: The code protection Configuration bit (\overline{CP}) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY



PIC12(L)F1612/16(L)F161X

4.3.10 ROW ERASE PROGRAM MEMORY

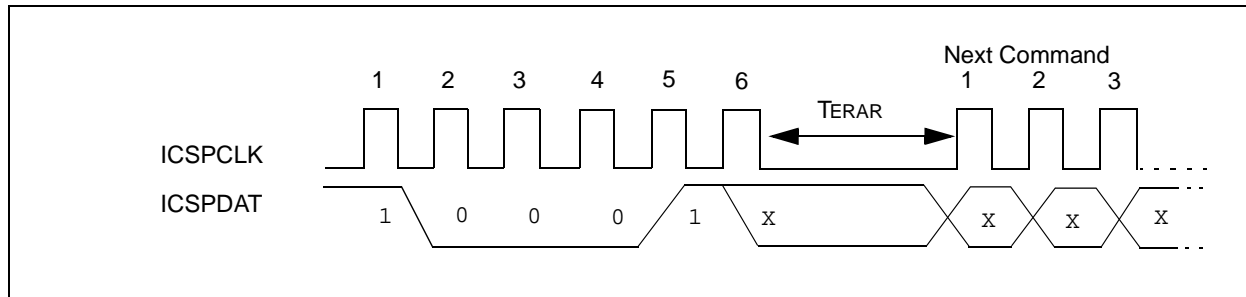
The Row Erase Program Memory command will erase an individual row. Refer to [Table 4-2](#) for row sizes of specific devices and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8009h, the Row Erase Program Memory command will only erase the user ID locations, regardless of the setting of the CP Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, TERAR, has expired.

TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES

| Devices | PC | Row Size | Number of Latches |
|---------------|--------|----------|-------------------|
| PIC12(L)F1612 | <15:5> | 16 | 16 |
| PIC16(L)F1613 | <15:5> | 16 | 16 |
| PIC16(L)F1614 | <15:5> | 32 | 32 |
| PIC16(L)F1615 | <15:5> | 32 | 32 |
| PIC16(L)F1618 | <15:5> | 32 | 32 |
| PIC16(L)F1619 | <15:5> | 32 | 32 |

FIGURE 4-10: ROW ERASE PROGRAM MEMORY



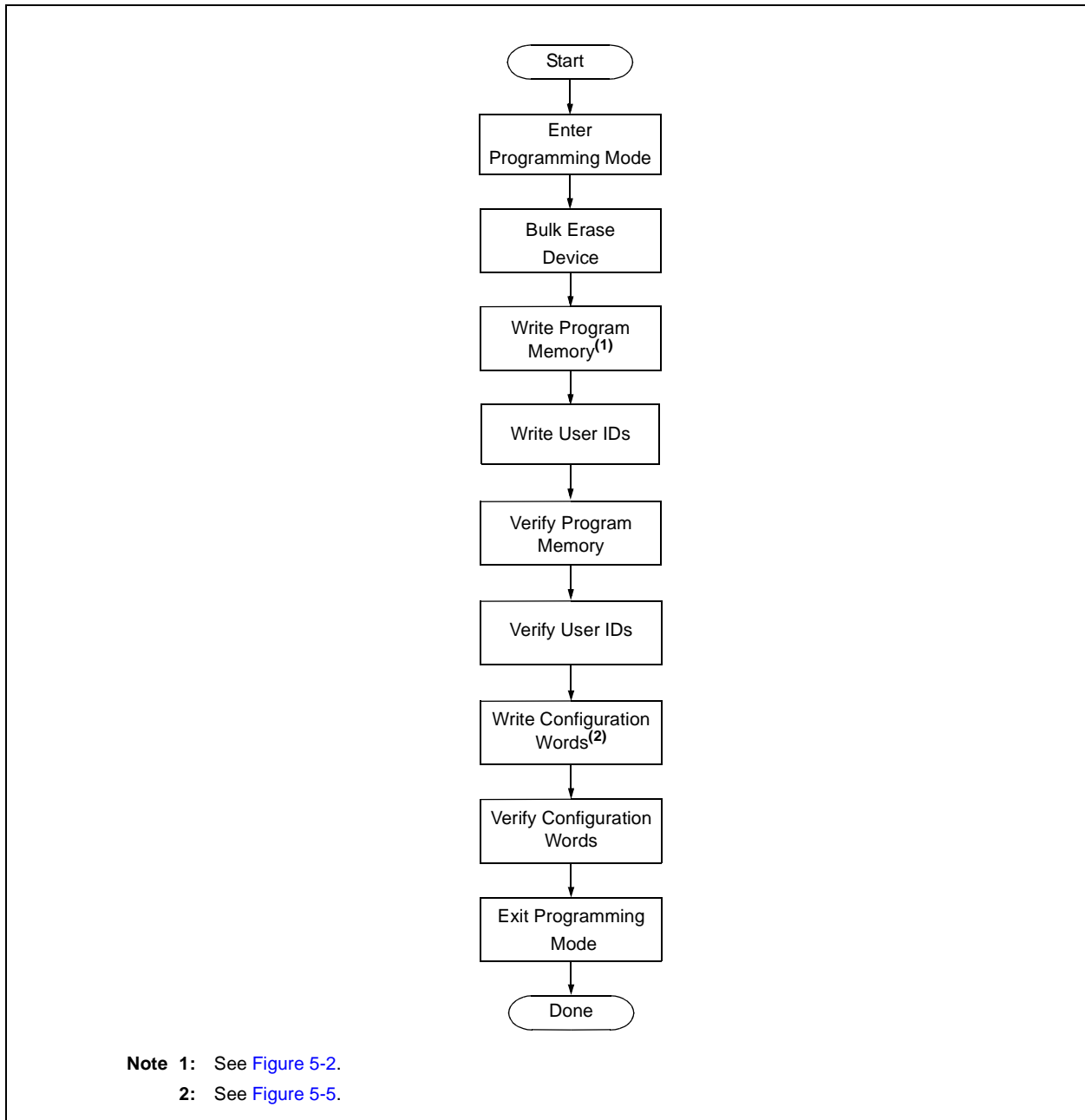
5.0 PROGRAMMING ALGORITHMS

The devices use internal latches to temporarily store the 14-bit words used for programming. Refer to [Table 4-2](#) for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSBs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written.

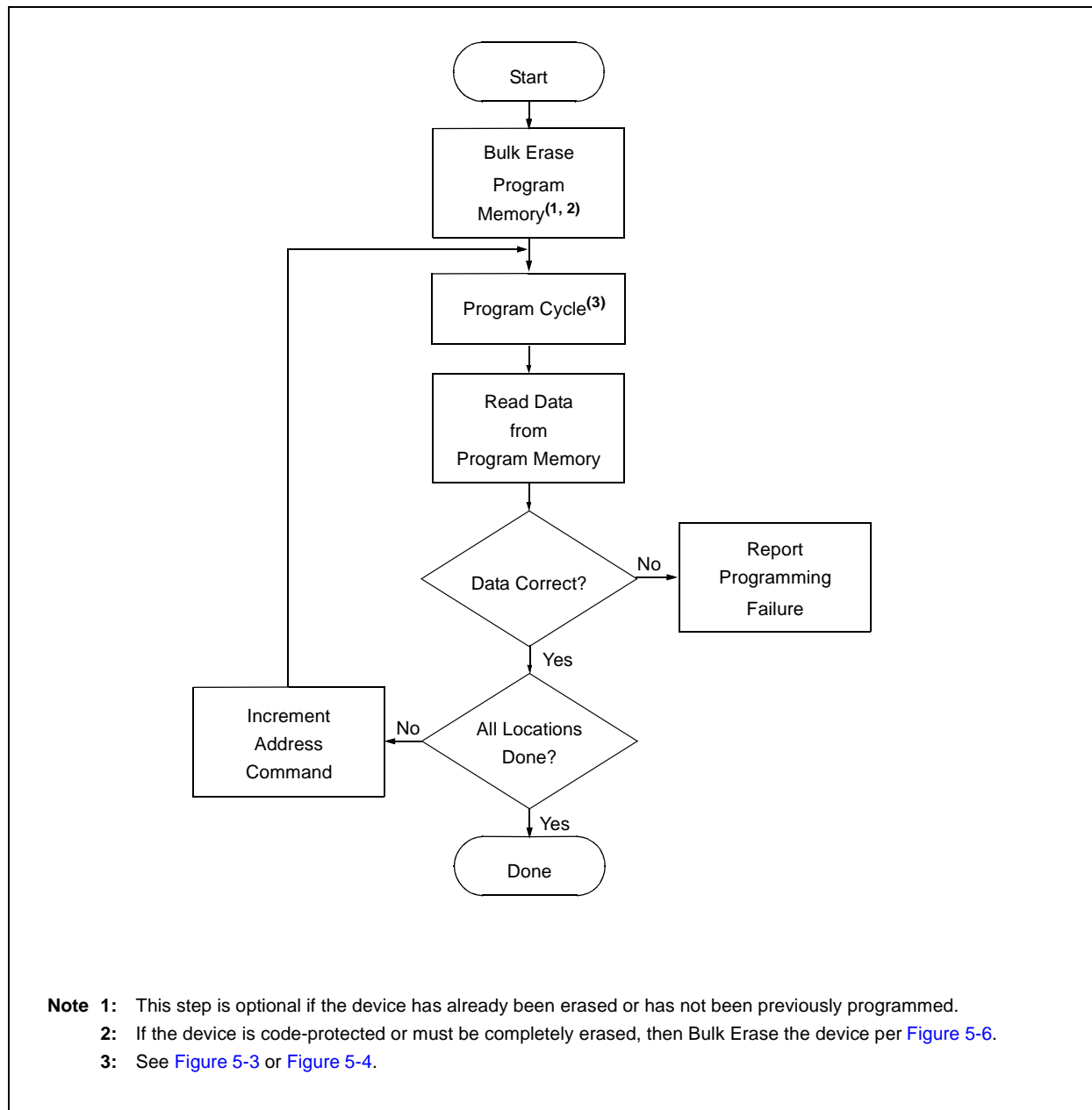
If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



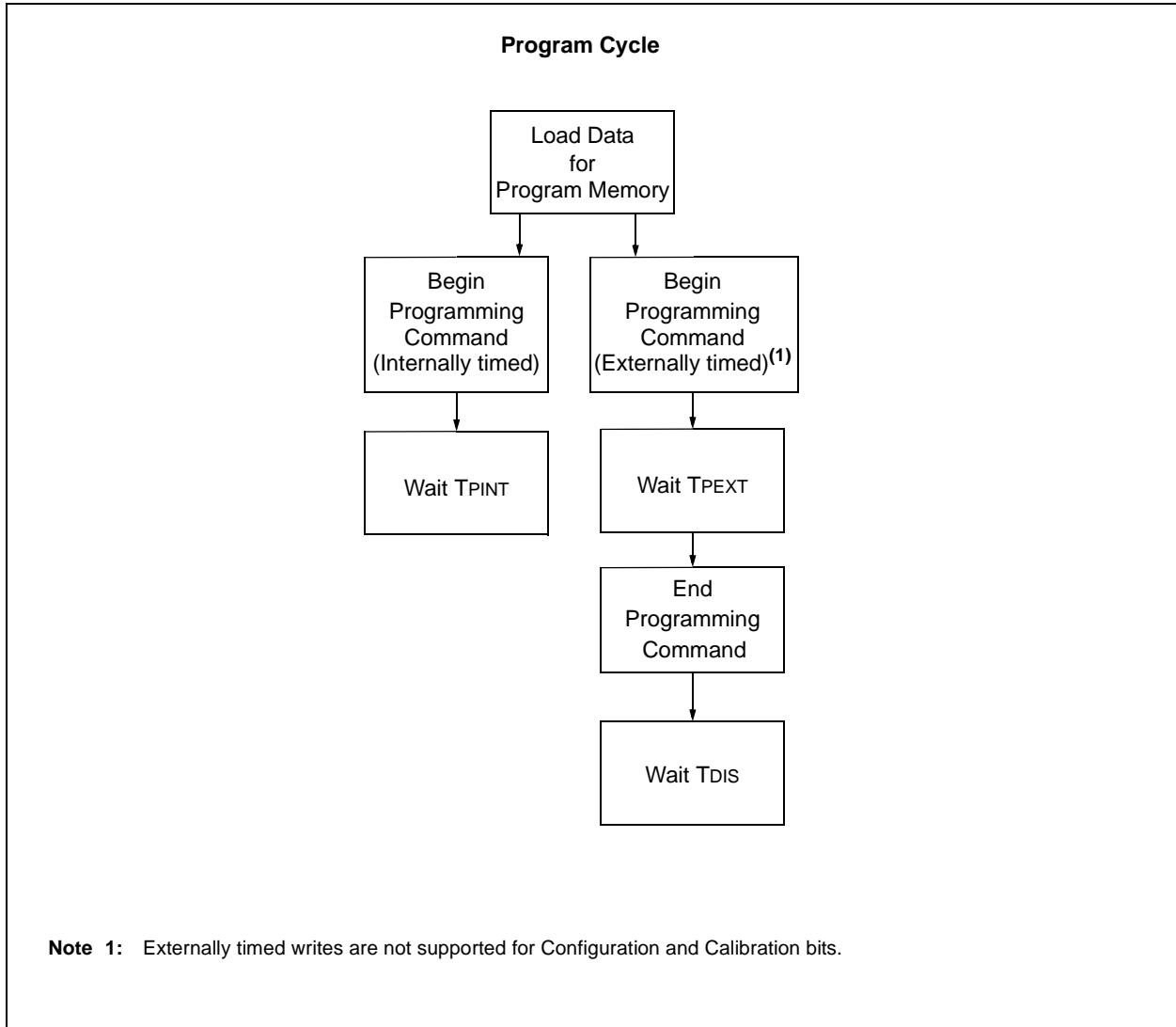
PIC12(L)F1612/16(L)F161X

FIGURE 5-2: PROGRAM MEMORY FLOWCHART



- Note 1:** This step is optional if the device has already been erased or has not been previously programmed.
Note 2: If the device is code-protected or must be completely erased, then Bulk Erase the device per [Figure 5-6](#).
Note 3: See [Figure 5-3](#) or [Figure 5-4](#).

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



PIC12(L)F1612/16(L)F161X

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

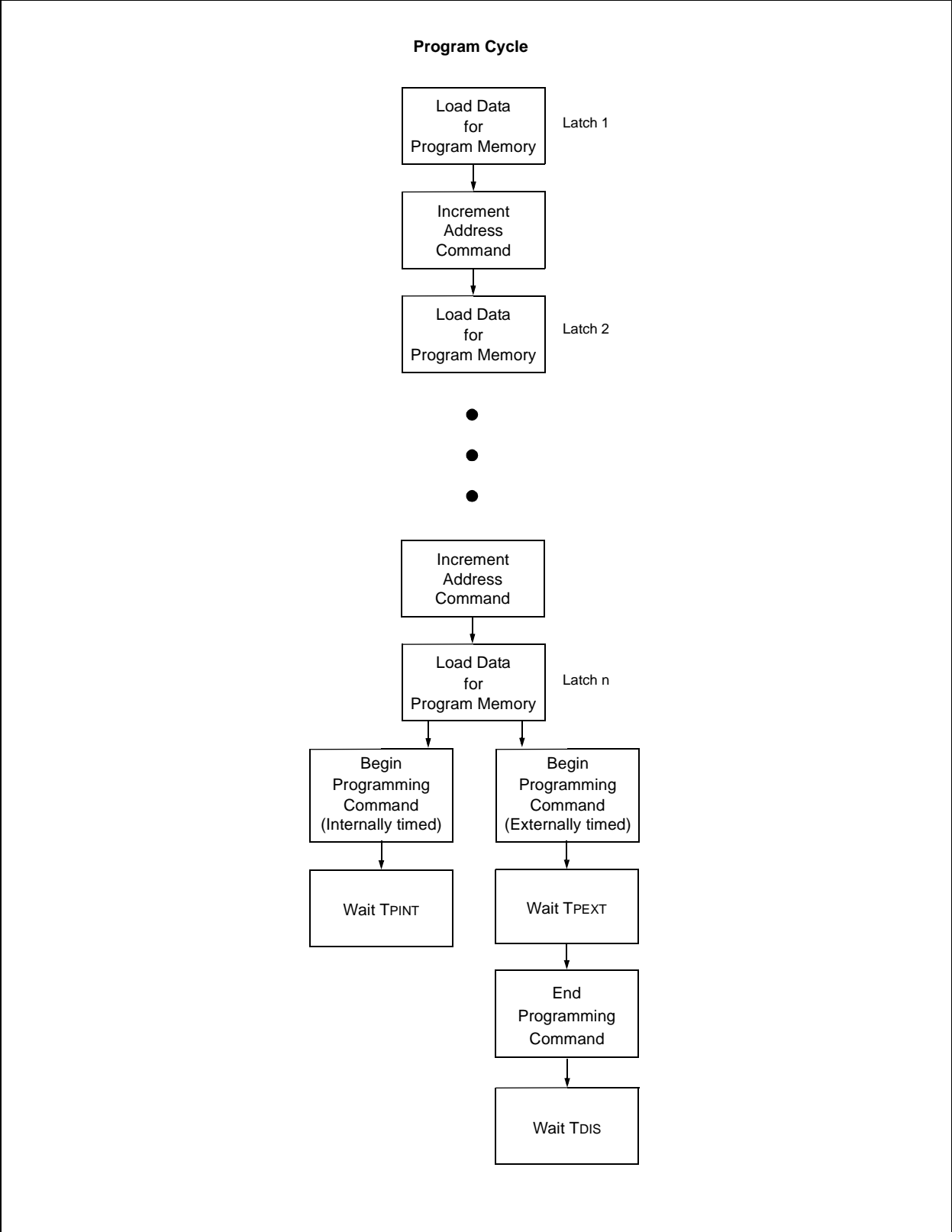
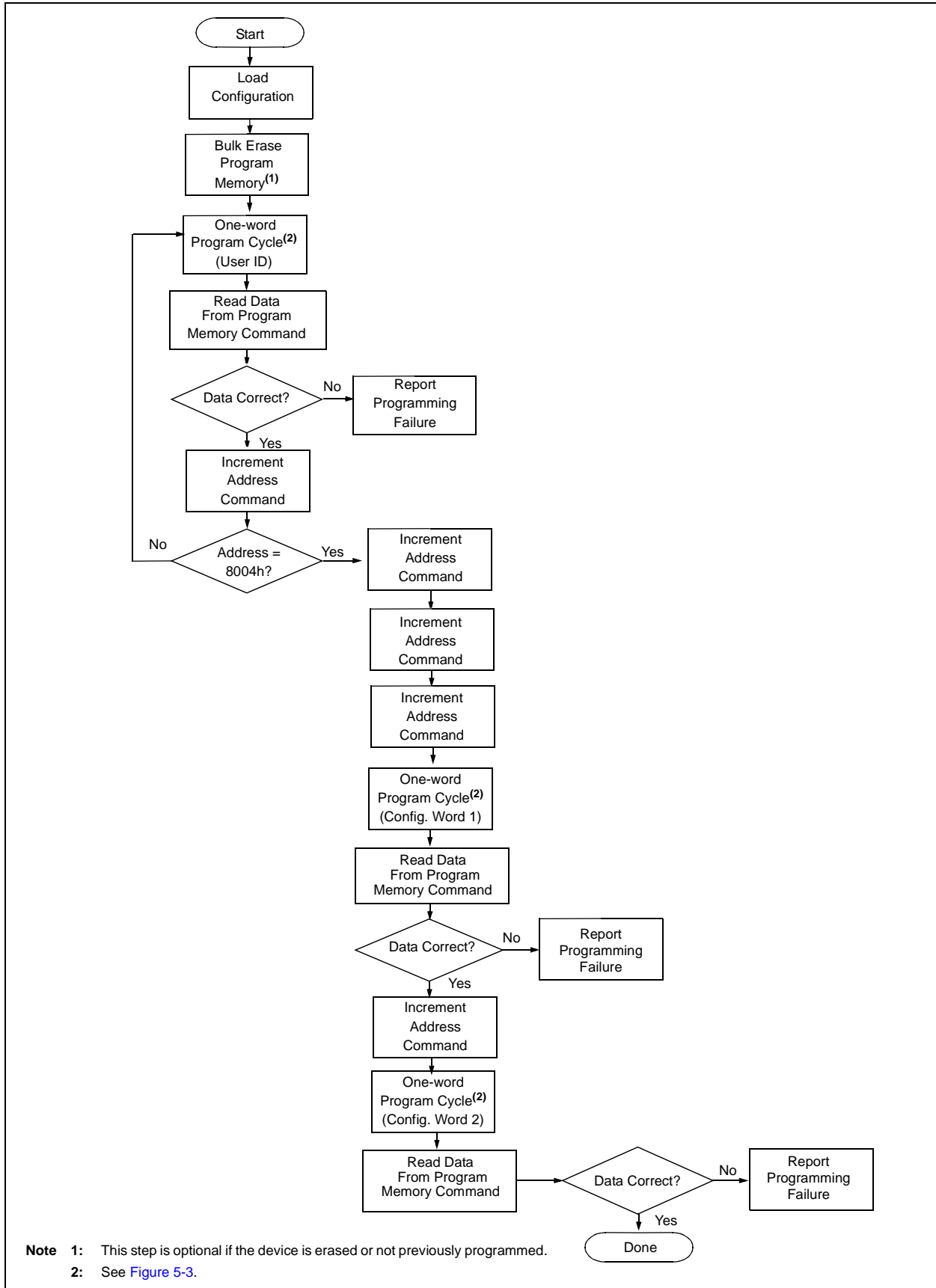
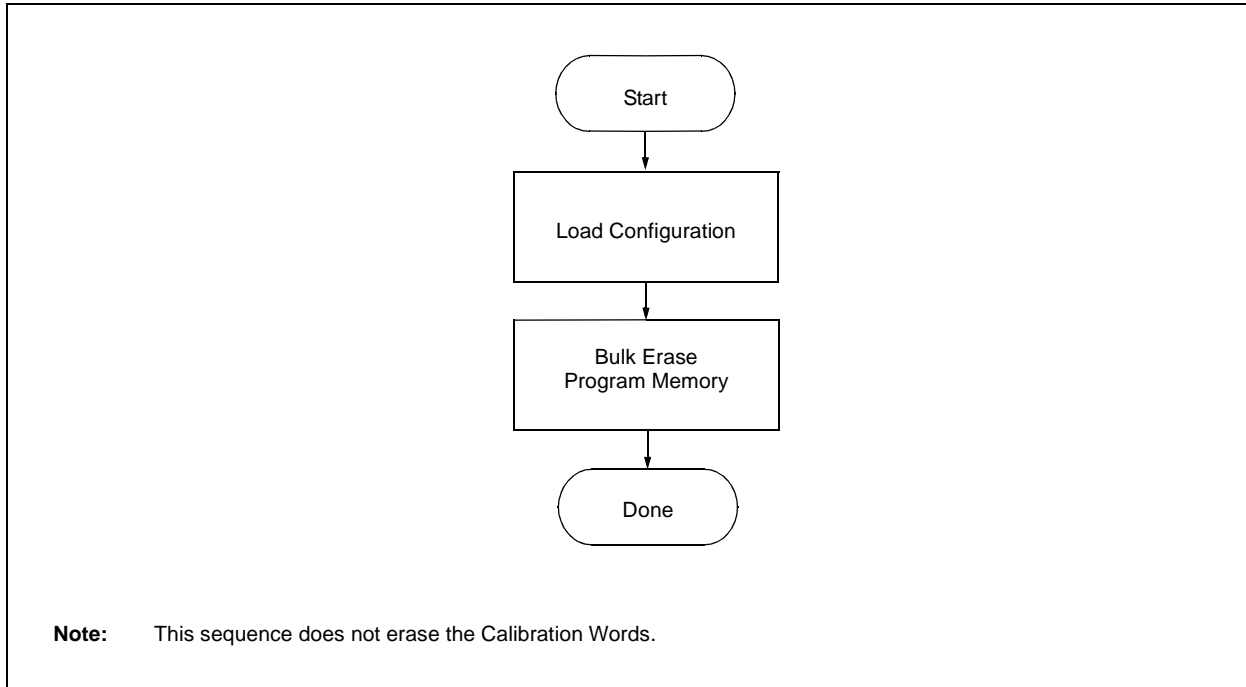


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



PIC12(L)F1612/16(L)F161X

FIGURE 5-6: ERASE FLOWCHART



6.0 CODE PROTECTION

Code protection is controlled using the \overline{CP} bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-07FFh) read as '0'. Further programming is disabled for the program memory (0000h-07FFh). The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the \overline{CP} bit in Configuration Word 1 register to '0'. The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel[®] INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID against the value read from the part. On a mismatch condition the programmer should generate a warning message.

PIC12(L)F1612/16(L)F161X

7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the \overline{CP} Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

| Part Variant | Config. Word 1 Mask | Config. Word 2 Mask | Config. Word 3 Mask |
|--------------------------|---------------------|---------------------|---------------------|
| PIC12(L)F1612/16(L)F1613 | 0EE3h | 3F83h | 3F7Fh |
| PIC16(L)F1614/8 | 0EE3h | 3F87h | 3F7Fh |
| PIC16(L)F1615/9 | 3EE3h | 3F87h | 3F7Fh |

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

7.3.2 PROGRAM CODE PROTECTION ENABLED

When the MPLAB[®] IDE check box for Dashboard→Project Properties→Conf:→Building→Insert Checksum in User ID Memory is checked, then the 16-bit checksum of the equivalent unprotected device is computed and stored in the user ID. Each nibble of the unprotected checksum is stored in the Least Significant nibble of each of the four user ID locations. The Most Significant checksum nibble is stored in the user ID at location 8000h, the second Most Significant nibble is stored at location 8001h, and so forth for the remaining nibbles and ID locations. The protected checksums in [Table 7-2](#) assume that the Insert Checksum in User ID Memory box is checked.

The checksum of a code-protected device is computed in the following manner: the Least Significant nibble of each user ID is used to create a 16-bit value. The Least Significant nibble of user ID location 8000h is the Most Significant nibble of the 16-bit value. The Least Significant nibble of user ID location 8001h is the second Most Significant nibble, and so forth for the remaining user IDs and 16-bit value nibbles. The resulting 16-bit value is summed with the Configuration Words. All unimplemented Configuration bits are masked to '0'.

TABLE 7-2: CHECKSUMS

| Device | Config1 | | | Config2 | | Config3 | | Checksum | | | |
|-------------|-------------|-----------|-------|---------|-------|---------|-------|-------------|----------------------|----------------|----------------------|
| | Unprotected | Protected | Mask | Word | Mask | Word | Mask | Unprotected | | Code-protected | |
| | | | | | | | | Blank | 00AAh First and Last | Blank | 00AAh First and Last |
| PIC12F1612 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F83h | 3FFFh | 3F7Fh | 85E5h | 073Bh | 134Ah | 94A0h |
| PIC16F1613 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F83h | 3FFFh | 3F7Fh | 85E5h | 073Bh | 134Ah | 94A0h |
| PIC16F1614 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 7DE9h | FF3Fh | 0B4Eh | 8CA4h |
| PIC16F1615 | 3FFFh | 3F7Fh | 3EE7h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 9DEDh | 1F43h | 5B56h | DCACH |
| PIC16F1618 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 7DE9h | FF3Fh | 0B4Eh | 8CA4h |
| PIC16F1619 | 3FFFh | 3F7Fh | 3EE7h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 9DEDh | 1F43h | 5B56h | DCACH |
| PIC12LF1612 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F83h | 3FFFh | 3F7Fh | 85E5h | 073Bh | 134Ah | 94A0h |
| PIC16LF1613 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F83h | 3FFFh | 3F7Fh | 85E5h | 073Bh | 134Ah | 94A0h |
| PIC16LF1614 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 7DE9h | FF3Fh | 0B4Eh | 8CA4h |
| PIC16LF1615 | 3FFFh | 3F7Fh | 3EE7h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 9DEDh | 1F43h | 5B56h | DCACH |
| PIC16LF1618 | 3FFFh | 3F7Fh | 0EE3h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 7DE9h | FF3Fh | 0B4Eh | 8CA4h |
| PIC16LF1619 | 3FFFh | 3F7Fh | 3EE7h | 3FFFh | 3F87h | 3FFFh | 3F7Fh | 9DEDh | 1F43h | 5B56h | DCACH |

PIC12(L)F1612/16(L)F161X

8.0 ELECTRICAL SPECIFICATIONS

Refer to the device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

| AC/DC CHARACTERISTICS | | Standard Operating Conditions Production tested at 25°C | | | | |
|--|---|--|------|--|---------------|--|
| Sym. | Characteristics | Min. | Typ. | Max. | Units | Conditions/Comments |
| Supply Voltages and Currents | | | | | | |
| | VDD | | | | | |
| VDD | Read/Write and Row Erase operations | VDD min. | — | VDD max. | V | |
| | Bulk Erase operations | 2.7 | — | VDD max. | V | |
| IDDI | Current on VDD, Idle | — | — | 1.0 | mA | |
| IDDP | Current on VDD, Programming | — | — | 3.0 | mA | |
| | VPP | | | | | |
| IPP | Current on $\overline{\text{MCLR}}/\text{VPP}$ | — | — | 600 | μA | |
| V _{IHH} | High voltage on $\overline{\text{MCLR}}/\text{VPP}$ for Program/Verify mode entry | 8.0 | — | 9.0 | V | |
| T _{VHHR} | $\overline{\text{MCLR}}$ rise time (V _{IL} to V _{IHH}) for Program/Verify mode entry | — | — | 1.0 | μs | |
| | I/O pins | | | | | |
| V _{IH} | (ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}/\text{VPP}$) input high level | 0.8 V _{DD} | — | — | V | |
| V _{IL} | (ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}/\text{VPP}$) input low level | — | — | 0.2 V _{DD} | V | |
| V _{OH} | ICSPDAT output high level | V _{DD} -0.7 V _{DD} -0.7 V _{DD} -0.7 | — | — | V | IOH = 3.5 mA, V _{DD} = 5V IOH = 3 mA, V _{DD} = 3.3V IOH = 2 mA, V _{DD} = 1.8V |
| V _{OL} | ICSPDAT output low level | — | — | V _{SS} +0.6 V _{SS} +0.6 V _{SS} +0.6 | V | IOH = 8 mA, V _{DD} = 5V IOH = 6 mA, V _{DD} = 3.3V IOH = 3 mA, V _{DD} = 1.8V |
| Programming Mode Entry and Exit | | | | | | |
| TENTS | Programming mode entry setup time: ICSPCLK, ICSPDAT setup time before V _{DD} or $\overline{\text{MCLR}}\uparrow$ | 100 | — | — | ns | |
| TENTH | Programming mode entry hold time: ICSPCLK, ICSPDAT hold time after V _{DD} or $\overline{\text{MCLR}}\uparrow$ | 250 | — | — | μs | |
| Serial Program/Verify | | | | | | |
| TCKL | Clock Low Pulse Width | 100 | — | — | ns | |
| TCKH | Clock High Pulse Width | 100 | — | — | ns | |
| TDS | Data in setup time before clock \downarrow | 100 | — | — | ns | |
| TDH | Data in hold time after clock \downarrow | 100 | — | — | ns | |
| T _{CO} | Clock \uparrow to data out valid (during a Read Data command) | 0 | — | 80 | ns | |
| T _{LZD} | Clock \downarrow to data low-impedance (during a Read Data command) | 0 | — | 80 | ns | |
| T _{HZD} | Clock \downarrow to data high-impedance (during a Read Data command) | 0 | — | 80 | ns | |
| TDLY | Data input not driven to next clock input (delay required between command/data or command/command) | 1.0 | — | — | μs | |
| TERAB | Bulk Erase cycle time | — | — | 5 | ms | |
| TERAR | Row Erase cycle time | — | — | 2.5 | ms | |

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

PIC12(L)F1612/16(L)F161X

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE (CONTINUED)

| AC/DC CHARACTERISTICS | | Standard Operating Conditions Production tested at 25°C | | | | |
|-----------------------|--|--|------|----------|----------|---------------------------------------|
| Sym. | Characteristics | Min. | Typ. | Max. | Units | Conditions/Comments |
| TPINT | Internally timed programming operation time | — | — | 2.5 5 | ms ms | Program memory Configuration Words |
| TPEXT | Externally timed programming pulse | 1.0 | — | 2.1 | ms | Note 1 |
| TDIS | Time delay from program to compare (HV discharge time) | 300 | — | — | μs | |
| TEXIT | Time delay when exiting Program/Verify mode | 1 | — | — | μs | |

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

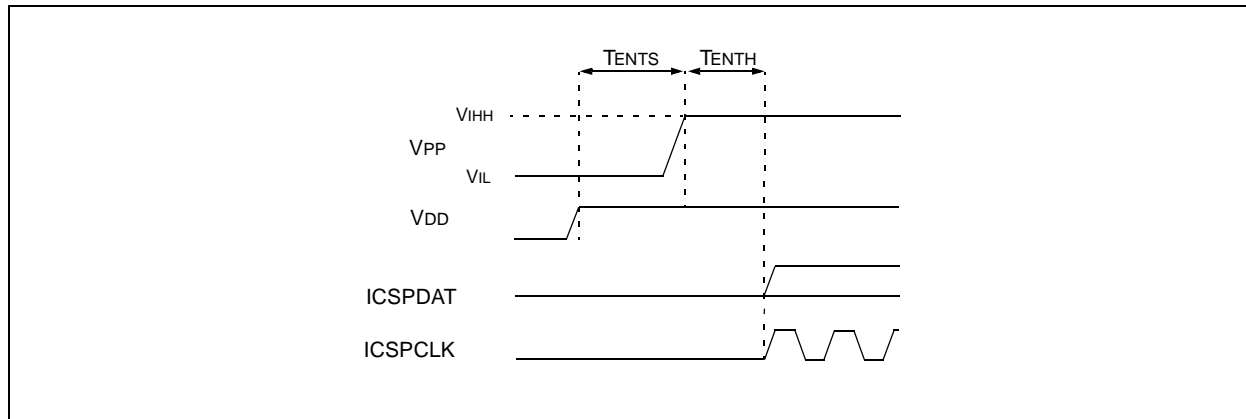
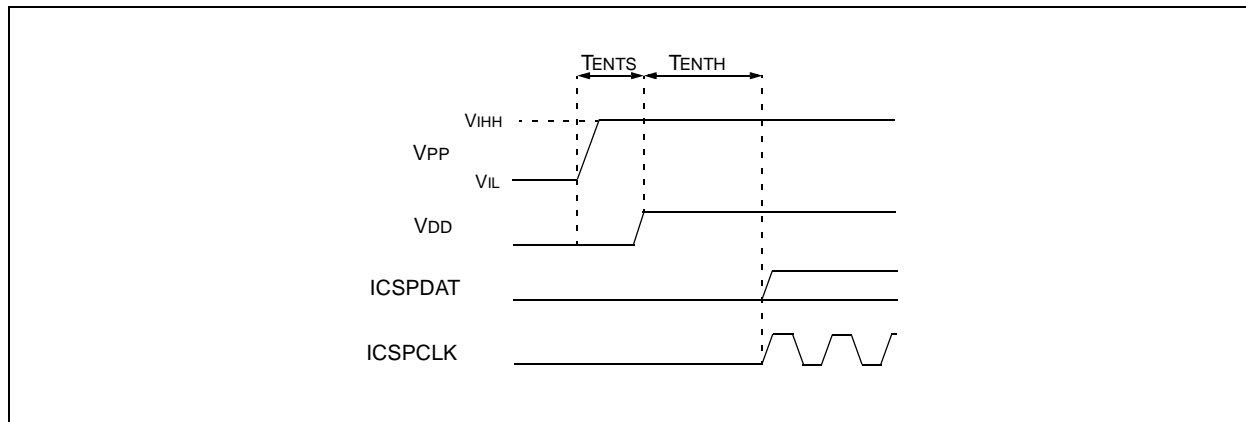


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST



PIC12(L)F1612/16(L)F161X

FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

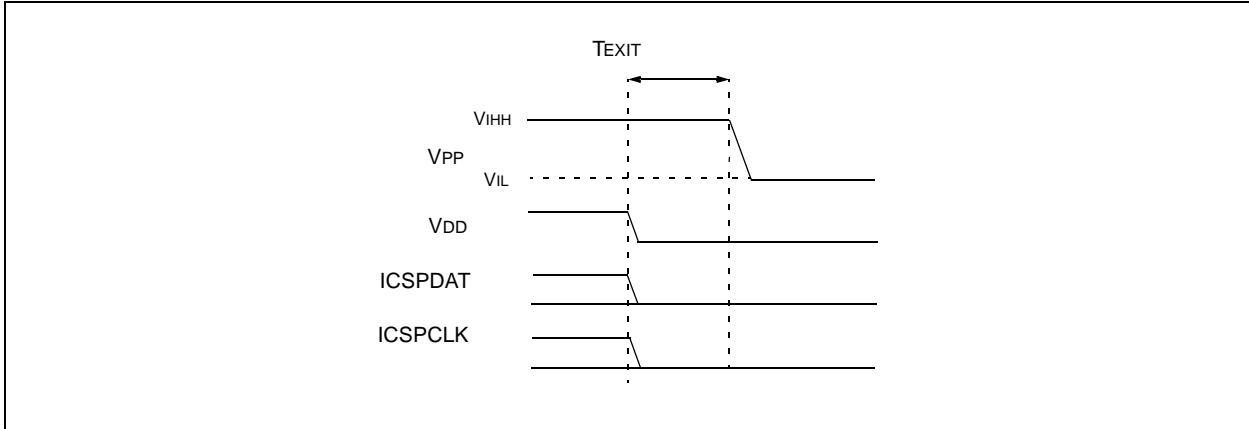
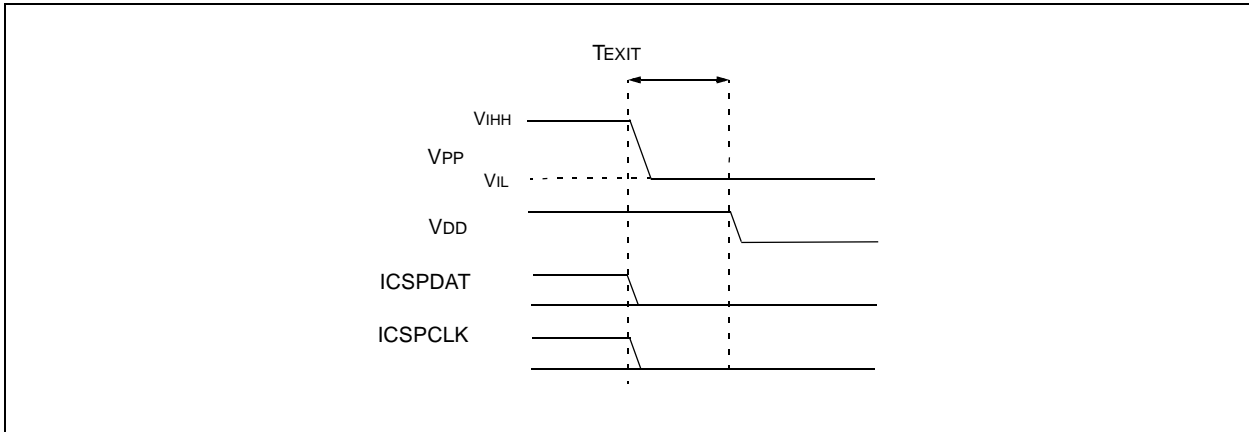


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST



PIC12(L)F1612/16(L)F161X

FIGURE 8-5: CLOCK AND DATA TIMING

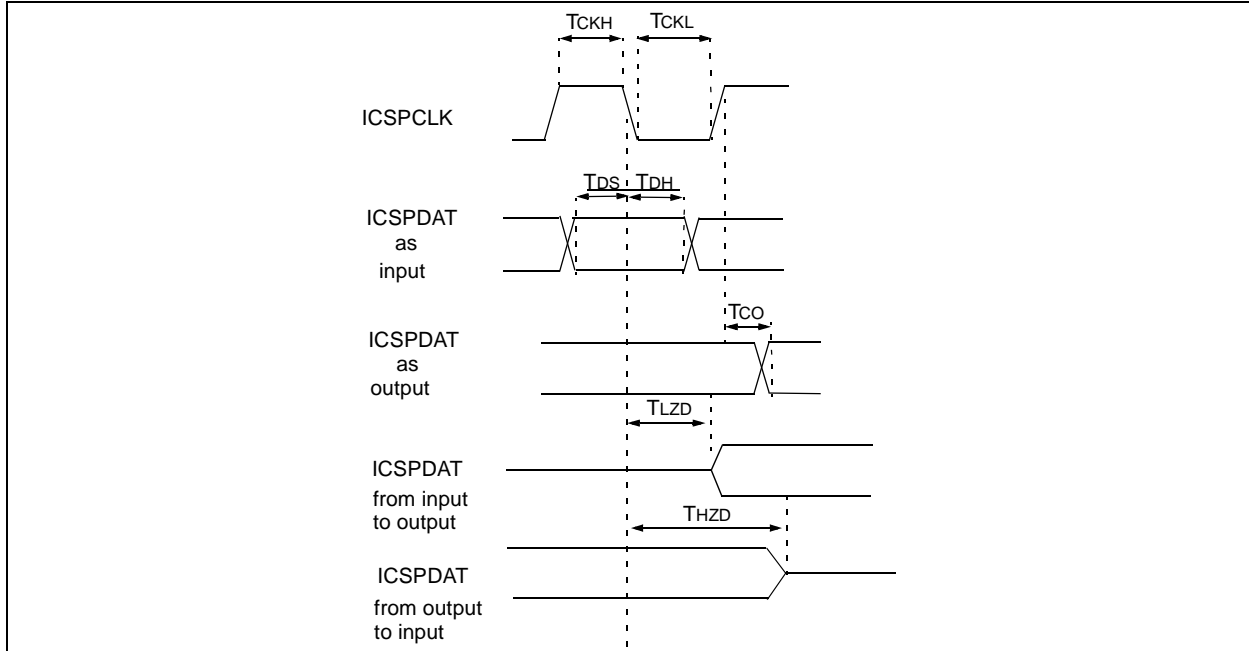


FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

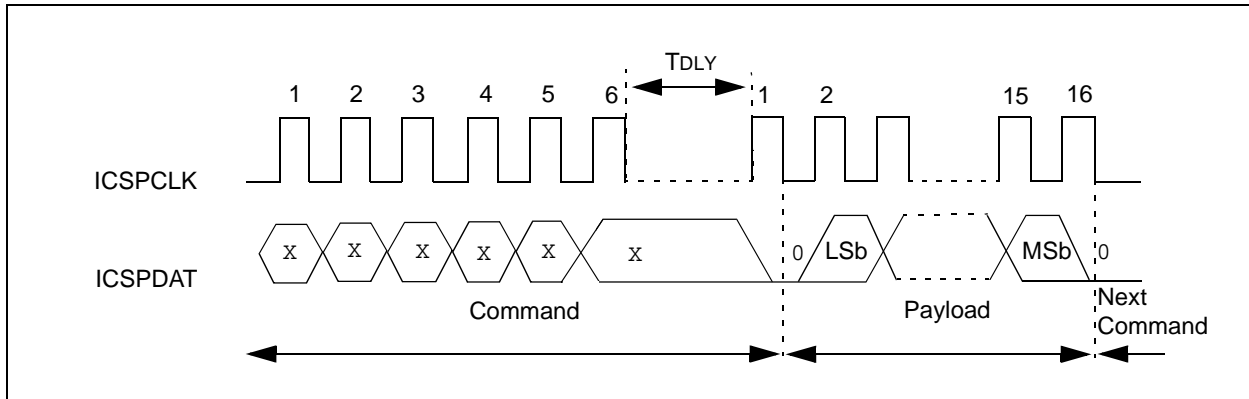
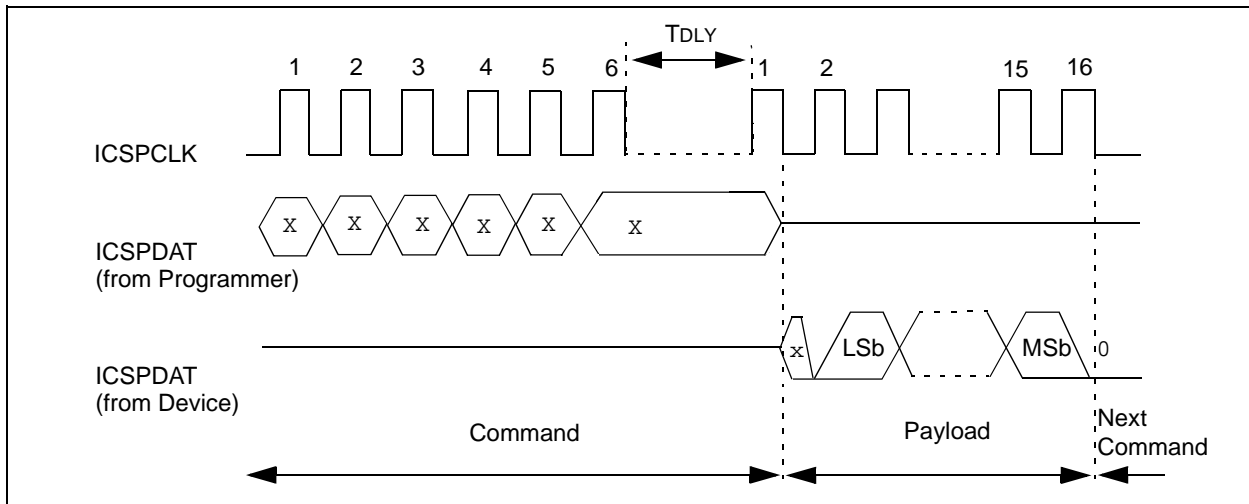


FIGURE 8-7: READ COMMAND-PAYLOAD TIMING



PIC12(L)F1612/16(L)F161X

FIGURE 8-8: LVP ENTRY (POWERED)

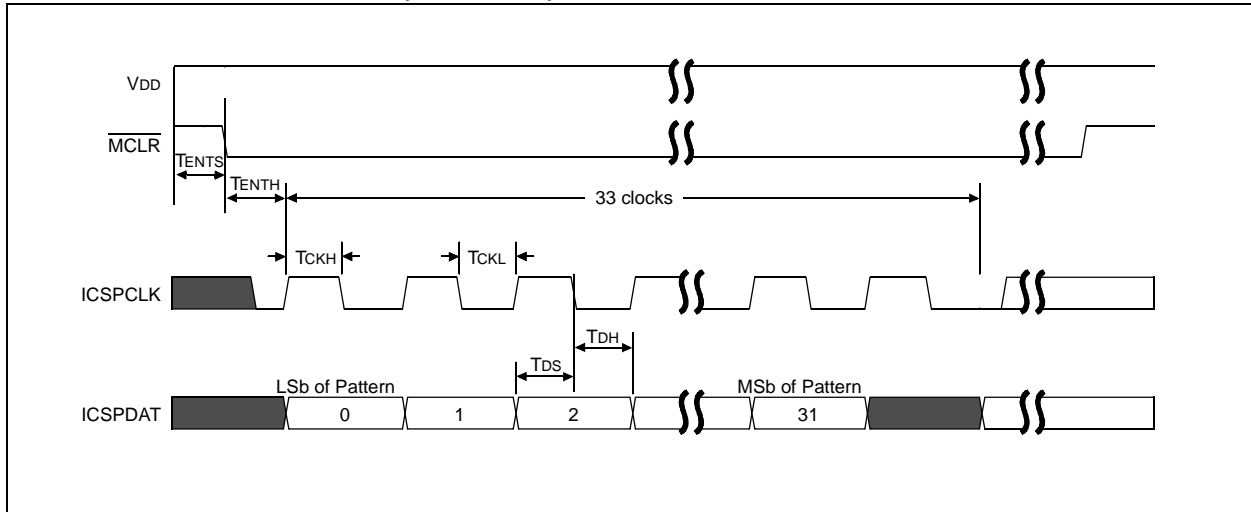
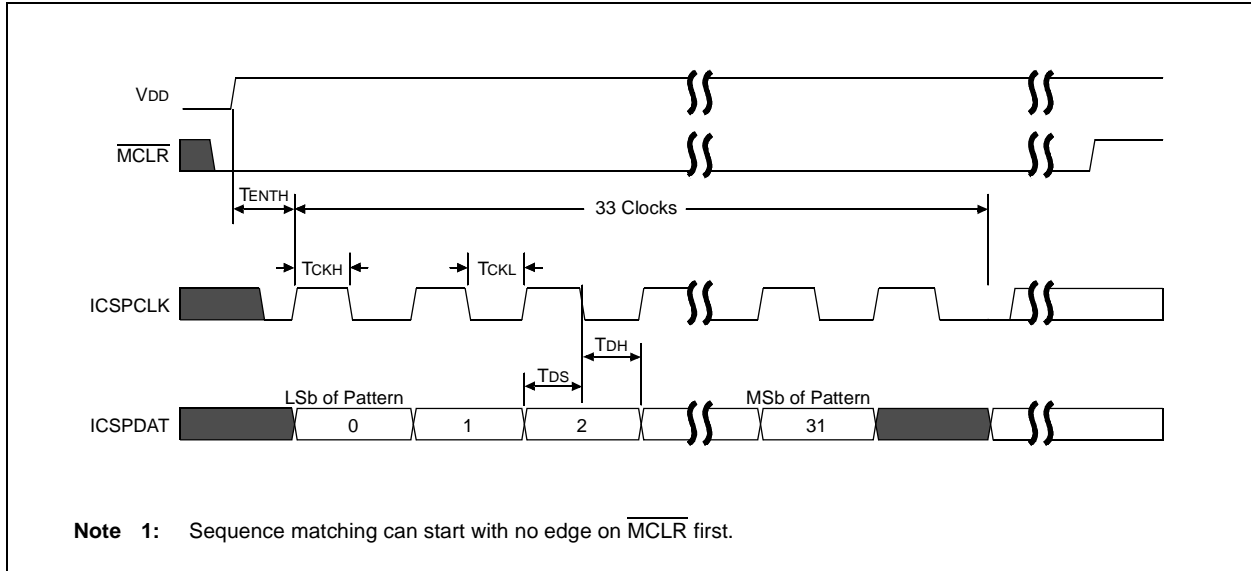


FIGURE 8-9: LVP ENTRY (POWERING UP)



PIC12(L)F1612/16(L)F161X

APPENDIX A: REVISION HISTORY

Revision A (09/2013)

Initial release of this document.

Revision B (04/2014)

Added PIC16(L)F1614/5/8/9 to the device family; Updated Figures 2-1 and 2-3; Added Figures 2-4 through 2-7, Figure 3-2 and Figure 3-3; Updated Registers 3-3 and 3-4; Updated Tables 3-1 and 4-2; Added Note to Section 4.1.3; Updated Section 7.3; Other minor corrections.

Revision C (08/2014)

Updated part number in Figure 2-2 (14-Pin PDIP, SOIC, TSSOP); Deleted Figure 2-4 (14-Pin PDIP, SOIC, TSSOP); Added Note 3 to Register 3-4; Updated Note 5 in Register 3-3; Updated Tables 7-1 and 7-2; Other minor corrections.

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