OPA462 High-Voltage (180-V), High-Current (30-mA) Operational Amplifier

1 Features

- Wide Power-Supply Range: ±6 V (12 V) to ±90 V (180 V)
- High-Output Load Drive: I_O ±30 mA
- Independent Output Disable or Shutdown
- Gain Bandwidth: 6.5 MHz
- Slew Rate: 25 V/µs
- Wide Temperature Range: –40°C to +85°C
- 8-Pin HSOIC (SO PowerPAD™) Package

2 Applications

- Memory and Semiconductor Test Equipment
- Optical Networking
- Piezo Drivers
- Transducer Drivers
- Servo Drivers
- Audio Amplifiers
- Avalanche Photodiode: High-V Current Sense
- High-Voltage Compliance Current Sources
- General High-Voltage Regulators and Power

3 Description

The OPA462 device is an operational amplifier with high voltage (180 V) and high current drive (30 mA). It is unity-gain stable and has a gain-bandwidth product of 6.5 MHz.

The OPA462 is internally protected against overtemperature conditions and current overloads. It is fully specified to perform over a wide power-supply range of ±6 V to ±90 V or on a single supply of 12 V to 180 V. The status flag is an open-drain output that allows it to be easily referenced to standard low-voltage logic circuitry. This high-voltage operational amplifier provides excellent accuracy, wide output swing, and is free from phase inversion problems that are often found in similar amplifiers.

The output can be independently disabled using the Enable/Disable (E/D) pin that has its own common return pin to allow easy interface to low-voltage logic circuitry. This disable is accomplished without disturbing the input signal path, not only saving power but also protecting the load.

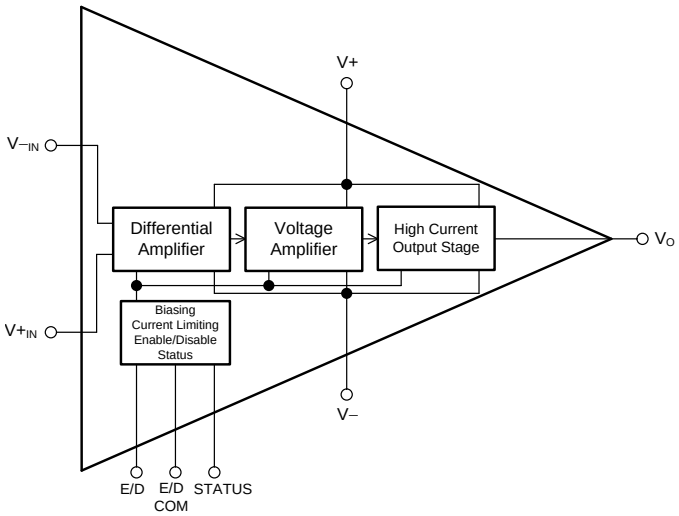
Featured in a small exposed-metal pad package, the OPA462 is easy to heat sink over the extended industrial temperature range, –40°C to +85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA462	HSOIC (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

OPA462 Block Diagram



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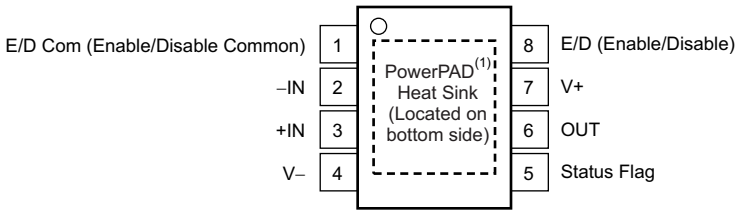
4 Revision History

DATE	REVISION	NOTES
December 2018	*	Initial release

5 Pin Configuration and Functions

DDA PACKAGE
8-Pin SO PowerPAD
Top View



(1) PowerPAD is internally connected to V–. Soldering the PowerPAD to a printed-circuit board (PCB) connected to V– is always required, even with applications that have low power dissipation.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
E/D (Enable/Disable)	8	I	Enable/Disable
E/D Com	1	I	Enable/Disable common
–IN	2	I	Inverting input
+IN	3	I	Noninverting input
OUT	6	O	Output
Status Flag	5	O	The Status Flag is an open-drain active-low output referenced to E/D Com. This pin goes active for either an overcurrent or overtemperature condition.
V–	4	—	Negative (lowest) power supply
V+	7	—	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		190	V
	Signal input pin(2)	(V–) – 0.3	(V+) + 0.3	V
	E/D to E/D Com		5.5	V
Current	All input pin(2)		±10	mA
	Output short circuit(3)	Continuous	Continuous	
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals, Status Flag, E/D, and E/D Com, and Output are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		Machine model (MM)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S	±6		±90	V
Specified temperature	–40		85	°C
Operating temperature, T_A	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA462 DDA (SO) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: V_S = ±90 V

At T_P (1) = 25°C, R_L = 10 kΩ to mid-supply, V_{CM} = V_{OUT} = mid-supply, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		I_O = 0 mA		±0.2	±4	mV
dV_{OS}/dT	Input offset voltage vs temperature		At T_A = –40°C to +85°C		±1.6	±10	µV/°C
PSRR	Input offset voltage vs power supply		V_S = ±6 V to ±90 V, V_{CM} = 0 V		5	10	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current		At T_P = 25°C		±1.4	±100	pA
I_{OS}	Input offset current				±0.2	±100	pA
NOISE							
e_n	Input voltage noise density		f = 1 kHz		35		nV/√Hz
			f = 10 kHz		23		nV/√Hz
	Input voltage noise		f = 0.01 Hz to 10 Hz		13		μV_{PP}
i_n	Current noise density		f = 1 kHz		500		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		Linear operation	(V–) + 1		(V+) – 3	V
CMRR	Common-mode rejection		V_S = ±90 V, –85 V ≤ V_{CM} ≤ 85 V	100	147		dB
			At T_A = –40°C to +85°C, V_S = ±90 V, –85 V ≤ V_{CM} ≤ 85 V	72	82		dB
INPUT IMPEDANCE							
	Differential				10^{13} || 6		Ω || pF
	Common-mode				10^{13} || 3.5		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 3 V < V_O < (V+) – 3 V, R_L = 10 kΩ, I_O = ±18 mA		110	130		dB
		(V–) + 3 V < V_O < (V+) – 3 V, R_L = 10 kΩ, I_O = ±18 mA	At T_A = –40°C to +85°C	90	115		dB
		(V–) + 5 V < V_O < (V+) – 5 V, R_L = 5 kΩ, I_O = ±36 mA		80	102		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product		Small-signal		6.5		MHz
SR	Slew rate		G = ±1, V_O = 80-V step, R_L = 3.27 kΩ		25		V/µs
	Full-power bandwidth				20		kHz
t_S	Settling time		To ±0.01%, G = ±5 or ±10, V_O = 120-V step		10		µs
THD+N	Total harmonic distortion + noise		G = +10, f = 1 kHz, V_O = 150 V_{PP}		0.0012		%
OUTPUT							
V_O	Voltage output swing from rail		R_L = 10 kΩ,	(V–) + 3		(V+) – 1.5	V
			R_L = 5 kΩ,	(V–) + 5		(V+) – 3	V
I_O	Maximum peak current output, current limit (2)				+/-30		mA
			At T_A = –40°C to +85°C		+/-20		mA
C_{LOAD}	Capacitive load drive				200		pF
R_O	Open-loop output impedance		f = 1 MHz		72		Ω

(1) T_P is the temperature of the leadframe die pad (exposed thermal pad) of the PowerPAD package.
(2) Measured using low-frequency (<10 Hz) ±98-V square wave.

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Electrical Characteristics: V_S = ±90 V (continued)

At T_P (1) = 25°C, R_L = 10 kΩ to mid-supply, V_{CM} = V_{OUT} = mid-supply, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output disabled	Output capacitance			18		pF
		Feedthrough capacitance			150		fF
STATUS FLAG PIN (Referenced to E/D Com)							
	Status Flag delay		Enable → Disable		6		µs
			Disable → Enable		4		µs
			Overcurrent delay		15		µs
			Overcurrent recovery delay		10		µs
T_J	Junction temperature	Alarm (Status Flag high)			150		°C
		Return to normal operation (Status Flag low)			130		°C
	Status Flag Output voltage		Normal operation			E/D Com + 2	V
			R_L = 100 Ω during thermal overdrive, alarm	(V+) – 2.5			V
E/D (ENABLE/DISABLE) PIN							
	E/D pin, referenced to E/D Com pin (3)						
V_{SD}	High (output enabled)		Pin open or forced high	E/D Com + 2.5		E/D Com + 5	V
	Low (output disabled)		Pin forced low	E/D Com	E/D Com + 0.65	E/D Com + 0.65	V
	Output disable time				4		µs
	Output enable time				3		µs
E/D COM PIN							
	Voltage range			(V–)		(V-) +100	V
POWER SUPPLY							
I_Q	Quiescent current		I_O = 0 mA		3.2	4	mA
	Quiescent current in Shutdown mode		I_O = 0 mA, $V_{E/D}$ = 0.65 V		1	2	mA

(3) High enables the outputs.

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6.6 Typical Characteristics

At T_P = 25°C, V_S = ±90 V, and R_L = 10 kΩ connected to GND, output enabled unless otherwise noted.

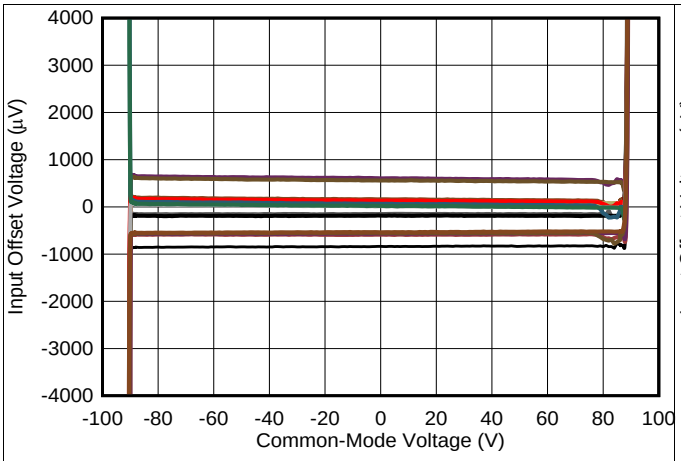

Figure 1. Input Offset Voltage vs Input Common-Mode Voltage

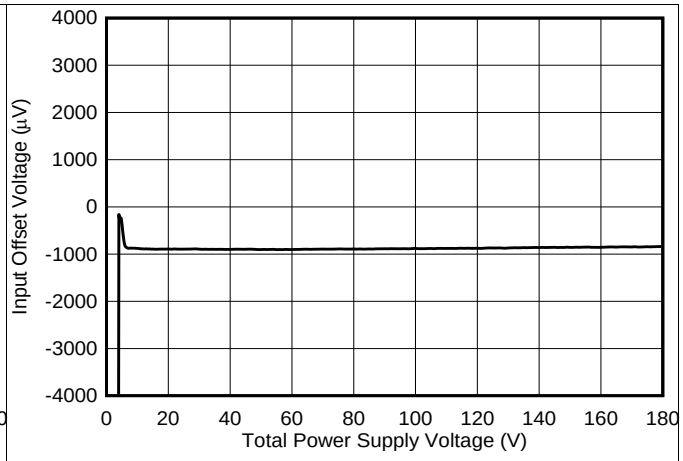

Figure 2. Input Offset Voltage vs Total Power Supply Voltage

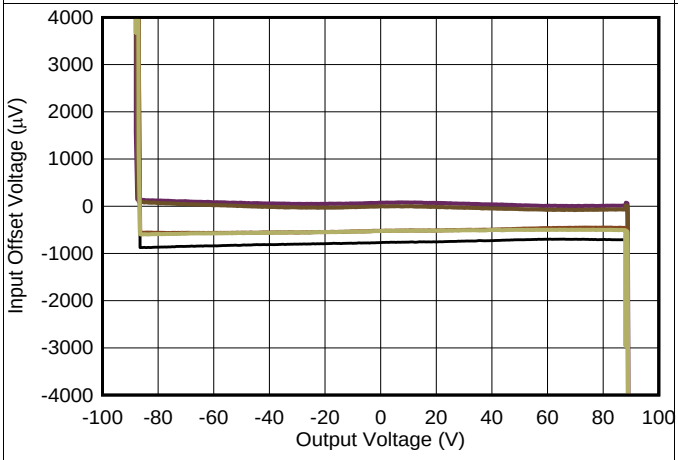

Figure 3. Input Offset Voltage vs Output Voltage

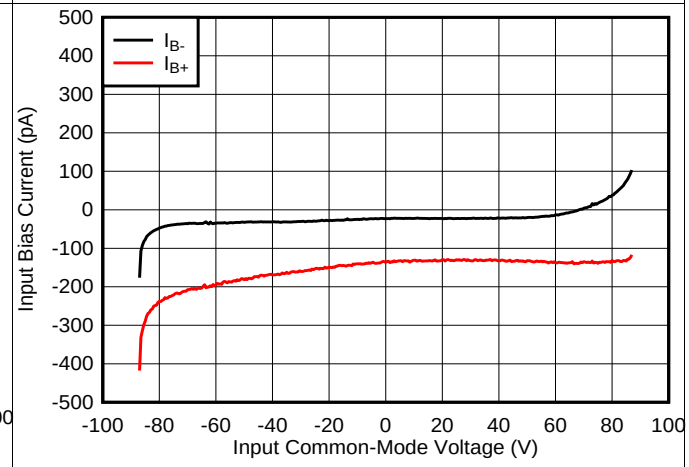

Figure 4. Input Bias Current vs Input Common-Mode Voltage

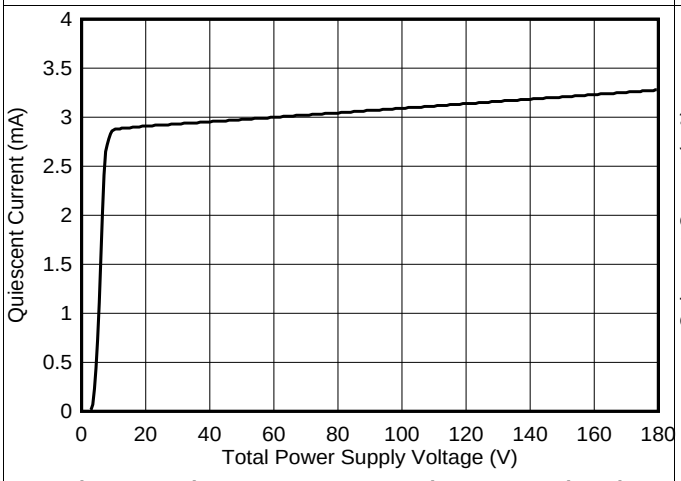

Figure 5. Quiescent Current vs Total Power Supply Voltage

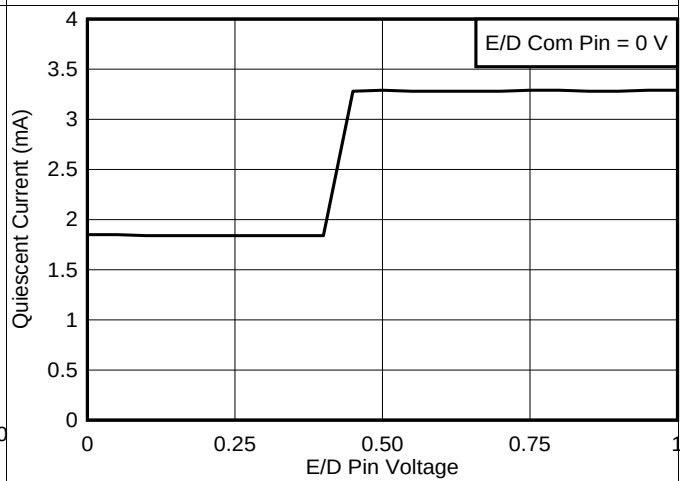

Figure 6. Quiescent Current vs Enable/Disable Voltage

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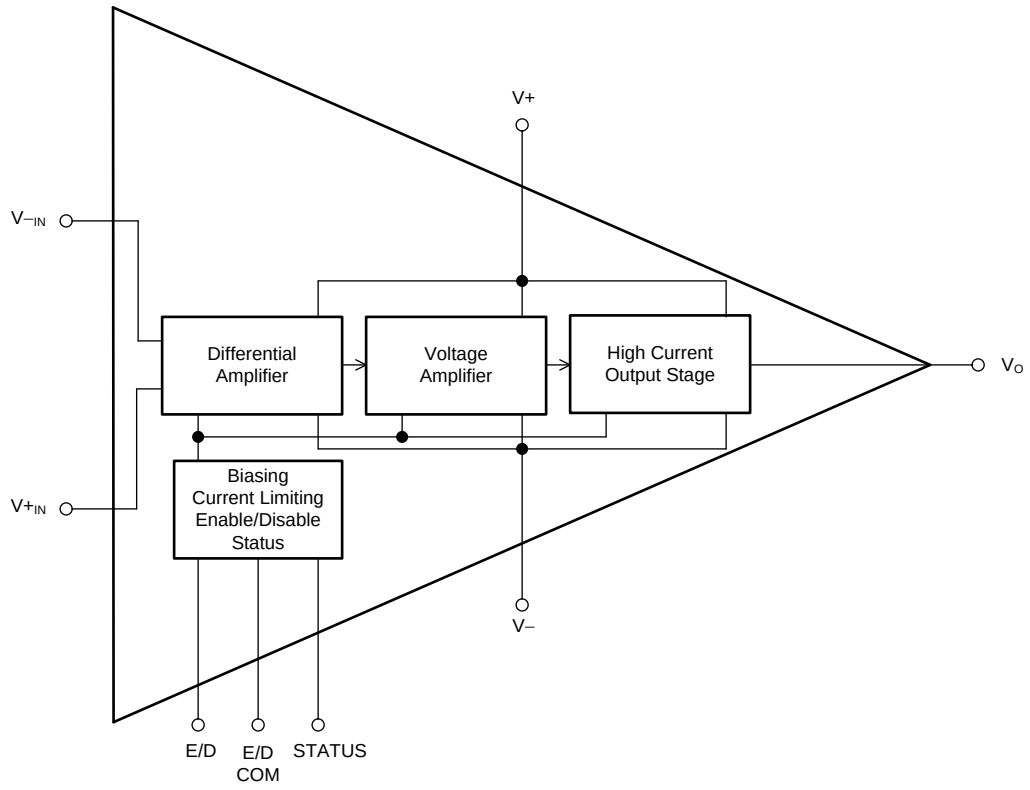
7 Detailed Description

7.1 Overview

The OPA462 is an operational amplifier (op amp) with high voltage (180 V) and a high current drive of 30 mA. This device is unity-gain stable and features a gain-bandwidth product of 6.5 MHz. The high-voltage OPA462 offers excellent accuracy, wide output swing, and has no phase inversion problems that are typically found in similar op amps. The device can be used in virtually any ±6-V to ±90-V op amp configuration.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA462 includes safety features on both the device input and output. On the input, protection is provided for a variety of fault conditions. The OPA462 is specified to give linear operation with input swing to within 1 V of the negative supply rail and 3 V of the positive supply rail. On the output, current limiting and thermal protection are provided. The OPA462 output is specified to swing within 3 V of the negative supply rail and 1.5 V of the positive supply rail with a 10-kΩ load while maintaining excellent linearity. Swing to the rail decreases with increasing output current. The OPA462 can swing to within 5 V of the negative rail and 3 V of the positive rail with a 5-kΩ load. The Enable/Disable function provides the ability to turn off the output stage and reduce power consumption when not being used. The Status Flag indicates fault conditions and can be used in conjunction with the Enable/Disable function to implement fault control loops.

7.3.1 ENABLE and E/D Com

If left disconnected, E/D Com is pulled near V– (negative supply) by an internal 10-μA current source. When left floating, ENABLE is held approximately 2 V above E/D Com by an internal 1-μA source. Even though active operation of the OPA462 results when the ENABLE and E/D Com pins are not connected, a moderately fast, negative-going signal capacitively coupled to the ENABLE pin can overpower the 1-μA pullup current and cause device shutdown. This behavior can appear as an oscillation and is encountered first near extreme cold

Feature Description (continued)

temperatures. If the enable function is not used, a conservative approach is to connect ENABLE through a 30-pF capacitor to a low impedance source. Another alternative is the connection of an external current source from V+ (positive supply) sufficient to hold the enable level above the shutdown threshold. Figure 7 shows a circuit that connects ENABLE and E/D Com. E/D Com is limited to (V-) + 100 V to enable the use of digital ground in a application where the OPA462 power supply is ± 90 V.

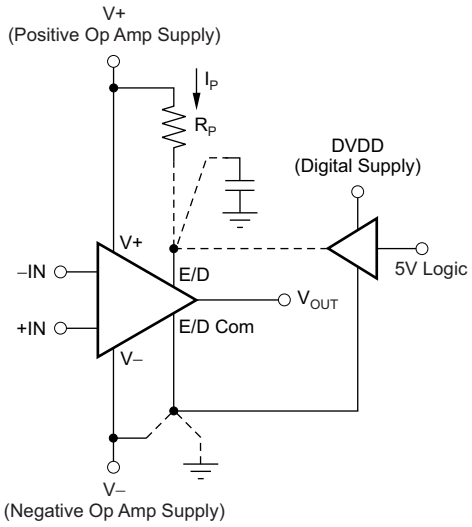


Figure 7. ENABLE and E/D Com

7.3.2 Current Limit

Current limiting is accomplished by internally limiting the drive to the output transistors. The output can supply the limited current continuously, unless the die temperature rises to 150°C, which initiates thermal shutdown. With adequate heatsinking, and use of the lowest possible supply voltage, the OPA462 can remain in current limit continuously without entering thermal shutdown. It is always best to provide proper heatsinking (either by a physical plate or by airflow) to remain considerably below the thermal shutdown threshold. For longest operational life of the device, keep the junction temperature below 125°C.

7.4 Device Functional Modes

A unique mode of the OPA462 is the output disable capability. This function conserves power during idle periods (quiescent current drops to approximately 1 mA). This disable is accomplished without disturbing the input signal path, not only saving power but also protecting the load. This feature makes disable useful for implementing external fault shutdown loops.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA462 is a high-voltage, high-current operational amplifier capable of operating with supply voltages as high as ±90 V (+180 V), or as low as ±6 V (+12 V). The high-voltage process and design of the OPA462 allows it to be used in applications where most operational amplifiers cannot be applied such as high-voltage power supply conditions, or when there is a need for very high-output voltage swing. The output is capable of delivering up to ±30 mA output current, or swinging within a few volts of the supply rails at moderate current levels. Additionally, the OPA462 features input overvoltage protection, output current limiting, thermal protection, a status flag and enable/disable capability.

8.2 Typical Application

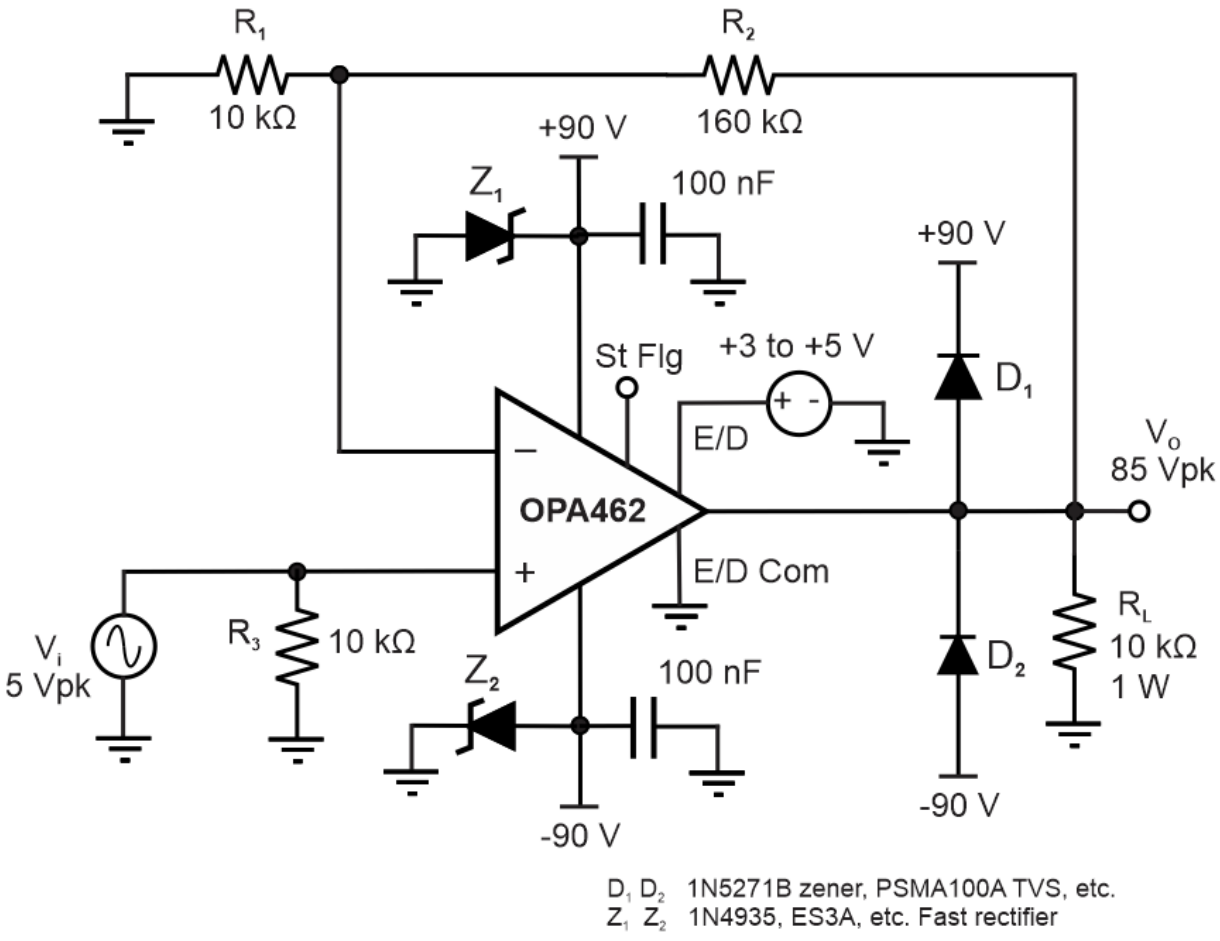

Figure 8. OPA462, High-voltage Non-Inverting amplifier, A_V = 17 V/V

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Typical Application (continued)

8.2.1 Design Requirements

The OPA462 high-voltage op amp can be used in commonly applied op amp circuits, but with the added capability of allowing the use much higher supply voltages. A very common application of an op amp is that of a non-inverting amplifier, one having a gain of 1 V/V or higher. Figure 8 shows the OPA462 in a non-inverting configuration.

The design goals for this circuit are:

- A noninverting gain of 17 V/V (24.6 dB)
- A peak output voltage approaching 85 V, while driving a 10 kΩ output load
- Correct biasing of the Enable/Disable (E/D) and E/D Com
- Protection against back electromagnetic force (EMF)

8.2.2 Detailed Design Procedure

Figure 8 shows a non-inverting circuit with a moderately high closed-loop gain (A_V) of 17 V/V (24.6 dB). In this example, a 5-V_{pp} ac signal is amplified to 85-V_{pp} across a 10-kΩ load resistor connected to its output. The peak current for this application is 8.5 mA, which is well within the OPA462 output current capability. Higher output current, typically up to 30 mA, may be attained at the expense of the output swing to the supply rails. A ±90-V_{DC} power supply is required for this configuration.

The non-inverting amplifier circuit shows the OPA462 enable/disable (E/D) function. When placed in disabled mode the op amp becomes non-functional, and the current consumption is reduced to about one-third to one-half the enabled level. An enable active state occurs when the E/D pin left open, or is biased 3 to 5 V above the E/D Com voltage level. If biased between the E/D com level, to E/D Com + 0.65 V, the OPA462 disables. More information about this function is provided in the *ENABLE and E/D Com* section.

Op amps designed for high-voltage and high-power applications may encounter output loads that can be quite different than those used in low-voltage, non-power op amp applications. Although every effort is made to make a high-voltage op amp such as the OPA462 robust and tolerant of different supply and different output load conditions, some loads can present potentially harmful circumstances.

Purely resistive output loads operating within the current capability range of the OPA462 should not present an unsafe condition provided the thermal requirements discussed in the *Layout* section. Complex loads that have inductive or capacitive reactive elements might, and need to be fully considered and addressed before implementation.

A potentially destructive mechanism is the back EMF transient that can be generated when driving an inductive load. D_1, D_2, Z_1 and Z_2 in Figure 8 have been added to the basic OPA462 amplifier circuit to provide protection against back EMF. If the voltage at the OPA462 output attempts to momentarily rise above V+, D_1 becomes forward biased and clamps the voltage between the output and V+ pins. It must be sufficient to protect the OPA462 output transistor. If the event causes the V+ voltage to rise the power supply bypass capacitor and/or Z_1, a Zener diode or a transient voltage suppressor (TVS) can provide a path for the transient current to ground. D_2 and Z_2 provide the same protection in the negative supply circuit.

The OPA462 non-inverting amplifier circuit having a closed-loop gain of 17 V/V has a small signal band –3 dB bandwidth of nearly 800-kHz. However, more importantly the large signal bandwidth is likely of greater importance in a high output voltage application. For that mode of operation the slew rate of the op amp and the peak output swing voltage must be considered on order to determine the maximum large signal bandwidth. The slew rate (SR) of the OPA462 is typically 6.5 V/µs, or 6.5 × 10^6 V/s. Using the 85-V_{PK} output voltage available from the circuit in Figure 8, the maximum large signal bandwidth can be calculated from the slew rate formula. Equation 1, Equation 2 and Equation 3 show the calculation process.

$$SR = 2\Pi \times f_{MAX} \times V_{PK} \quad (1)$$

$$f_{MAX} = SR / \left(2\Pi \times V_{PK}\right) \quad (2)$$

$$f_{MAX} = 6.5 \times 10^6 \text{ V/s} / \left(2\Pi / 85 \text{ V}\right) = 12 \text{ kHz}$$

where

- SR = 6.5 × 10^6 V/s
- V_{PK} = 85 V (3)

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Typical Application (continued)

It is always best for a typical parameter such as slew rate to allow for variance. In this example, keeping the large signal f_{MAX} to 10 kHz should be sufficient to assure the output stays away from slew rate limiting.

8.2.3 Application Curve

Figure 9 shows the OPA462 85-V_{PK} output produced from a 5-V_{PK}, 10-kHz sine input. The results were obtained from a TINA-TI simulation.

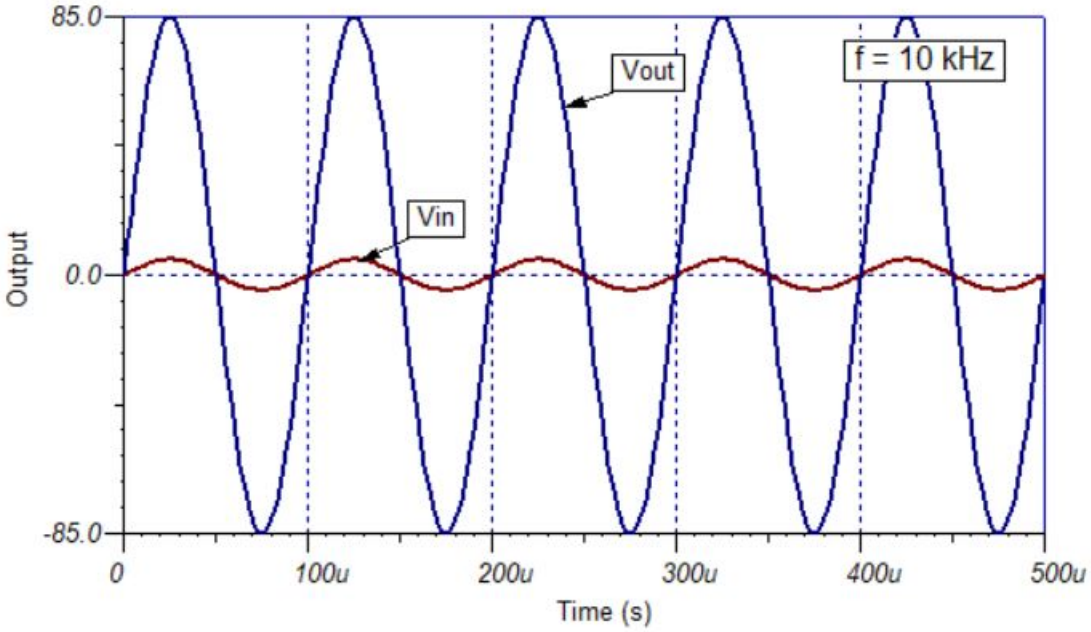

Figure 9. OPA462 Large Signal Output with a 10 kHz sine input from TINA-TI Simulation

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9 Power Supply Recommendations

The OPA462 may be operated from power supplies up to ±90 V or a total of 180 V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Parameters that vary significantly with operating voltage are shown in *Typical Characteristics*.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA462 can operate with as little as 12 V between the supplies and with up to 180 V between the supplies.

10 Layout

10.1 Layout Guidelines

10.1.1 Thermally-Enhanced PowerPAD Package

The OPA462 comes in an 8-pin SO with PowerPAD version that provides an extremely low thermal resistance $R_{\theta JC(bot)}$ path between the die and the exterior of the package. This package features an exposed thermal pad. This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The OPA462 SO-8 PowerPAD is a standard-size SO-8 package constructed using a downset leadframe upon which the die is mounted, as Figure 10 shows. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB. This architecture enhances the OPA462 power dissipation capability significantly, eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages, and allows the OPA462 to be easily mounted using standard PCB assembly techniques.

NOTE

Because the SO-8 PowerPAD is pin-compatible with standard SO-8 packages, the OPA462 is a drop-in replacement for operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB V– plane is always required, even with applications that have low power dissipation. Soldering the device to the PCB provides the necessary thermal, mechanical and electrical connection between the leadframe die pad and the PCB.

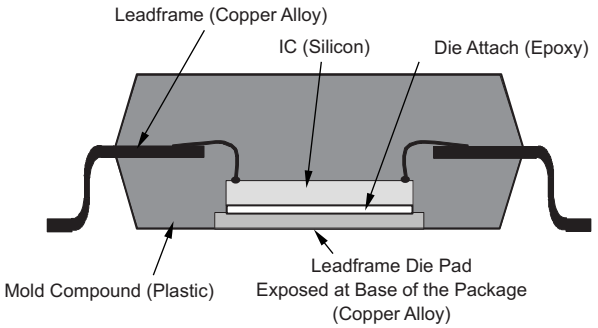

Figure 10. Cross-Section View of a PowerPAD Package

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Layout Guidelines (continued)

10.1.2 PowerPAD Layout Guidelines

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. The PowerPAD must be connected to the most negative supply voltage on the device, V–.
2. Prepare the PCB with a top-side etch pattern. There must be etching for the leads as well as etch for the thermal pad.
3. Use of thermal vias improves heat dissipation, but are not required. The thermal pad can connect to the PCB using an area equal to the pad size with no vias, but externally connected to V–.
4. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package are shown in the thermal land pattern mechanical drawing appended at the end of this document. These holes must be 13 mils (.013 in, or 0.3302 mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
5. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA462 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all holes to the internal power plane of the correct voltage potential (V–).
7. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA462 PowerPAD package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask must leave the terminals of the package and the thermal pad area exposed. The bottom-side solder mask must cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
10. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see technical brief SLMA002, available for download at www.ti.com.

10.2 Layout Example

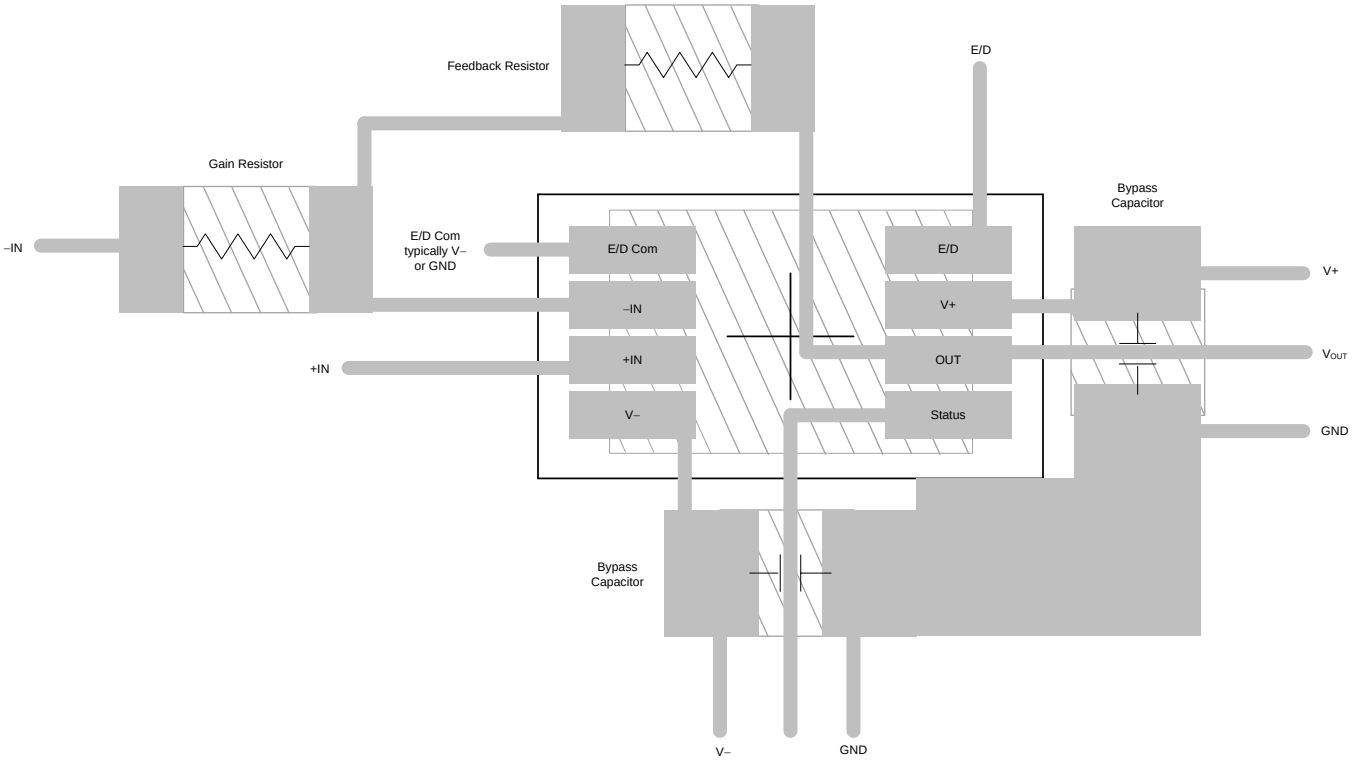

Figure 11. OPA462 Layout Example

10.3 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For DC signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S – V_O)$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower because the root-mean square (RMS) value determines heating. Application bulletin SBOA022 explains how to calculate or measure dissipation with unusual loads or signals.

The OPA462 can supply output currents of 25 mA and larger. Supplying this amount of current presents no problem for some op amps operating from ±15-V supplies. However, with high supply voltages, internal power dissipation of the op amp can be quite high. Operation from a single power supply (or unbalanced power supplies) can produce even greater power dissipation because a large voltage is impressed across the conducting output transistor. Applications with high power dissipation may require a heatsink or a heat spreader.

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPA462, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- Application bulletin AB-038: *Heat Sinking—TO-3 Thermal Model*, SBOA021
- Application bulletin AB-039: *Power Amplifier Stress and Power Handling Limitations*, SBOA022
- Application bulletin AB-045: *Op Amp Performance Analysis*, SBOA054
- Application bulletin AB-067: *Single-Supply Operation of Operational Amplifiers*, SBOA059
- Application bulletin AB-105: *Tuning in Amplifiers*, SBOA067.
- Technical brief: *PowerPAD Thermally-Enhanced Package*, SLMA002.

ADVANCE INFORMATION

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, TINA-TI, E2E are trademarks of Texas Instruments.
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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA462IDDA	PREVIEW	SO PowerPAD	DDA	8	75	TBD	Call TI	Call TI	-40 to 85		
OPA462IDDAR	PREVIEW	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	-40 to 85		
XOPA462IDDA	ACTIVE	SO PowerPAD	DDA	8	75	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

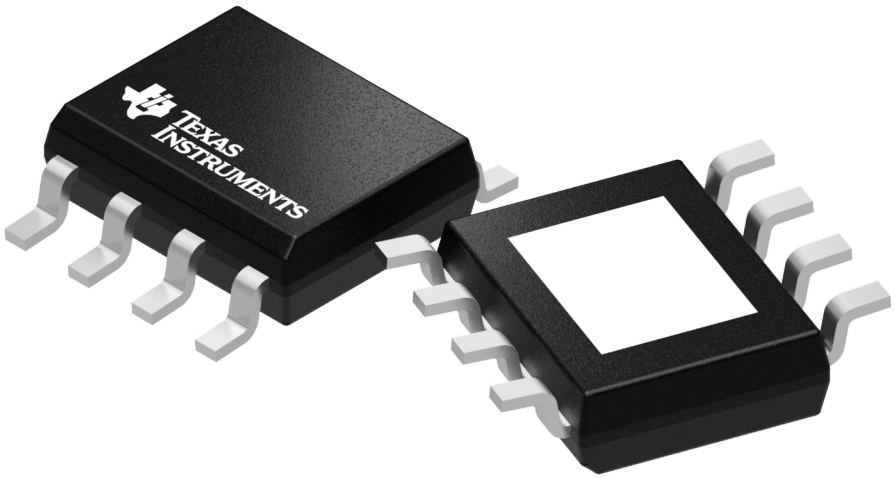
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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