

## OPAx354 250-MHz, Rail-to-Rail I/O, CMOS Operational Amplifiers

### 1 Features

- Unity-Gain Bandwidth: 250 MHz
- Wide Bandwidth: 100-MHz GBW
- High Slew Rate: 150 V/ $\mu$ s
- Low Noise: 6.5 nV $\sqrt{\text{Hz}}$
- Rail-to-Rail I/O
- High Output Current: > 100 mA
- Excellent Video Performance:
  - Diff Gain: 0.02%, Diff Phase: 0.09°
  - 0.1-dB Gain Flatness: 40 MHz
- Low Input Bias Current: 3 pA
- Quiescent Current: 4.9 mA
- Thermal Shutdown
- Supply Range: 2.5 V to 5.5 V
- *MicroSIZE* and PowerPAD™ Packages

### 2 Applications

- Video Processing
- Ultrasound
- Optical Networking, Tunable Lasers
- Photodiode Transimpedance Amps
- Active Filters
- High-Speed Integrators
- Analog-to-Digital (A/D) Converter Input Buffers
- Digital-to-Analog (D/A) Converter Output Amplifiers
- Barcode Scanners
- Communications

### 3 Description

The OPA354 series of high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. They are unity-gain stable and can drive large output currents. Differential gain is 0.02% and differential phase is 0.09°. Quiescent current is only 4.9 mA per channel.

The OPA354 series op amps are optimized for operation on single or dual supplies as low as 2.5 V ( $\pm 1.25$  V) and up to 5.5 V ( $\pm 2.75$  V). Common-mode input range extends beyond the supplies. The output swing is within 100 mV of the rails, supporting wide dynamic range.

For applications requiring the full 100-mA continuous output current, single and dual 8-pin HSOP PowerPAD versions are available.

The single version (OPA354) is available in the tiny 5-pin SOT-23 and 8-pin HSOP PowerPAD packages. The dual version (OPA2354) comes in the miniature 8-pin VSSOP and 8-pin HSOP PowerPAD packages. The quad version (OPA4354) is offered in 14-pin TSSOP and 14-pin SOIC packages.

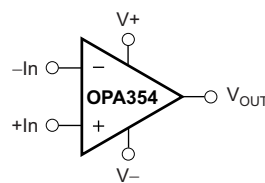
Multichannel version feature completely independent circuitry for lowest crosstalk and freedom from interaction. All are specified over the extended  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  temperature range.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA354	HSOP (8)	4.89 mm x 3.90 mm
	SOT-23 (5)	2.90 mm x 1.60 mm
OPA2354	VSSOP (8)	3.00 mm x 3.00 mm
	HSOP (8)	4.89 mm x 3.90 mm
OPA4354	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



Copyright © 2016,  
Texas Instruments Incorporated



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>20</b>
<b>2 Applications</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>21</b>
<b>3 Description</b> .....	<b>1</b>	9.1 Application Information.....	<b>21</b>
<b>4 Revision History</b> .....	<b>2</b>	9.2 Typical Application .....	<b>21</b>
<b>5 Device Comparison Table</b> .....	<b>3</b>	<b>10 Power Supply Recommendations</b> .....	<b>23</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>11 Layout</b> .....	<b>23</b>
<b>7 Specifications</b> .....	<b>6</b>	11.1 Layout Guidelines .....	<b>23</b>
7.1 Absolute Maximum Ratings .....	<b>6</b>	11.2 Layout Example .....	<b>23</b>
7.2 ESD Ratings.....	<b>6</b>	11.3 Power Dissipation .....	<b>23</b>
7.3 Recommended Operating Conditions.....	<b>6</b>	11.4 PowerPAD Thermally-Enhanced Package .....	<b>24</b>
7.4 Thermal Information: OPA354 .....	<b>7</b>	11.5 PowerPAD Assembly Process.....	<b>24</b>
7.5 Thermal Information: OPA2354 .....	<b>7</b>	<b>12 Device and Documentation Support</b> .....	<b>26</b>
7.6 Thermal Information: OPA4354 .....	<b>7</b>	12.1 Documentation Support .....	<b>26</b>
7.7 Electrical Characteristics: $V_S = 2.7\text{ V to }5.5\text{ V Single-Supply}$ .....	<b>8</b>	12.2 Related Links .....	<b>26</b>
7.8 Typical Characteristics .....	<b>10</b>	12.3 Receiving Notification of Documentation Updates .....	<b>26</b>
<b>8 Detailed Description</b> .....	<b>15</b>	12.4 Community Resources.....	<b>26</b>
8.1 Overview .....	<b>15</b>	12.5 Trademarks .....	<b>26</b>
8.2 Functional Block Diagram .....	<b>15</b>	12.6 Electrostatic Discharge Caution.....	<b>26</b>
8.3 Feature Description.....	<b>16</b>	12.7 Glossary .....	<b>27</b>
		<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>27</b>

## 4 Revision History

### Changes from Revision E (March 2002) to Revision F

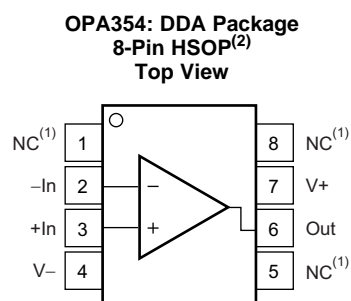
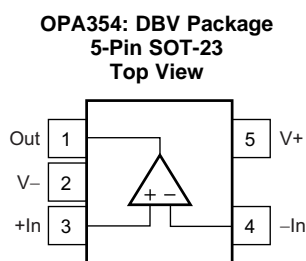
Page

• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Deleted <i>Package/Ordering Information</i> table, see POA at the end of the data sheet.....	<b>1</b>
• Renamed <i>OPAx354 Related Products</i> table to <i>Device Comparison Table</i> .....	<b>3</b>

## 5 Device Comparison Table

FEATURES	PRODUCT
Shutdown Version of OPA354 Family	<a href="#">OPAx357</a>
200-MHz GBW, Rail-to-Rail Output, CMOS, Shutdown	<a href="#">OPAx355</a>
200-MHz GBW, Rail-to-Rail Output, CMOS	<a href="#">OPAx356</a>
38-MHz GBW, Rail-to-Rail Input/Output, CMOS	<a href="#">OPAx350/OPAx353</a>
75-MHz BW G = 2, Rail-to-Rail Output	<a href="#">OPA2631</a>
150-MHz BW G = 2, Rail-to-Rail Output	<a href="#">OPA2634</a>
100-MHz BW, Differential Input/Output, 3.3-V Supply	<a href="#">THS412x</a>

## 6 Pin Configuration and Functions

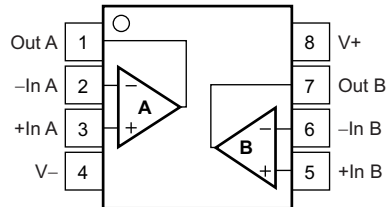


- (1) NC means no internal connection.  
PowerPAD must be connected to V- or left floating.

**Pin Functions: OPA354**

NAME	PIN		I/O	DESCRIPTION
	SOT-23	HSOP		
-In	4	2	I	Inverting input
+In	3	3	I	Noninverting input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
Out	1	6	O	Output
V-	2	4	—	Negative (lowest) supply
V+	5	7	—	Positive (highest) supply

**OPA2354: DGK and DDA Packages**  
**8-Pin VSSOP, HSOP<sup>(1)</sup>**  
**Top View**

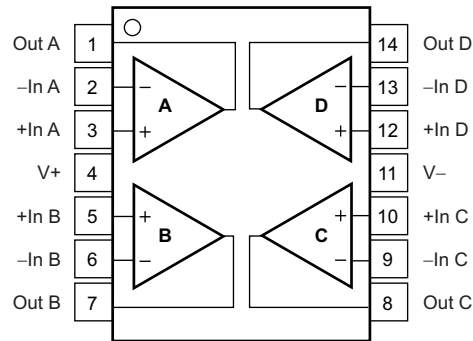


(1) PowerPAD must be connected to V- or left floating.

**Pin Functions: OPA2354**

NAME	PIN		I/O	DESCRIPTION
	VSSOP	HSOP		
-In A	2	2	I	Inverting input, channel A
+In A	3	3	I	Noninverting input, channel A
-In B	6	6	I	Inverting input, channel B
+In B	5	5	I	Noninverting input, channel B
Out A	1	1	O	Output, channel A
Out B	7	7	O	Output, channel B
V-	4	4	—	Negative (lowest) supply
V+	8	8	—	Positive (highest) supply

**OPA4354: D and PW Packages  
14-Pin SOIC, TSSOP  
Top View**



**Pin Functions: OPA4354**

NAME	PIN		I/O	DESCRIPTION
	SOIC	TSSOP		
-In A	2	2	I	Inverting input, channel A
+In A	3	3	I	Noninverting input, channel A
-In B	6	6	I	Inverting input, channel B
+In B	5	5	I	Noninverting input, channel B
-In C	9	9	I	Inverting input, channel C
+In C	10	10	I	Noninverting input, channel C
-In D	13	13	I	Inverting input, channel D
+In D	12	12	I	Noninverting input, channel D
Out A	1	1	O	Output, channel A
Out B	7	7	O	Output, channel B
Out C	8	8	O	Output, channel C
Out D	14	14	O	Output, channel D
V-	11	11	—	Negative (lowest) supply
V+	4	4	—	Positive (highest) supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V–	7.5		V
	Signal input terminals <sup>(2)</sup>	(V–) – (0.5)	(V+) + 0.5	
Current	Signal input terminals <sup>(2)</sup>	–10	10	mA
	Output short circuit <sup>(3)</sup>	Continuous		
Temperature	Operating, T <sub>A</sub>	–55	150	°C
	Junction, T <sub>J</sub>	150		
	Storage, T <sub>stg</sub>	–65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage, V– to V+	2.5	5.5	V
	Specified temperature	–40	125	°C

## 7.4 Thermal Information: OPA354

THERMAL METRIC <sup>(1)</sup>		OPA354		UNIT
		DBV (SOT-23)	DDA (HSOP)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.3	42.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.3	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	26.5	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	3.8	8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	42.3	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Thermal Information: OPA2354

THERMAL METRIC <sup>(1)</sup>		OPA2354		UNIT
		DDA (HSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	175.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	97.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	5.6	9.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	20.6	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Thermal Information: OPA4354

THERMAL METRIC <sup>(1)</sup>		OPA4354		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	33.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	11.6	1.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	37.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Electrical Characteristics: $V_S = 2.7\text{ V to }5.5\text{ V}$ Single-Supply

 At  $T_A = 25^\circ\text{C}$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V}$ , at $T_A = 25^\circ\text{C}$		$\pm 2$	$\pm 8$	mV
		$V_S = 5\text{ V}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$			$\pm 10$	
$dV_{OS}/dT$	Input offset voltage vs temperature	$V_S = 5\text{ V}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$		$\pm 4$		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage vs power supply	$V_S = 2.7\text{ V to }5.5\text{ V}$ , $V_{CM} = (V_S/2) - 0.55\text{ V}$		$\pm 200$	$\pm 800$	$\mu\text{V}/\text{V}$
		$V_S = 2.7\text{ V to }5.5\text{ V}$ , $V_{CM} = (V_S/2) - 0.55\text{ V}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$			$\pm 900$	
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			3	$\pm 50$	pA
$I_{OS}$	Input offset current			$\pm 1$	$\pm 50$	pA
<b>NOISE</b>						
$e_n$	Input voltage noise density	$f = 1\text{ MHz}$		6.5		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Current noise density	$f = 1\text{ MHz}$		50		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage		$(V_-) - 0.1$		$(V_+) + 0.1$	V
CMRR	Common-mode rejection ratio	$V_S = 5.5\text{ V}$ , $-0.1\text{ V} < V_{CM} < 3.5\text{ V}$ , at $T_A = 25^\circ\text{C}$	66	80		dB
		$V_S = 5.5\text{ V}$ , $-0.1\text{ V} < V_{CM} < 3.5\text{ V}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$	64			
		$V_S = 5.5\text{ V}$ , $-0.1\text{ V} < V_{CM} < 5.6\text{ V}$ , at $T_A = 25^\circ\text{C}$	56	68		
		$V_S = 5.5\text{ V}$ , $-0.1\text{ V} < V_{CM} < 5.6\text{ V}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$	55			
<b>INPUT IMPEDANCE</b>						
	Differential			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
	Common-mode			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop gain	$V_S = 5.5\text{ V}$ , $0.3\text{ V} < V_O < 4.7\text{ V}$ , at $T_A = 25^\circ\text{C}$	94	110		dB
		$V_S = 5\text{ V}$ , $0.4\text{ V} < V_O < 4.6\text{ V}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$	90			
<b>FREQUENCY RESPONSE</b>						
$f_{-3\text{dB}}$	Small-signal bandwidth	At $G = +1$ , $V_O = 100\text{ mV}_{PP}$ , $R_F = 25\ \Omega$		250		MHz
		At $G = +2$ , $V_O = 100\text{ mV}_{PP}$		90		
GBW	Gain-bandwidth product	$G = +10$		100		MHz
$f_{0.1\text{dB}}$	Bandwidth for 0.1-dB gain flatness	At $G = +2$ , $V_O = 100\text{ mV}_{PP}$		40		MHz
SR	Slew rate	$V_S = 5\text{ V}$ , $G = +1$ , 4-V step		150		V/ $\mu\text{s}$
		$V_S = 5\text{ V}$ , $G = +1$ , 2-V step		130		
		$V_S = 3\text{ V}$ , $G = +1$ , 2-V step		110		
	Rise-and-fall time	At $G = +1$ , $V_O = 200\text{ mV}_{PP}$ , 10% to 90%		2		ns
		At $G = +1$ , $V_O = 2\text{ V}_{PP}$ , 10% to 90%		11		
	Settling time	0.1%, $V_S = 5\text{ V}$ , $G = +1$ , 2-V output step		30		ns
		0.01%, $V_S = 5\text{ V}$ , $G = +1$ , 2-V output step		60		
	Overload recovery time	$V_{IN} \times \text{Gain} = V_S$		5		ns



**Electrical Characteristics:  $V_S = 2.7\text{ V to }5.5\text{ V}$  Single-Supply (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FREQUENCY RESPONSE, continued</b>						
Harmonic distortion	Second harmonic	At $G = +1$ , $f = 1\ \text{MHz}$ , $V_O = 2\ V_{PP}$ , $R_L = 200\ \Omega$ , $V_{CM} = 1.5\ \text{V}$		-75		dBc
	Third harmonic	At $G = +1$ , $f = 1\ \text{MHz}$ , $V_O = 2\ V_{PP}$ , $R_L = 200\ \Omega$ , $V_{CM} = 1.5\ \text{V}$		-83		
Differential gain error		NTSC, $R_L = 150\ \Omega$		0.02%		
Differential phase error		NTSC, $R_L = 150\ \Omega$		0.09		°
Channel-to-channel crosstalk	OPA2354	$f = 5\ \text{MHz}$		-100		dB
	OPA4354			-84		
<b>OUTPUT</b>						
Voltage output swing from rail		$V_S = 5\ \text{V}$ , $R_L = 1\ \text{k}\Omega$ , $A_{OL} > 94\ \text{dB}$ , at $T_A = 25^\circ\text{C}$		0.1	0.3	V
		$V_S = 5\ \text{V}$ , $R_L = 1\ \text{k}\Omega$ , $A_{OL} > 90\ \text{dB}$ , at $T_A = -40^\circ\text{C to }125^\circ\text{C}$			0.4	
$I_O$	Output current, single, dual, quad <sup>(1)(2)</sup>	$V_S = 5\ \text{V}$	100			mA
		$V_S = 3\ \text{V}$		50		mA
Closed-loop output impedance		$f < 100\ \text{kHz}$		0.05		$\Omega$
$R_O$	Open-loop output resistance			35		$\Omega$
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage		2.7		5	V
	Operating voltage		2.5		5.5	
$I_Q$	Quiescent current (per amplifier)	At $T_A = 25^\circ\text{C}$ , $V_S = 5\ \text{V}$ , enabled, $I_O = 0$		4.9	6	mA
		At $T_A = -40^\circ\text{C to }125^\circ\text{C}$			7.5	
<b>THERMAL SHUTDOWN – JUNCTION TEMPERATURE</b>						
Shutdown				160		°C
Reset from shutdown				140		°C
<b>THERMAL RANGE</b>						
Specified			-40		125	°C
Operating			-55		150	°C
Storage			-65		150	°C

(1) See typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 20 and Figure 22).

(2) Specified by design.

## 7.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $G = +1$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.

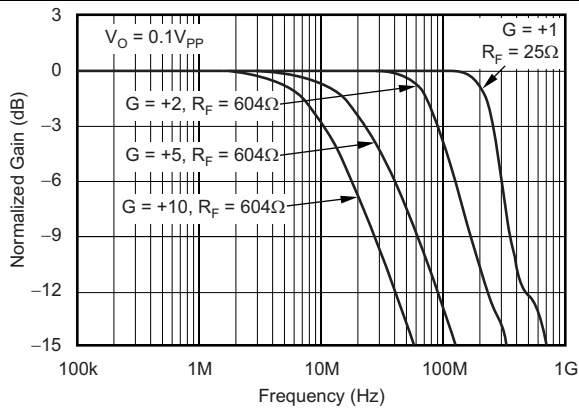


Figure 1. Noninverting Small-Signal Frequency Response

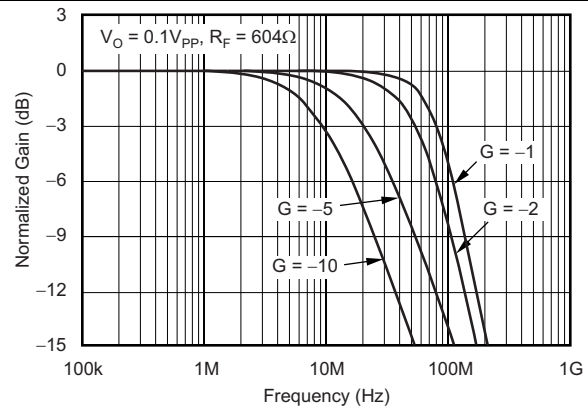


Figure 2. Inverting Small-Signal Frequency Response

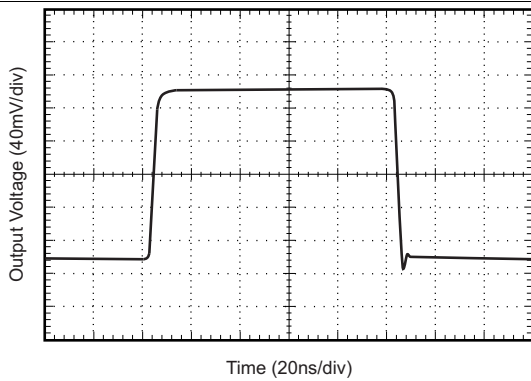


Figure 3. Noninverting Small-Signal Step Response

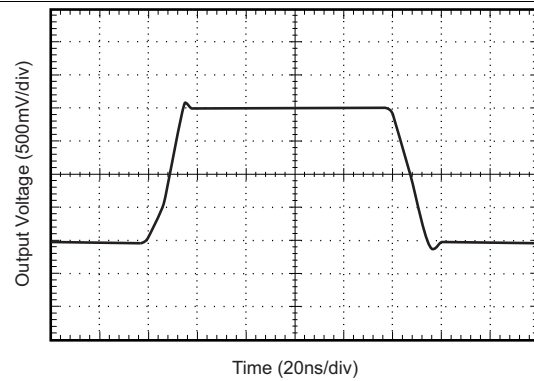


Figure 4. Noninverting Large-Signal Step Response

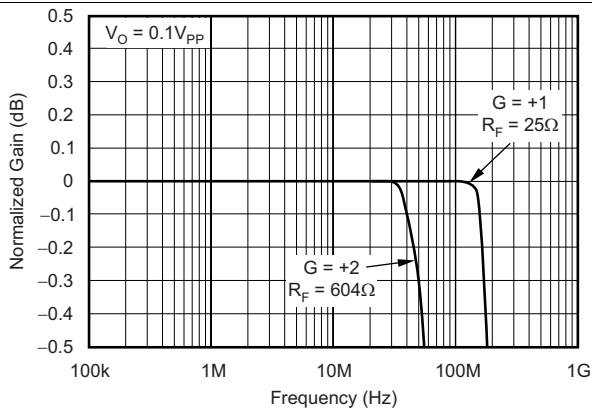


Figure 5. 0.1-dB Gain Flatness

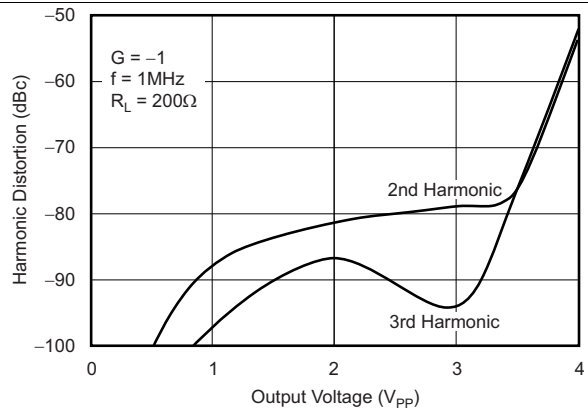
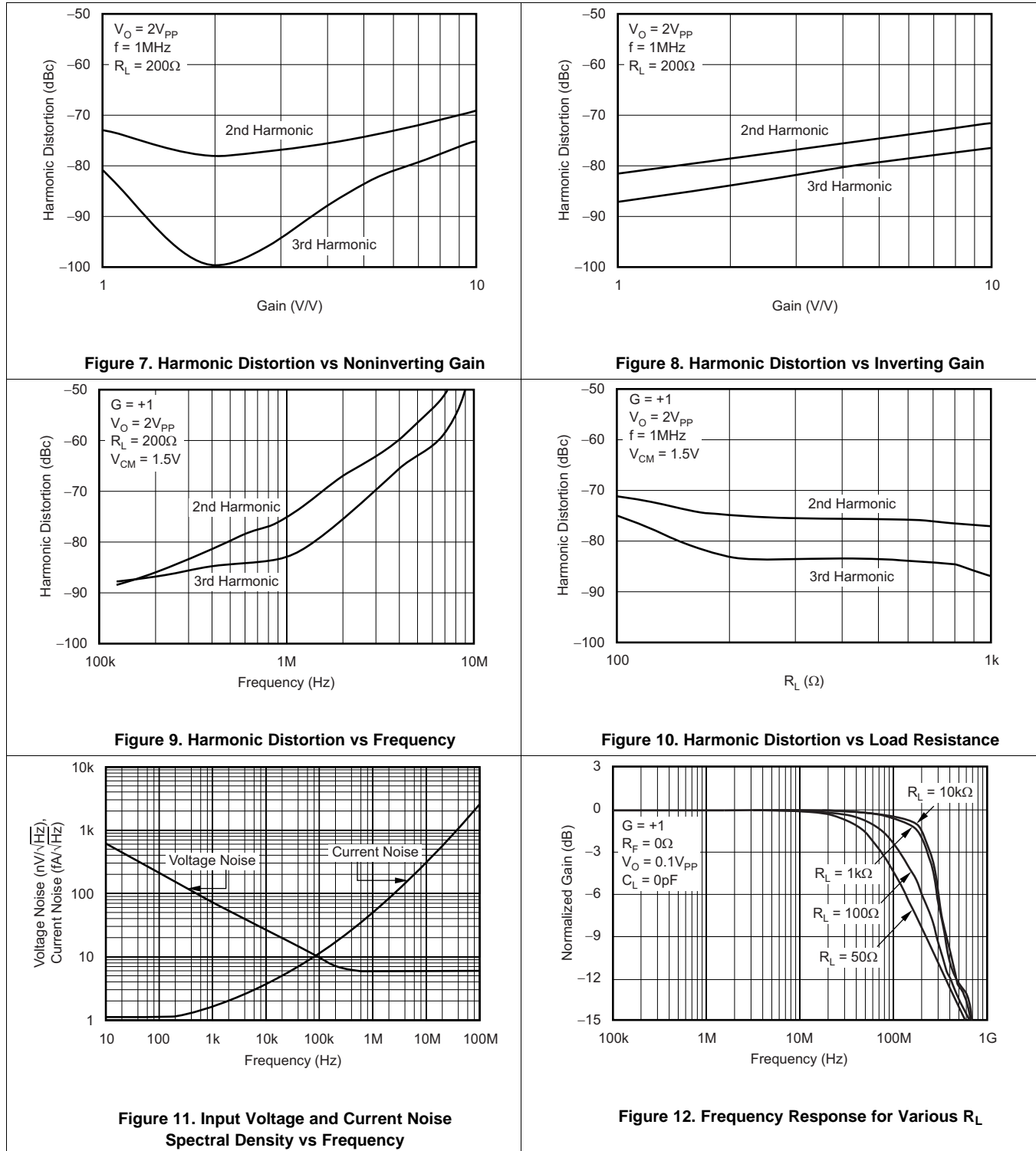


Figure 6. Harmonic Distortion vs Output Voltage

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $G = +1$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $G = +1$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.

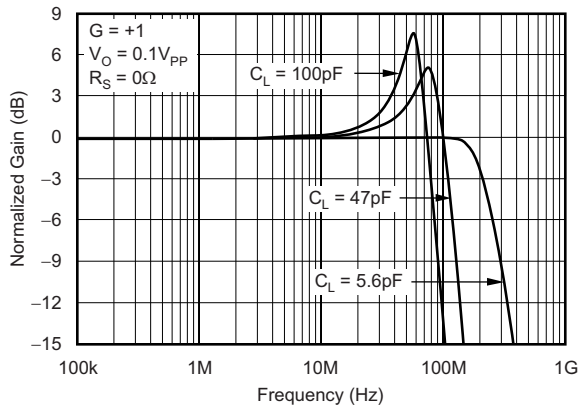


Figure 13. Frequency Response for Various  $C_L$

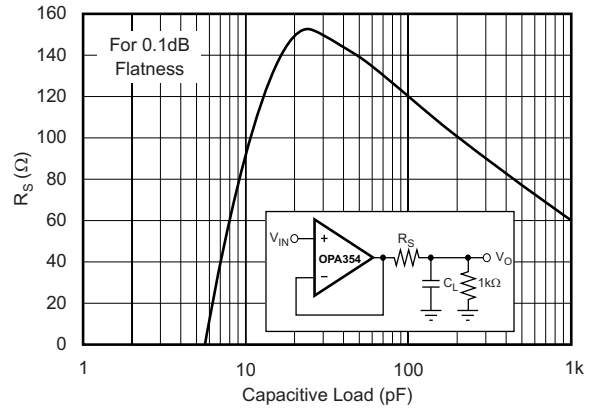


Figure 14. Recommended  $R_S$  vs Capacitive Load

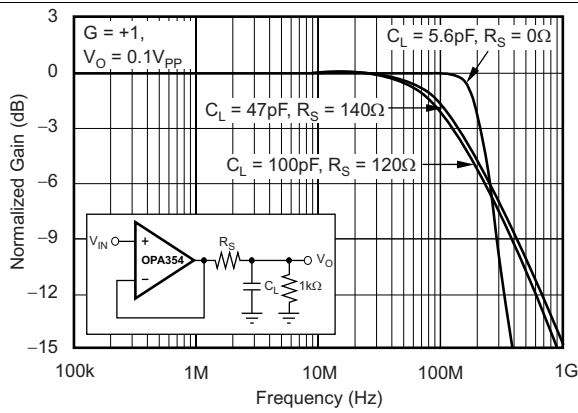


Figure 15. Frequency Response vs Capacitive Load

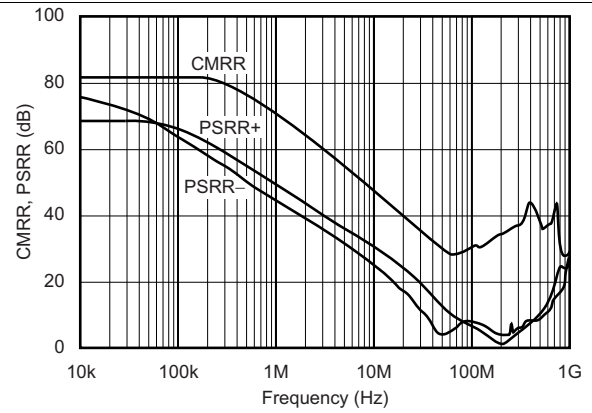


Figure 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

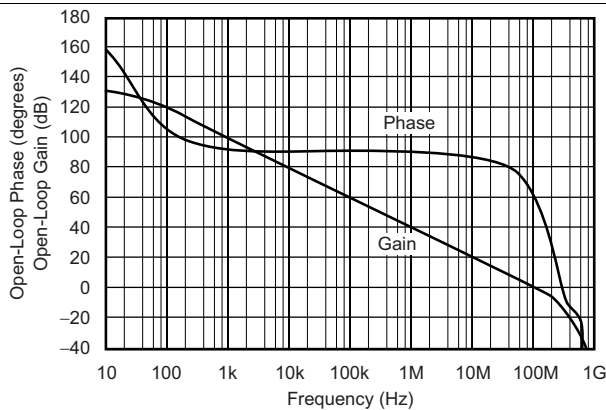


Figure 17. Open-Loop Gain and Phase

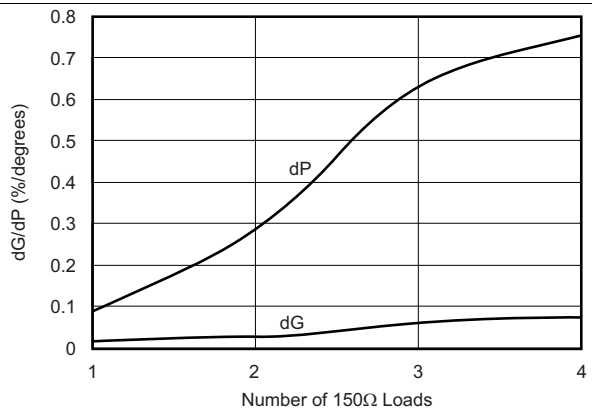


Figure 18. Composite Video Differential Gain and Phase

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $G = +1$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.

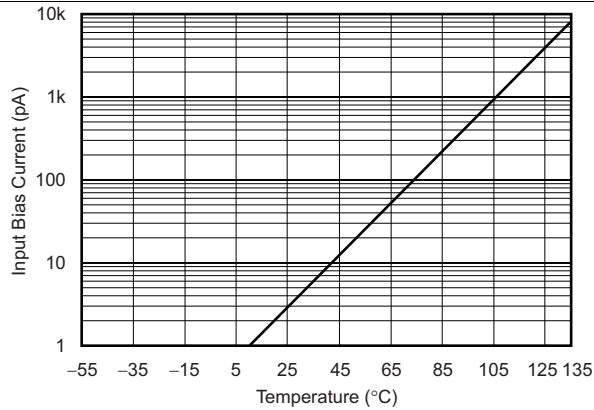


Figure 19. Input Bias Current vs Temperature

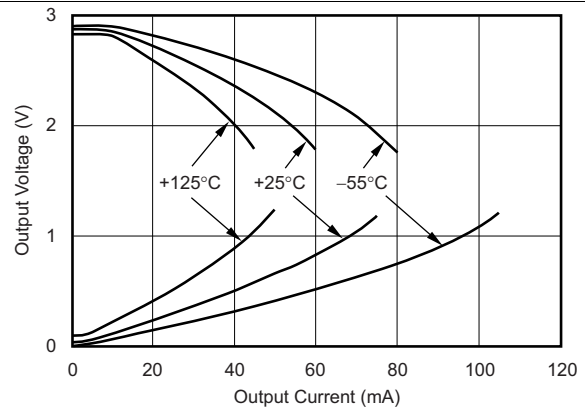


Figure 20. Output Voltage Swing vs Output Current for  $V_S = 3\text{ V}$

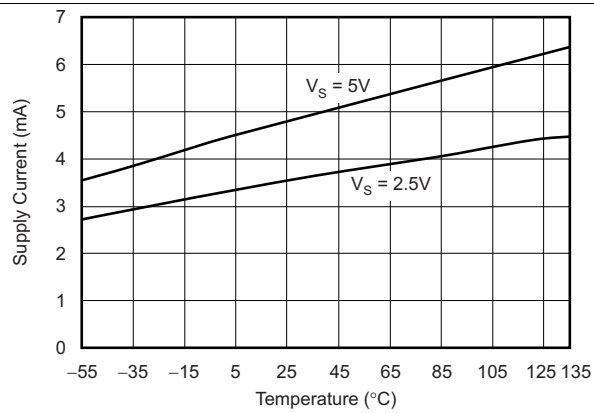


Figure 21. Supply Current vs Temperature

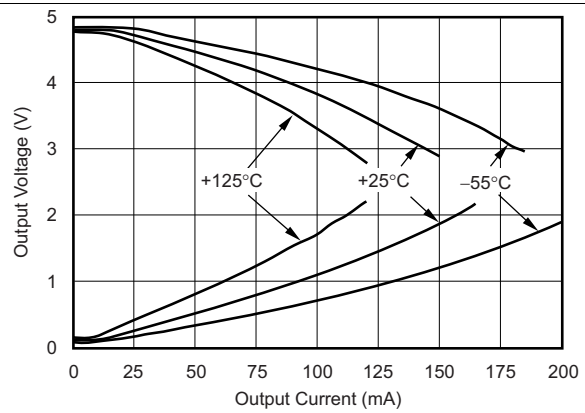


Figure 22. Output Voltage Swing vs Output Current for  $V_S = 5\text{ V}$

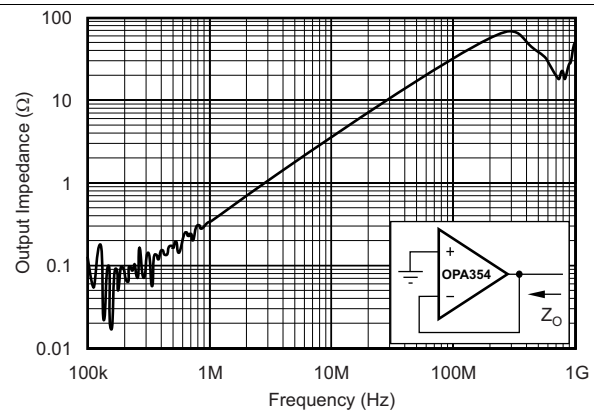


Figure 23. Closed-Loop Output Impedance vs Frequency

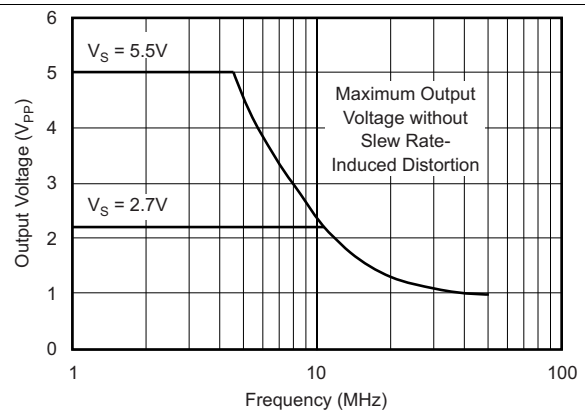
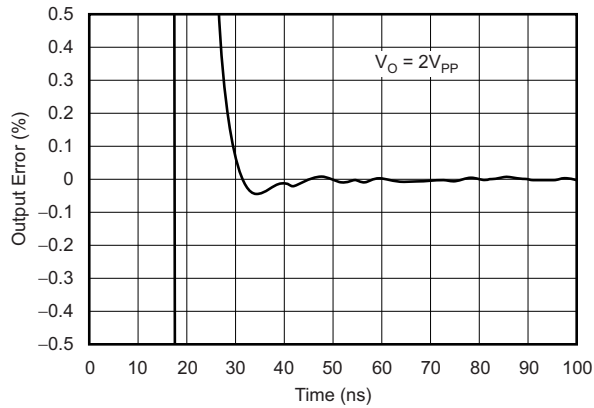


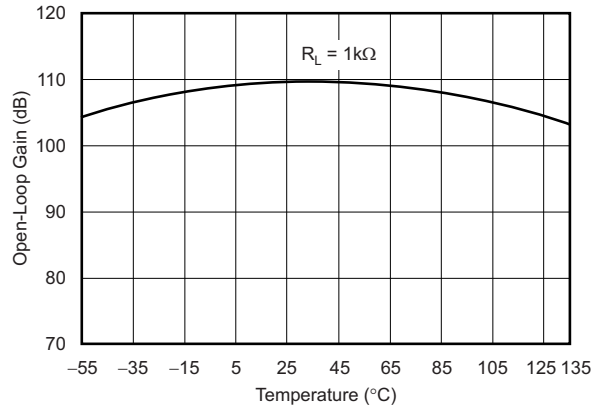
Figure 24. Maximum Output Voltage vs Frequency

**Typical Characteristics (continued)**

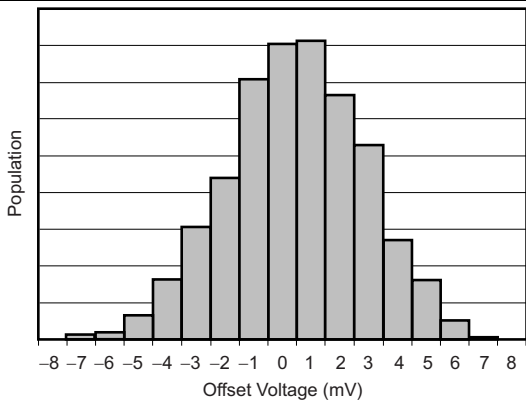
At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ ,  $G = +1$ ,  $R_F = 0\ \Omega$ ,  $R_L = 1\ \text{k}\Omega$ , and connected to  $V_S/2$ , unless otherwise noted.



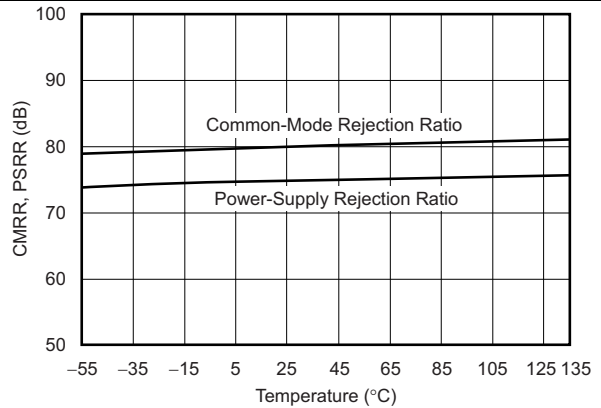
**Figure 25. Output Settling Time to 0.1%**



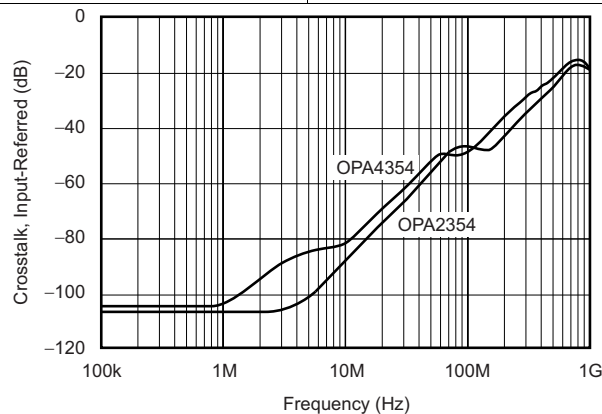
**Figure 26. Open-Loop Gain vs Temperature**



**Figure 27. Offset Voltage Production Distribution**



**Figure 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature**



**Figure 29. Channel-to-Channel Crosstalk**

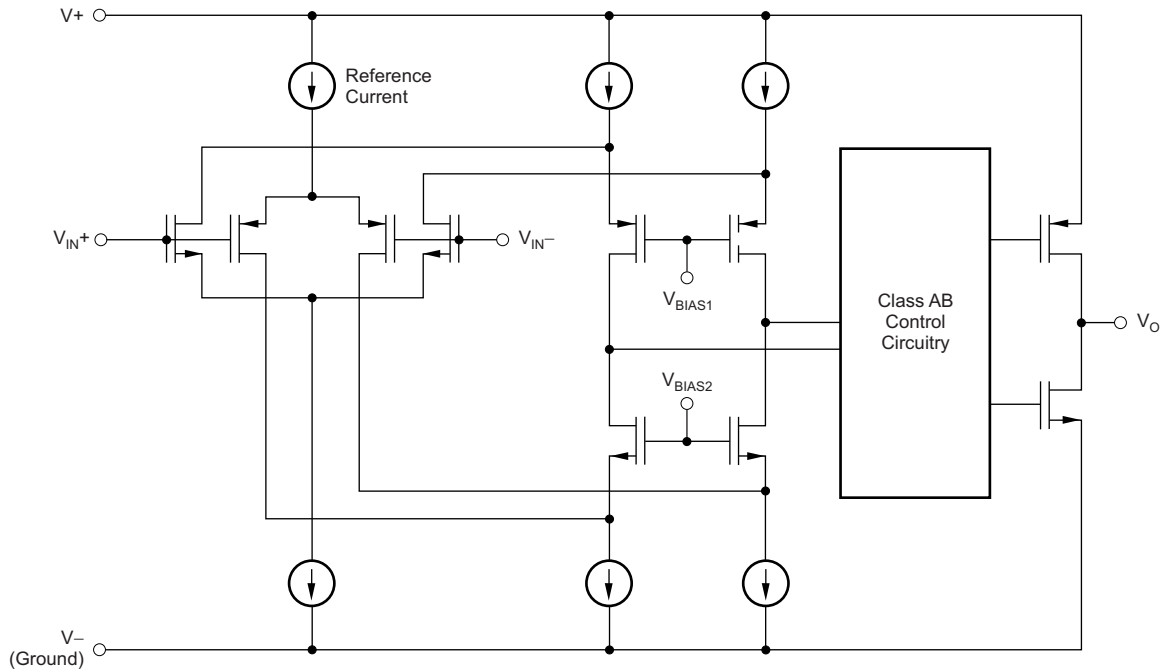
## 8 Detailed Description

### 8.1 Overview

The OPA354 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. It is available as a single, dual, or quad op amp.

The amplifier features a 100-MHz gain bandwidth, and 150-V/ $\mu$ s slew rate, but it is unity-gain stable and can be operated as a +1-V/V voltage follower.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Operating Voltage

The OPA354 is specified over a power-supply range of 2.7 V to 5.5 V ( $\pm 1.35$  V to  $\pm 2.75$  V). However, the supply voltage may range from 2.5 V to 5.5 V ( $\pm 1.25$  V to  $\pm 2.75$  V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in [Typical Characteristics](#) of this data sheet.

### 8.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the OPA354 extends 100 mV beyond the supply rails. This extended range is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.2$  V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately  $(V+) - 1.2$  V. There is a small transition region, typically  $(V+) - 1.5$  V to  $(V+) - 0.9$  V, in which both pairs are on. This 600-mV transition region can vary  $\pm 500$  mV with process variation. Thus, the transition region (both input stages on) can range from  $(V+) - 2$  V to  $(V+) - 1.5$  V on the low end, up to  $(V+) - 0.9$  V to  $(V+) - 0.4$  V on the high end.

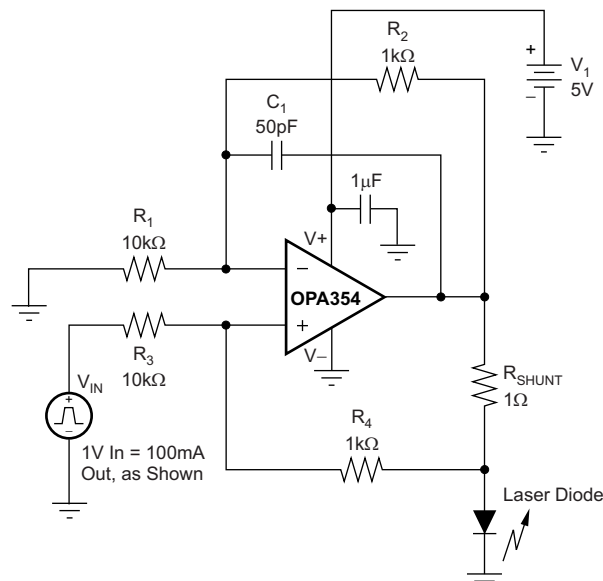
A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

### 8.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads ( $> 200 \Omega$ ), the output voltage swing is typically 100 mV from the supply rails. With 10- $\Omega$  loads, a useful output swing can be achieved while maintaining high open-loop gain. See the typical characteristic curves, [Output Voltage Swing vs Output Current](#) (Figure 20 and Figure 22).

### 8.3.4 Output Drive

The OPA354 output stage can supply a continuous output current of  $\pm 100$  mA and yet provide approximately 2.7 V of output swing on a 5-V supply, as shown in Figure 30. For maximum reliability, TI does not recommend running a continuous DC current in excess of  $\pm 100$  mA. Refer to the typical characteristic curves, [Output Voltage Swing vs Output Current](#) (Figure 20 and Figure 22). For supplying continuous output currents greater than  $\pm 100$  mA, the OPA354 may be operated in parallel, as shown in Figure 31.



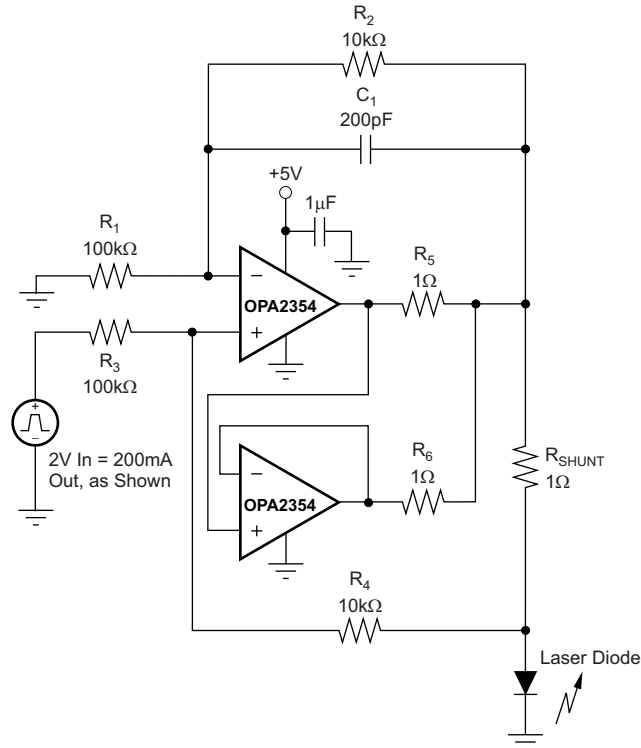
Copyright © 2016, Texas Instruments Incorporated

**Figure 30. Laser Diode Driver**



## Feature Description (continued)

The OPA354 provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA354 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

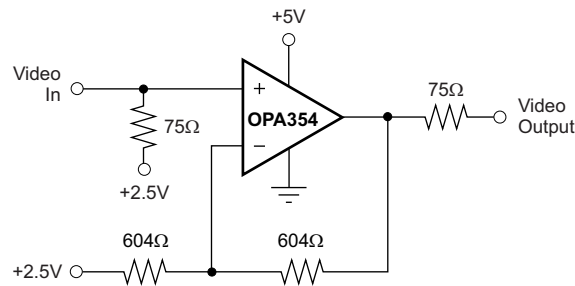


Copyright © 2016, Texas Instruments Incorporated

**Figure 31. Parallel Operation**

### 8.3.5 Video

The OPA354 output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in Figure 32. By back-terminating a transmission line, it does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; it presents only a 150-Ω resistive load to the OPA354 output.

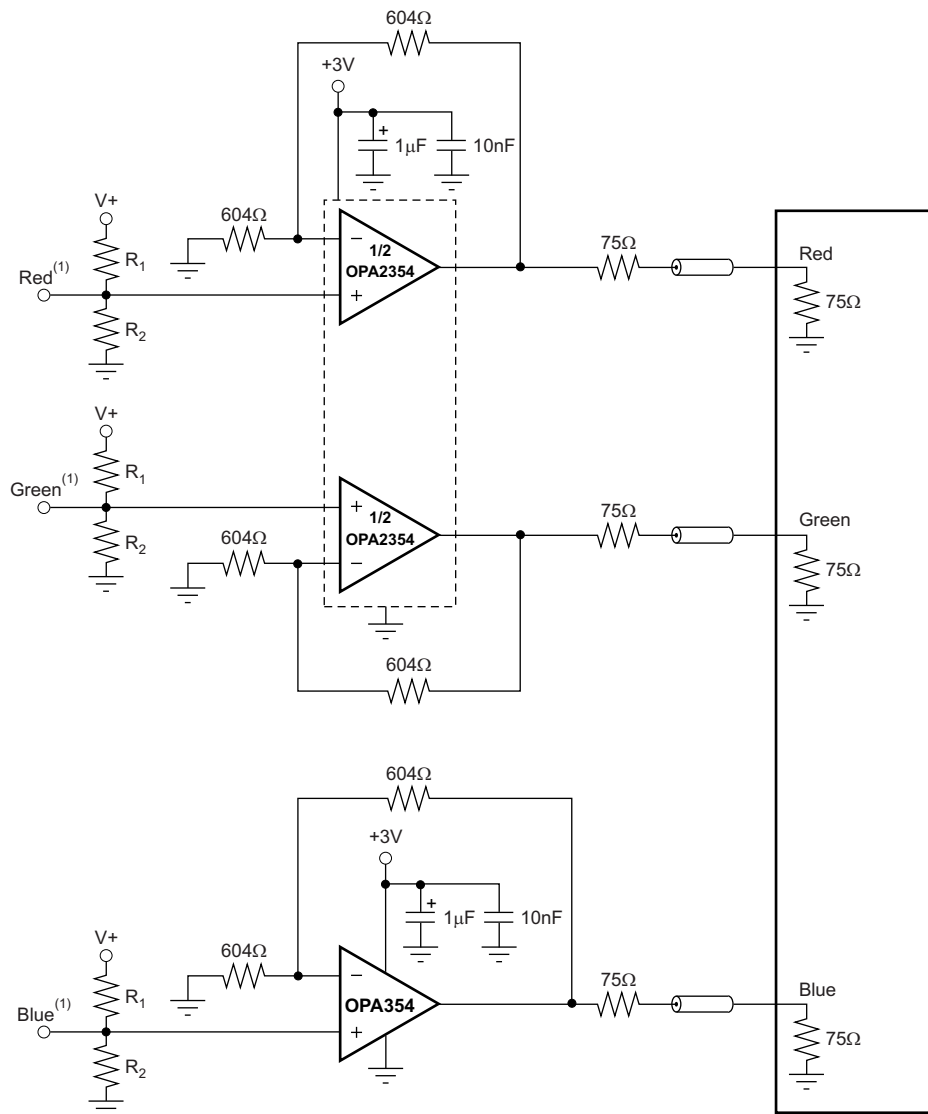


Copyright © 2016, Texas Instruments Incorporated

**Figure 32. Single-Supply Video Line Driver**

The OPA354 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See Figure 33.

Feature Description (continued)



Copyright © 2016, Texas Instruments Incorporated

(1) Source video signal offset 300 mV above ground to accommodate op amp swing-to-ground capability.

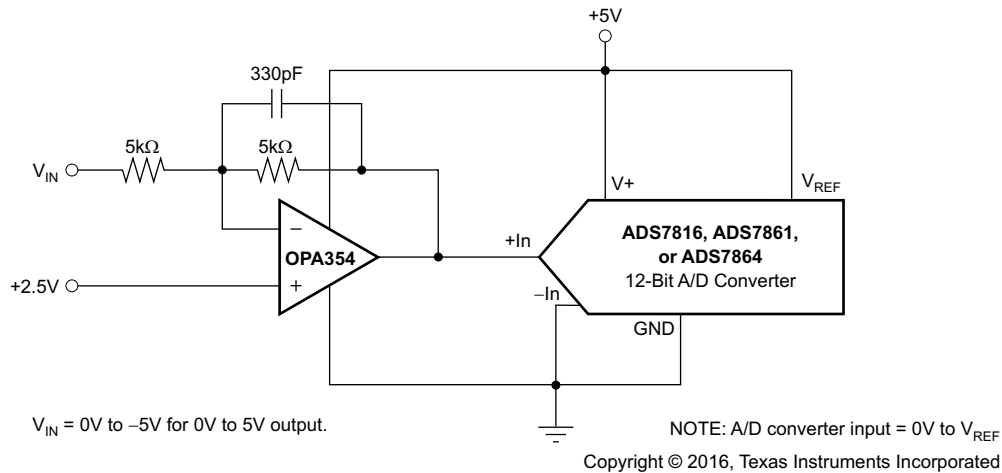
Figure 33. RGB Cable Driver

## Feature Description (continued)

### 8.3.6 Driving Analog-to-Digital converters

The OPA354 series op amps offer 60 ns of settling time to 0.01%, making them a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The OPA354 series provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, the [OPA350 series](#) is recommended.

[Figure 34](#) illustrates the OPA354 driving an A/D converter. With the OPA354 in an inverting configuration, a capacitor across the feedback resistor can be used to filter high-frequency noise in the signal.



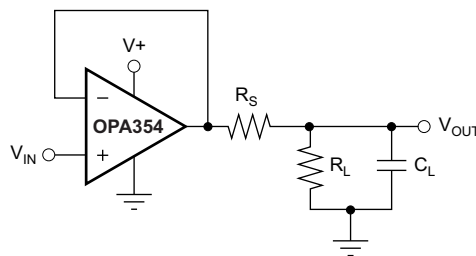
**Figure 34. The OPA354 in Inverting Configuration Driving the ADS7816**

### 8.3.7 Capacitive Load and Stability

The OPA354 series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. Refer to the typical characteristic curve, *Frequency Response for Various  $C_L$*  ([Figure 13](#)) for details.

The OPA354 topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. Refer to the typical characteristic curves, *Recommended  $R_S$  vs Capacitive Load* ([Figure 14](#)) and *Frequency Response vs Capacitive Load* ([Figure 15](#)) for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10- $\Omega$  to 20- $\Omega$  resistor in series with the output, as shown in [Figure 35](#). This configuration significantly reduces ringing with large capacitive loads—see the typical characteristic curve, *Frequency Response vs Capacitive Load* ([Figure 15](#)). However, if there is a resistive load in parallel with the capacitive load,  $R_S$  creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with  $R_L = 10\text{ k}\Omega$  and  $R_S = 20\ \Omega$ , there is approximately a 0.2% error at the output.



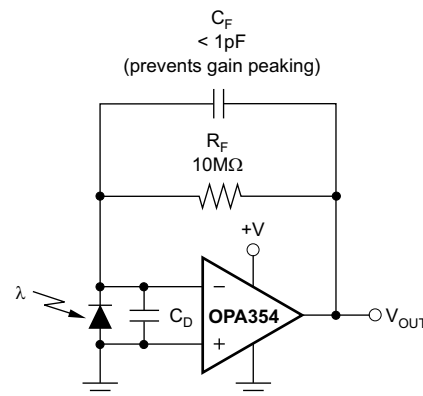
**Figure 35. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive**

## Feature Description (continued)

### 8.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, low input voltage, and current noise make the OPA354 an ideal wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in [Figure 36](#), are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the OPA354], the desired transimpedance gain ( $R_F$ ), and the Gain-Bandwidth Product (GBW) for the OPA354 (100 MHz typical). With these three variables set, the feedback capacitor value ( $C_F$ ) may be set to control the frequency response.



Copyright © 2016, Texas Instruments Incorporated

**Figure 36. Transimpedance Amplifier**

To achieve a maximally flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in [Equation 1](#):

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{\text{GBP}}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by [Equation 2](#):

$$f_{-3\text{dB}} = \sqrt{\frac{\text{GBP}}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS [OPA355](#) (200-MHz GBW) or the [OPA655](#) (400-MHz GBW) may be used.

## 8.4 Device Functional Modes

The OPAx354 family of devices is powered on when the supply is connected. The devices can be operated as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices can also be used with asymmetrical supplies as long as the differential voltage ( $V_-$  to  $V_+$ ) is at least 1.8 V and no greater than 5.5 V (example:  $V_-$  set to -3.5 V and  $V_+$  set to 1.5 V).

## 9 Application and Implementation

### NOTE

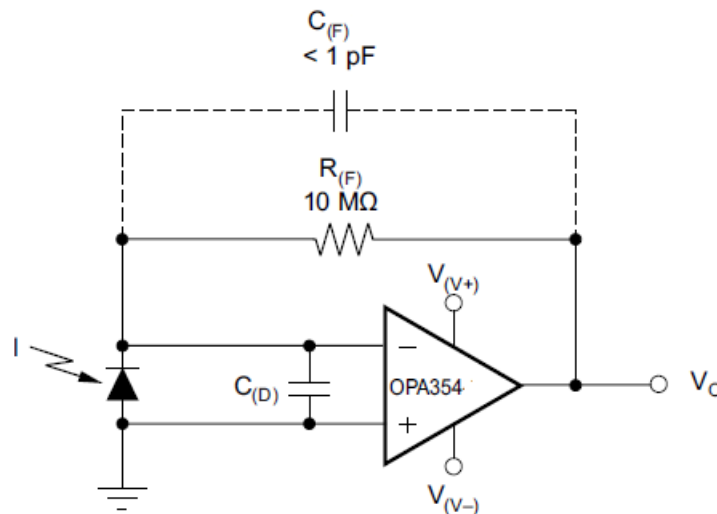
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The OPAx354 family of devices is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The OPAx354 family of devices is available as a single, dual, or quad op amp. The amplifier features a 100-MHz gain bandwidth, and 150-V/ $\mu$ s slew rate, but it is unity-gain stable and can be operated as a 1-V/V voltage follower.

### 9.2 Typical Application

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 family of devices an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in Figure 37, are the expected diode capacitance, which include the parasitic input common-mode and differential-mode input capacitance; the desired transimpedance gain; and the gain-bandwidth (GBW) for the OPAx354 family of devices (20 MHz). With these three variables set, the feedback capacitor value can be set to control the frequency response. Feedback capacitance includes the stray capacitance of, which is 0.2 pF for a typical surface-mount resistor.



Copyright © 2016, Texas Instruments Incorporated

Figure 37. Dual-Supply Transimpedance Amplifier

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage, $V_{(V+)}$	2.5 V
Supply voltage, $V_{(V-)}$	-2.5 V

$C_{(F)}$  is optional to prevent gain peaking.  $C_{(F)}$  includes the stray capacitance of  $R_{(F)}$ .

### 9.2.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using [Equation 3](#).

$$\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{\text{GBW}}{4 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (3)$$

Calculate the bandwidth using [Equation 4](#).

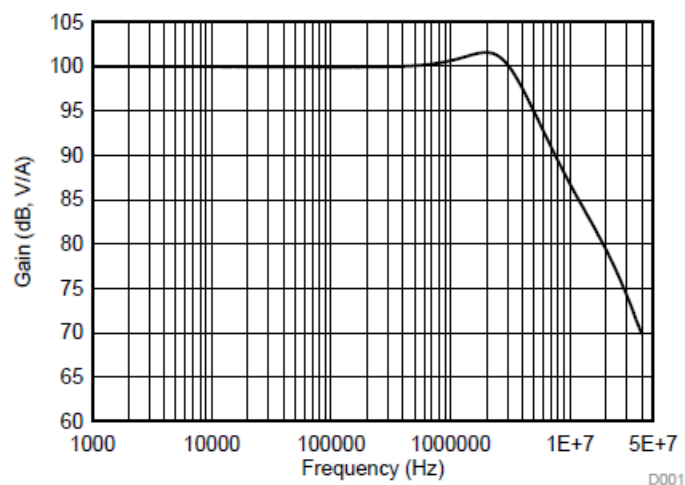
$$f_{(-3 \text{ dB})} = \sqrt{\frac{\text{GBW}}{2 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (4)$$

#### 9.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select  $R_{(F)}$  to create the total required gain. Using a lower value for  $R_{(F)}$  and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by  $R_{(F)}$  increases with the square-root of  $R_{(F)}$ , whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the  $R_{(F)}$  to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

### 9.2.3 Application Curve



**Figure 38. AC Transfer Function**

## 10 Power Supply Recommendations

The OPAx354 family of devices is specified for operation from 2.5 V to 5.5 V ( $\pm 1.25$  to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown *Typical Characteristics*.

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

## 11 Layout

### 11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be employed for the OPA354. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin assure clean, stable operation. Large areas of copper also provides a means of dissipating heat that is generated in normal operation.

TI does not recommend using sockets with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1- $\mu\text{F}$  or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

### 11.2 Layout Example

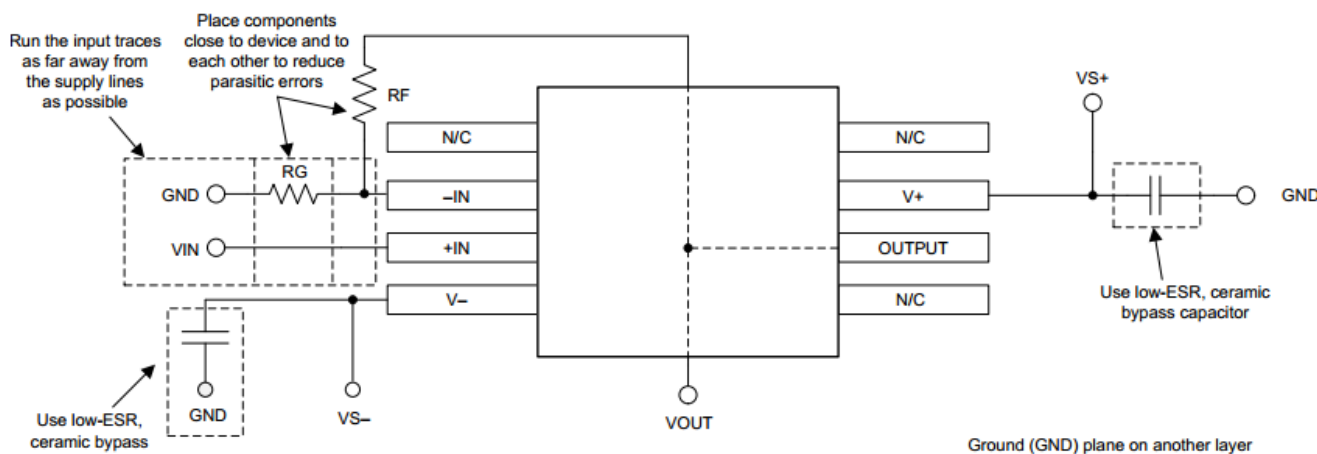


Figure 39. Operational Amplifier Board Layout for Noninverting Configuration

### 11.3 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor,  $V_S - V_O$ . Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. *AB-039 Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads, and can be found at [www.ti.com](http://www.ti.com).

## Power Dissipation (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application.

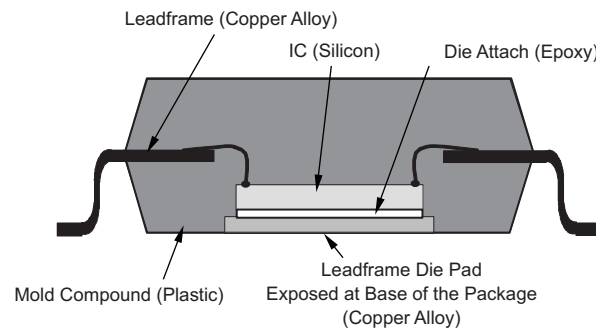
### 11.4 PowerPAD Thermally-Enhanced Package

In addition to the regular 5-pin SOT-23 and 9-pin VSSOP packages, the single and dual versions of the OPA354 also come in an 8-pin SOIC PowerPAD package. The 98-pin SO with PowerPAD is a standard size 8-pin SOIC package where the exposed leadframe on the bottom of the package can be soldered directly to the PCB to create an extremely low thermal resistance. This direct attachment enhances the OPA354 power dissipation capability significantly, and eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques.

#### NOTE

Because the 8-pin HSOP PowerPAD is pin-compatible with standard 8-pin SOIC packages, the OPA354 and OPA2354 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. This configuration provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC, as shown in [Figure 40](#). This exposed die provides an extremely low thermal resistance ( $R_{\theta JC}$ ) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.



**Figure 40. Section View of a PowerPAD Package**

### 11.5 PowerPAD Assembly Process

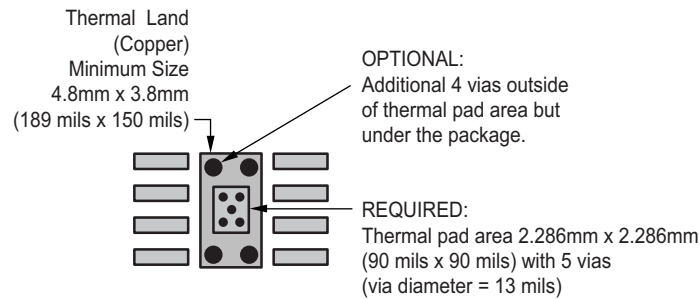
The PowerPAD must be connected to the most negative supply voltage for the device, which is ground in single-supply applications and  $V^-$  in split-supply applications.

Prepare the PCB with a top-side etch pattern, as shown in [Figure 41](#). The exact land design may vary based on the specific assembly process requirements. There must be etch for the leads as well as etch for the thermal land.

Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes must be 13 mils (.013 in) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow. TI recommends a minimum of 5 holes for the 8-pin HSOP PowerPAD package, as shown in [Figure 41](#).



**PowerPAD Assembly Process (continued)**

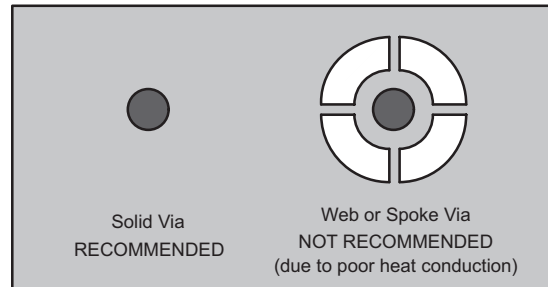


**Figure 41. 8-Pin PowerPAD PCB Etch and Via Pattern**

TI recommends, but does not require, placing a small number of additional holes under the package and outside the thermal pad area. These holes provide additional heat paths between the copper thermal land and the ground plane. They may be larger because they are not in the area to be soldered, so wicking is not a problem. This technique is illustrated in [Figure 41](#).

Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single-supply applications, and to V- for split-supply applications.

When laying out these holes, do not use the typical web or spoke via connection methodology, as shown in [Figure 42](#). Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This feature makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package must make connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.



**Figure 42. Via Connection**

The top-side solder mask must leave the pad connections and the thermal pad area exposed. The thermal pad area must leave the 13-mil holes exposed. The larger holes outside the thermal pad area may be covered with solder mask.

Apply solder paste to the exposed thermal pad area and all of the package terminals.

With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation and processing results in a part that is properly installed.

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, please see [PowerPAD Thermally Enhanced Package](#) located at [www.ti.com](http://www.ti.com).

## 12 Device and Documentation Support

### 12.1 Documentation Support

For related documentation see the following:

- [ADS8326 16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling ANALOG-TO-DIGITAL CONVERTER \(SBAS343\)](#)
- [Circuit Board Layout Techniques \(SLOA089\)](#)
- [Compensate Transimpedance Amplifiers Intuitively \(SBOA055\)](#)
- [FilterPro™ User's Guide \(SBFA001\)](#)
- [Noise Analysis for High-Speed Op Amps](#)
- [OPA380 and OPA2380 Precision, High-Speed Transimpedance Amplifier \(SBOS291\)](#)
- [OPA355, OPA2355, and OPA3355 200MHz, CMOS OPERATIONAL AMPLIFIER WITH SHUTDOWN \(SBOS195\)](#)
- [OPA656 Wideband, Unity-Gain Stable, FET-Input OPERATIONAL AMPLIFIER \(SBOS196\)](#)
- [POWER AMPLIFIER STRESS AND POWER HANDLING LIMITATIONS \(SBOA022\)](#)
- [PowerPAD Thermally Enhanced Package \(SLMA002\)](#)

### 12.2 Related Links

[Table 2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA354	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA2354	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA4354	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2354AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	<a href="#">Samples</a>
OPA2354AIDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	<a href="#">Samples</a>
OPA2354AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	<a href="#">Samples</a>
OPA2354AIDDARG3	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	<a href="#">Samples</a>
OPA2354AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	<a href="#">Samples</a>
OPA2354AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	<a href="#">Samples</a>
OPA2354AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	<a href="#">Samples</a>
OPA2354AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	<a href="#">Samples</a>
OPA354AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	<a href="#">Samples</a>
OPA354AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	<a href="#">Samples</a>
OPA354AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	<a href="#">Samples</a>
OPA354AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	<a href="#">Samples</a>
OPA354AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	<a href="#">Samples</a>
OPA354AIDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	<a href="#">Samples</a>
OPA354AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	<a href="#">Samples</a>
OPA4354AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	<a href="#">Samples</a>
OPA4354AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4354AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	<a href="#">Samples</a>
OPA4354AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	<a href="#">Samples</a>
OPA4354AIPWR	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	<a href="#">Samples</a>
OPA4354AIPWRG4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	<a href="#">Samples</a>
OPA4354AIPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	<a href="#">Samples</a>
OPA4354AIPWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA4354 :**

- Automotive: [OPA4354-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2354AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA354AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA354AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA354AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4354AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4354AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA354AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA354AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
OPA4354AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4354AIPWR	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA4354AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0



DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

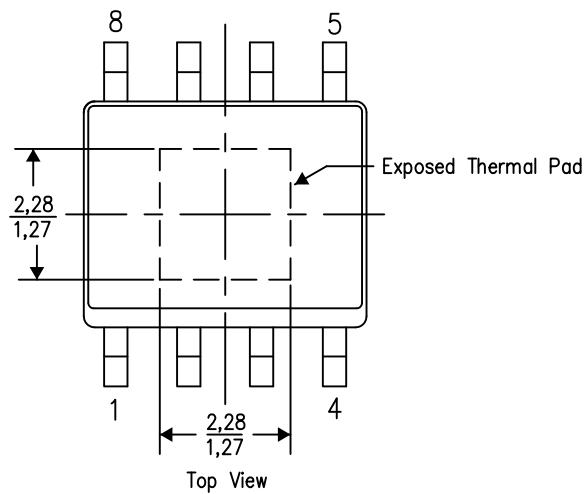
PowerPAD™ PLASTIC SMALL OUTLINE

**THERMAL INFORMATION**

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

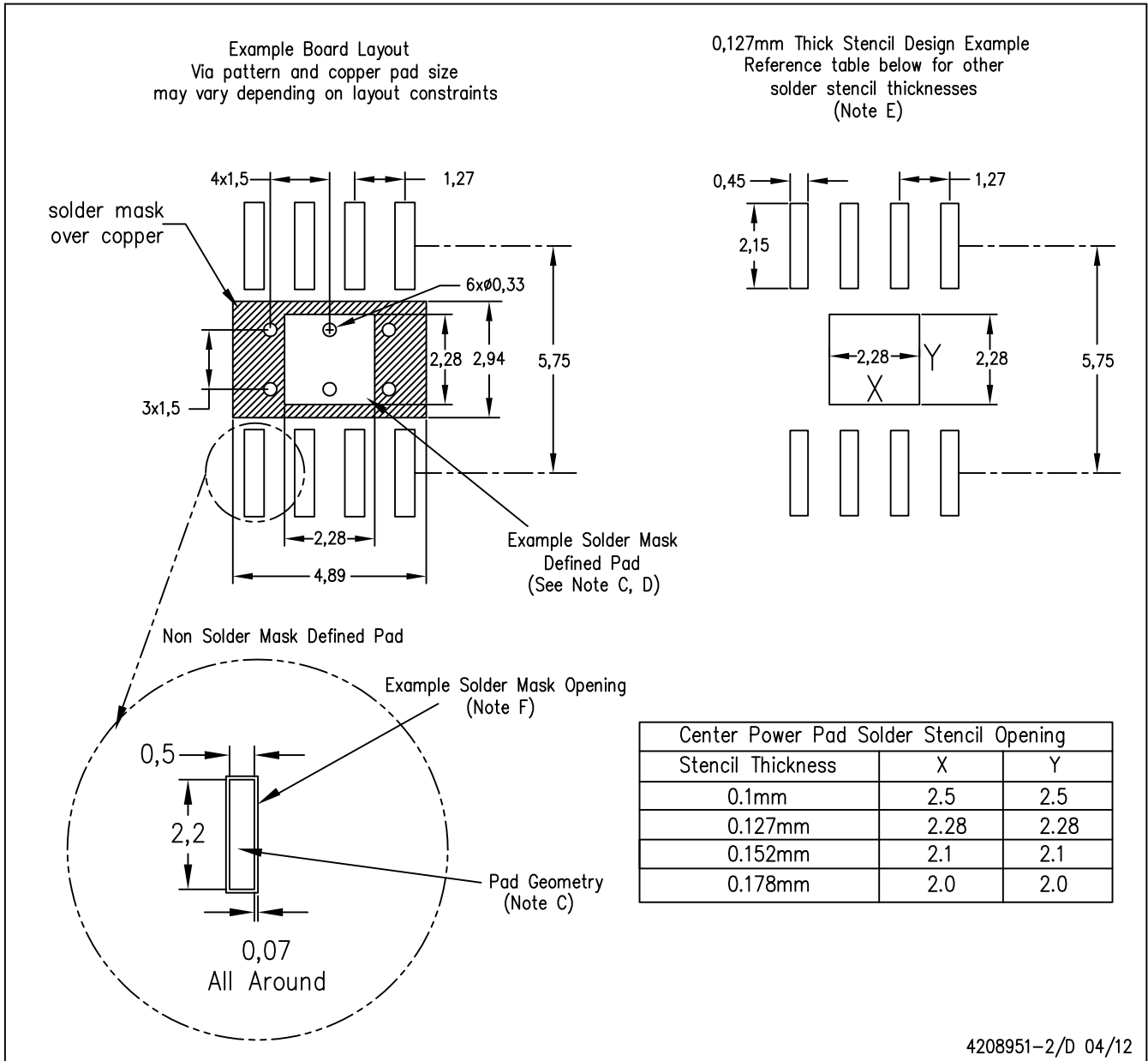


Exposed Thermal Pad Dimensions

4206322-2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



4208951-2/D 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)