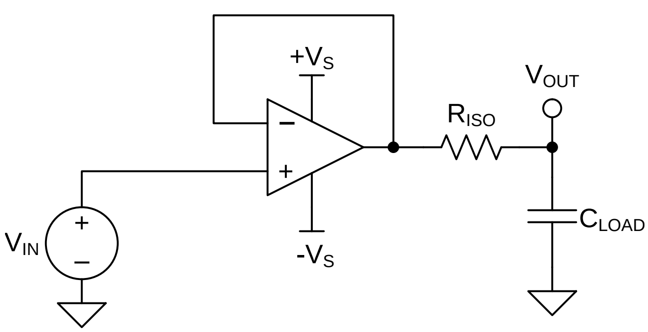
OPA2171-EP 36-V, Single-Supply, SOT553, General-Purpose Operational Amplifiers

1 Features

- Supply Range: 2.7 to 36 V, ±1.35 V to ±18 V
- Low Noise: 14 nV/√Hz
- Low Offset Drift: ±0.3 µV/°C (Typ)
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 3 MHz
- Low Quiescent Current: 475 µA per Amplifier
- High Common-Mode Rejection: 120 dB (Typ)
- Low-Input Bias Current: 8 pA
- *micro*Package: Dual in VSSOP-8
- **Supports Defense, Aerospace, and Medical Applications:**
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Available in Extended (–55°C to 125°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

Unity-Gain Buffer With R_{ISO} Stability Compensation



2 Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

3 Description

The OPA2171-EP is a 36-V, single-supply, low-noise operational amplifier with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most operational amplifiers, which are specified at only one supply voltage, the OPA2171-EP is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal. The OPA2171-EP is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPA2171-EP operational amplifier is specified from –55°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2171-EP	VSSOP (8)	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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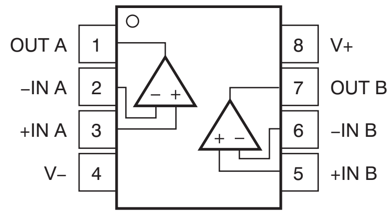
4 Revision History

DATE	REVISION	NOTES
September 2015	*	Initial release.

5 Pin Configuration and Functions

DCU Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage		±20		V
Signal input pins	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current	–10	10	mA
Output short circuit(2)		Continuous		
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Operating temperature, T_J	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA2171-EP	UNIT
		DCU (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	74.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_J = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.25	±1.8	mV
Over temperature		T_J = –55°C to 125°C		0.3	±2	mV
Drift	dV_{OS}/dT	T_J = –55°C to 125°C		0.3		µV/°C
vs power supply	PSRR	V_S = 4 to 36 V, T_A = –55°C to 125°C		1	±5	µV/V
Channel separation, dc		dc		5		µV/V
INPUT BIAS CURRENT						
Input bias current	I_B			±8	±15	pA
Over temperature		T_J = –55°C to 125°C			±4	nA
Input offset current	I_{OS}			±4		pA
Over temperature		T_J = –55°C to 125°C			±4	nA
NOISE						
Input voltage noise		f = 0.1 to 10 Hz		3		μV_{PP}
Input voltage noise density	e_n	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		14		nV/√Hz
INPUT VOLTAGE						
Common-mode voltage range(1)	V_{CM}		(V–) – 0.1 V		(V+) – 2 V	V
Common-mode rejection ratio	CMRR	V_S = ±2 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_J = –55°C to 125°C	87	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_J = –55°C to 125°C	104	120		dB
INPUT IMPEDANCE						
Differential				100 || 3		MΩ || pF
Common-mode				6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	V_S = 4 to 36 V, (V–) + 0.35 V < V_O < (V+) – 0.35 V, T_J = –55°C to 125°C	110	130		dB
FREQUENCY RESPONSE						
Gain bandwidth product	GBP			3.0		MHz
Slew rate	SR	G = +1		1.5		V/µs
Settling time	t_S	To 0.1%, V_S = ±18 V, G = +1, 10-V step		6		µs
		To 0.01% (12 bit), V_S = ±18 V, G = +1, 10-V step		10		µs
Overload recovery time		V_{IN} × Gain > V_S		2		µs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$		0.0002%		
OUTPUT						
Voltage output swing from rail	V_O	V_S = 5 V, R_L = 10 kΩ		30		mV
Over temperature		R_L = 10 kΩ, A_{OL} ≥ 110 dB, T_J = –55°C to 125°C	(V–) + 0.35		(V+) – 0.35	V
Short-circuit current	I_{SC}			+25/–35		mA
Capacitive load drive	C_{LOAD}			See *Typical Characteristics*		pF
Open-loop output resistance	R_O	f = 1 MHz, I_O = 0 A		150		Ω

(1) The input range can be extended beyond (V+) – 2 V up to V+. See *Typical Characteristics* and *Application and Implementation* for additional information.

Electrical Characteristics (continued)

at T_J = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
Specified voltage range	V_S		2.7		36	V
Quiescent current per amplifier	I_Q	I_O = 0 A		475	595	µA
Over temperature		I_O = 0 A, T_J = –55°C to 125°C			650	µA
TEMPERATURE						
Operating temperature	T_J		–55		125	°C

6.6 Typical Characteristics

Table 1. Characteristic Performance Measurements

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V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

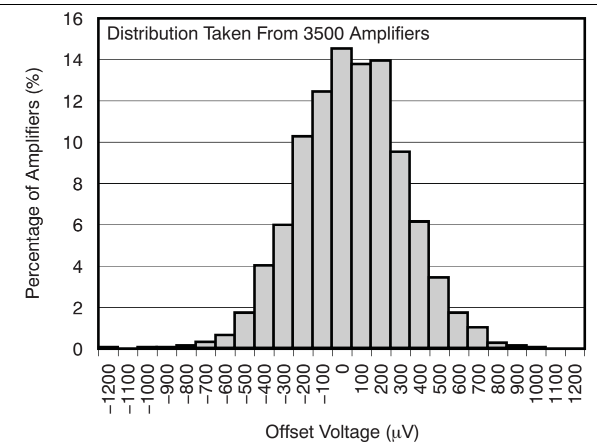


Figure 1. Offset Voltage Production Distribution

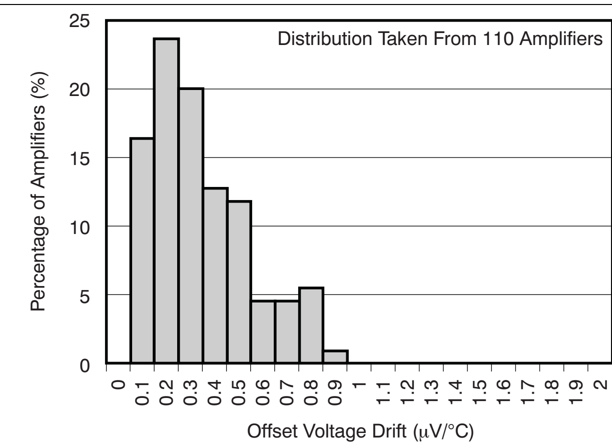


Figure 2. Offset Voltage Drift Distribution

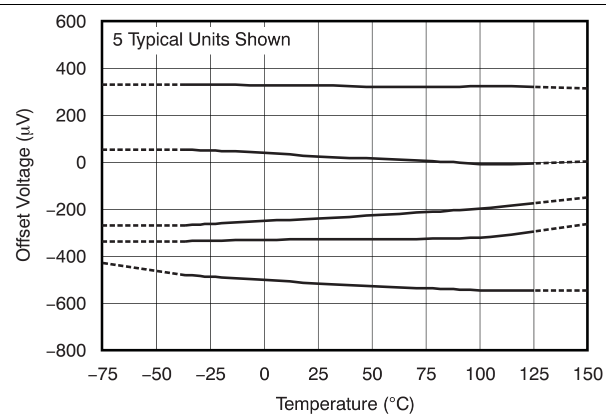


Figure 3. Offset Voltage vs Temperature

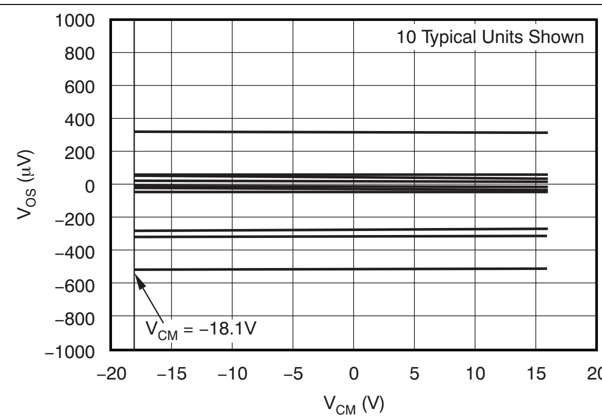


Figure 4. Offset Voltage vs Common-Mode Voltage

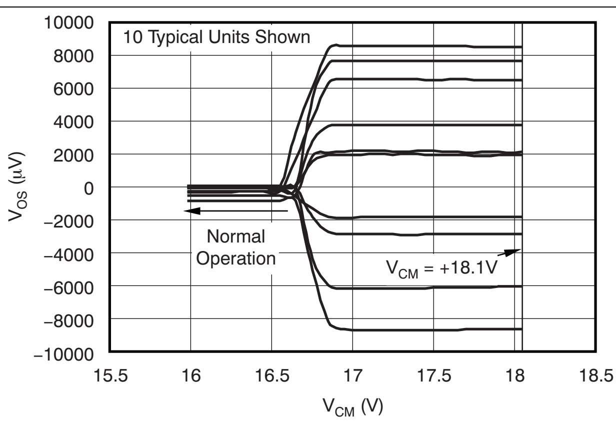


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

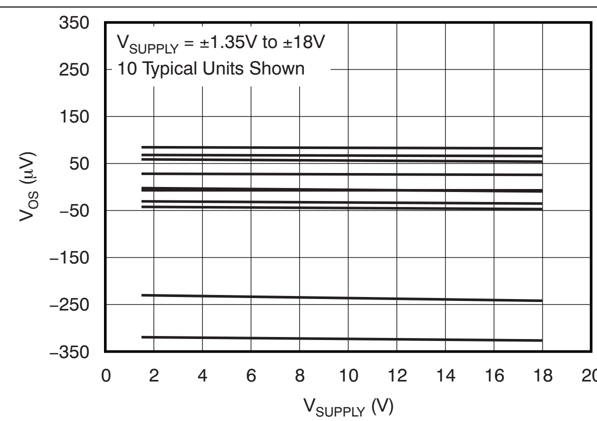


Figure 6. Offset Voltage vs Power Supply

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

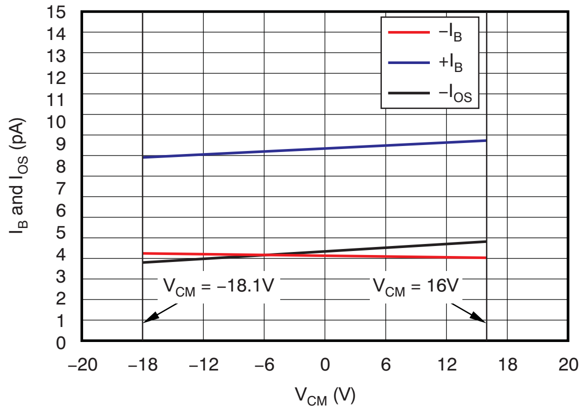


Figure 7. I_B and I_{OS} vs Common-Mode Voltage

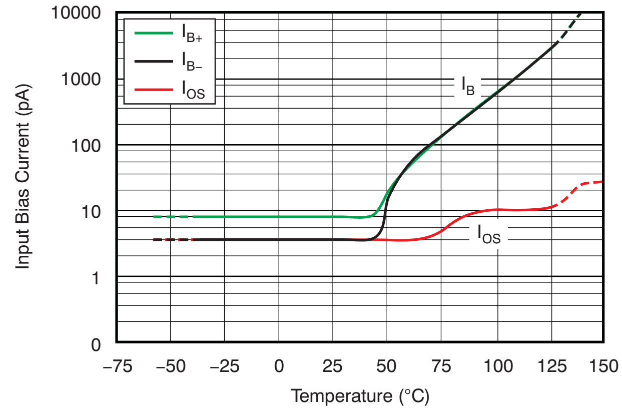


Figure 8. Input Bias Current vs Temperature

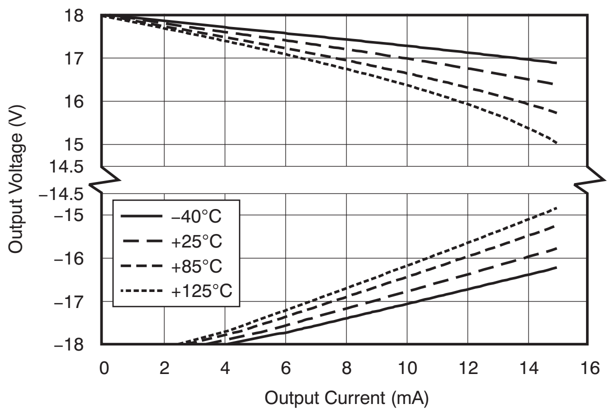


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

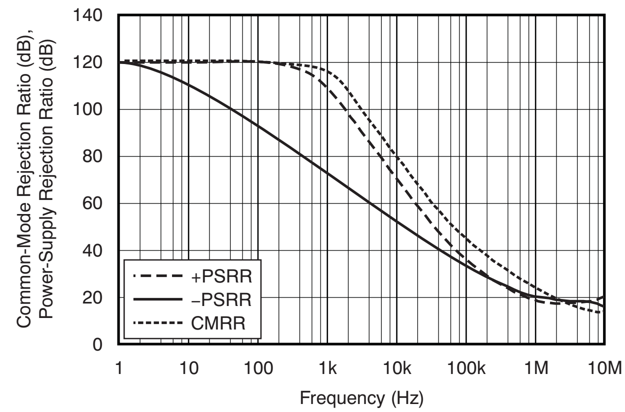


Figure 10. CMRR and PSRR vs Frequency (Referred-to Input)

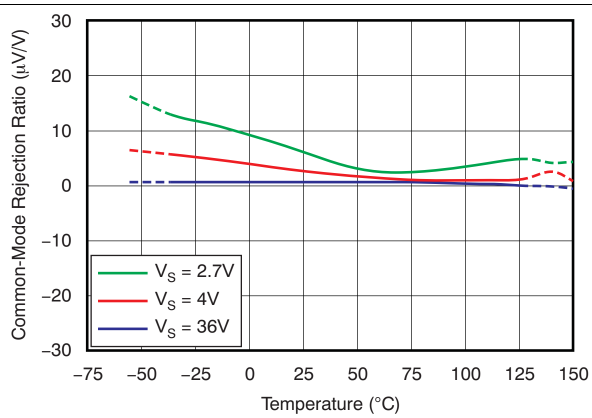


Figure 11. CMRR vs Temperature

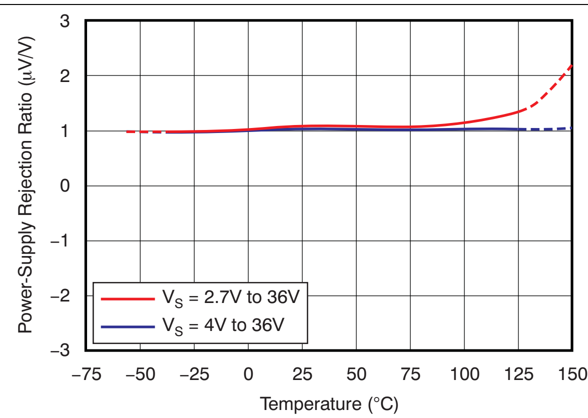


Figure 12. PSRR vs Temperature

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

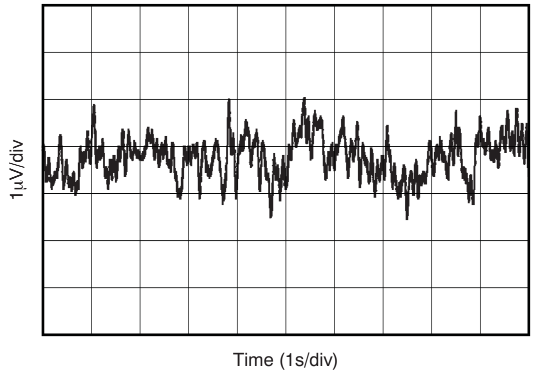


Figure 13. 0.1-Hz to 10-Hz Noise

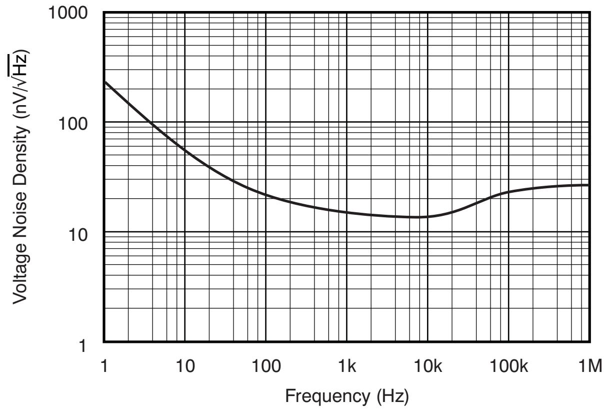


Figure 14. Input Voltage Noise Spectral Density vs Frequency

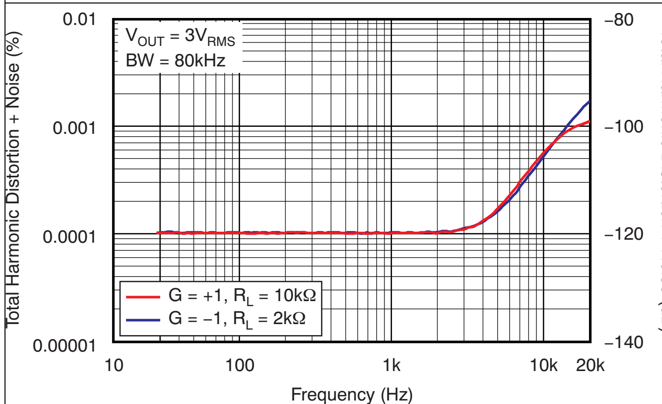


Figure 15. THD+N Ratio vs Frequency

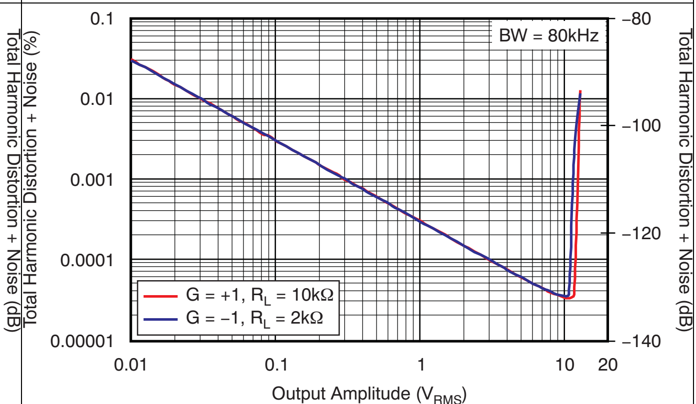


Figure 16. THD+N vs Output Amplitude

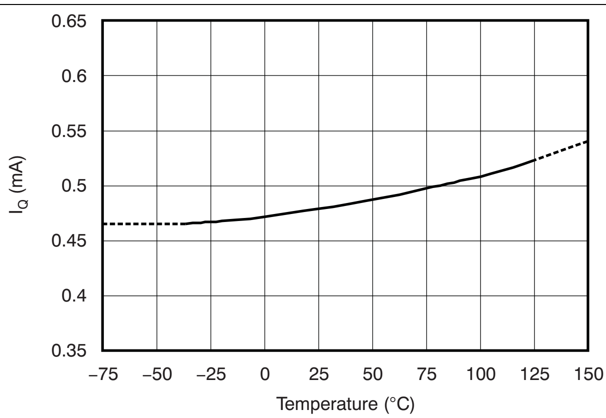


Figure 17. Quiescent Current vs Temperature

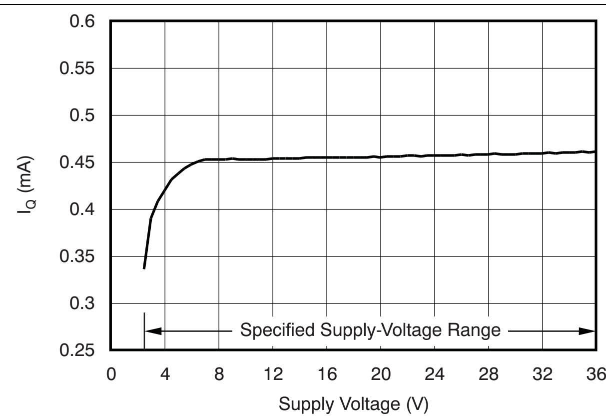


Figure 18. Quiescent Current vs Supply Voltage

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

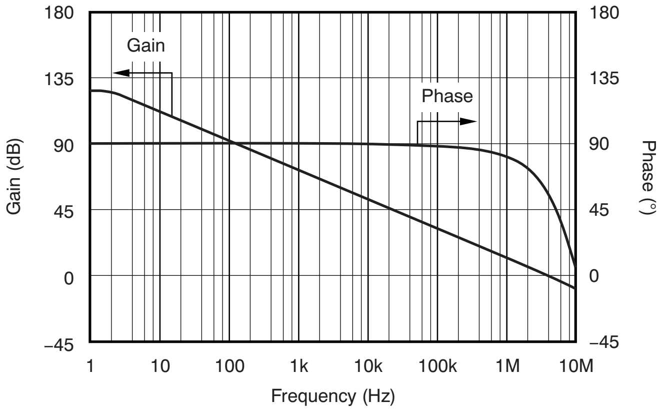


Figure 19. Open-Loop Gain and Phase vs Frequency

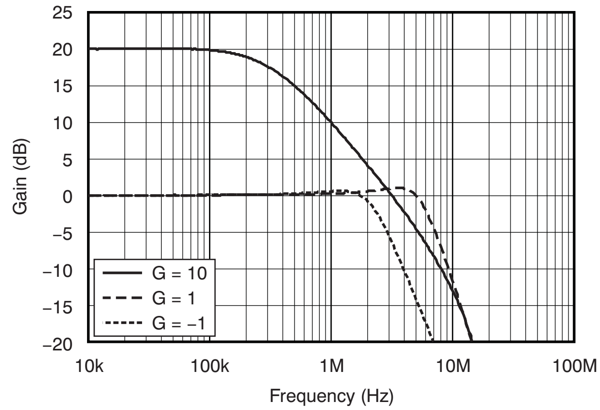


Figure 20. Closed-Loop Gain vs Frequency

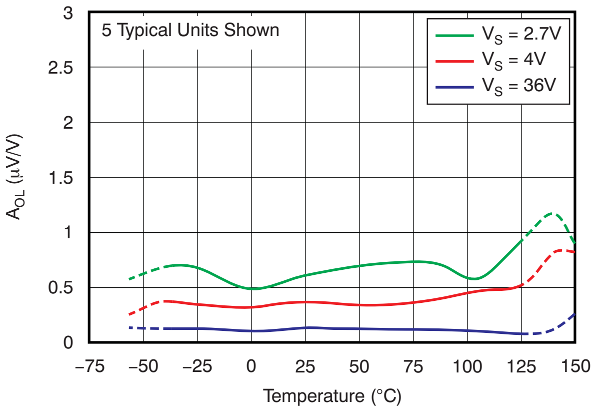


Figure 21. Open-Loop Gain vs Temperature

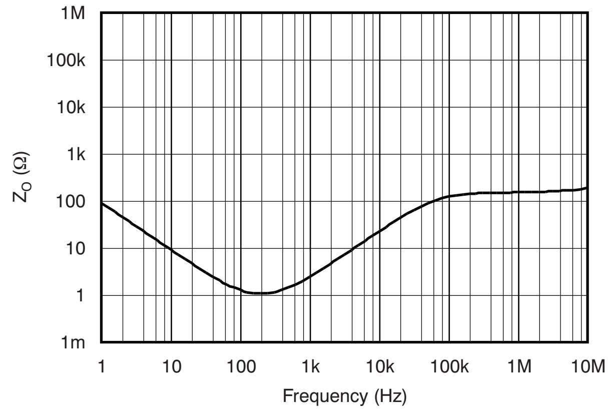


Figure 22. Open-Loop Output Impedance vs Frequency

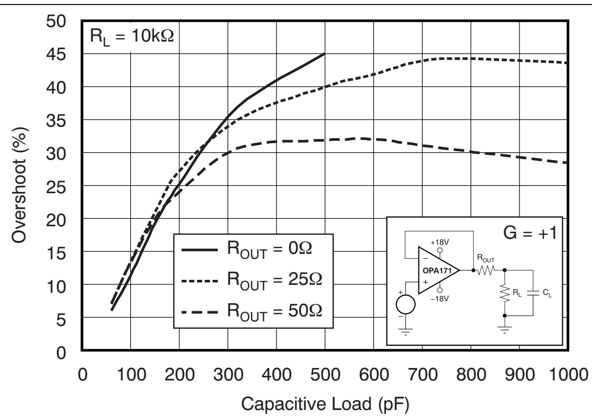


Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

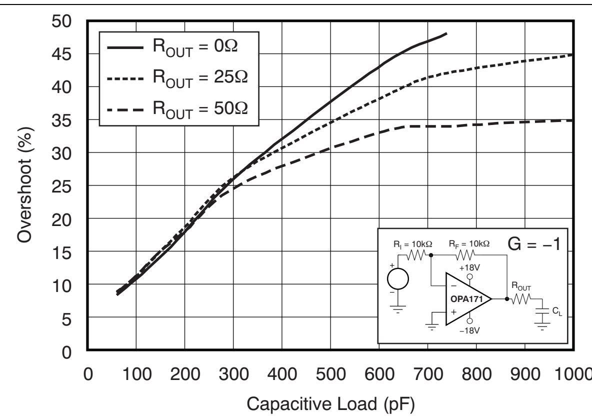


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

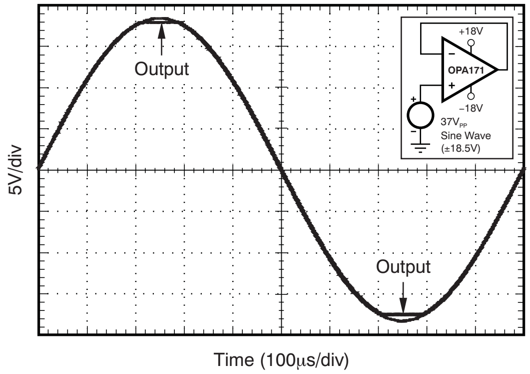


Figure 25. No Phase Reversal

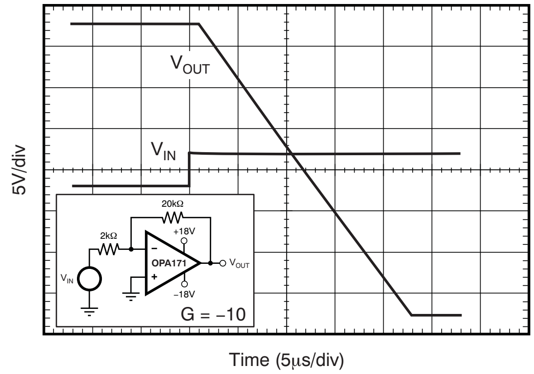


Figure 26. Positive Overload Recovery

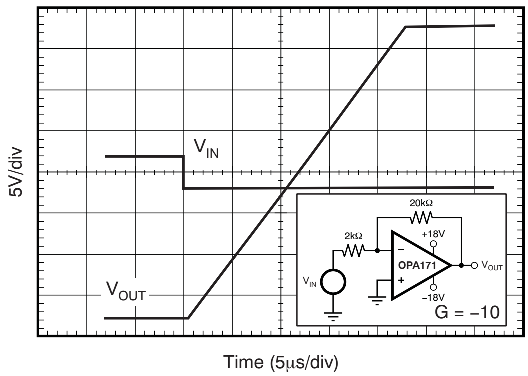


Figure 27. Negative Overload Recovery

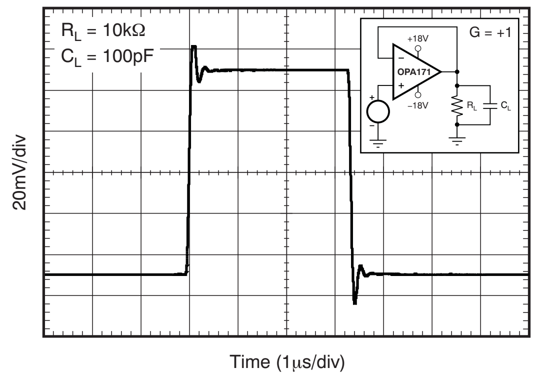


Figure 28. Small-Signal Step Response (100 mV)

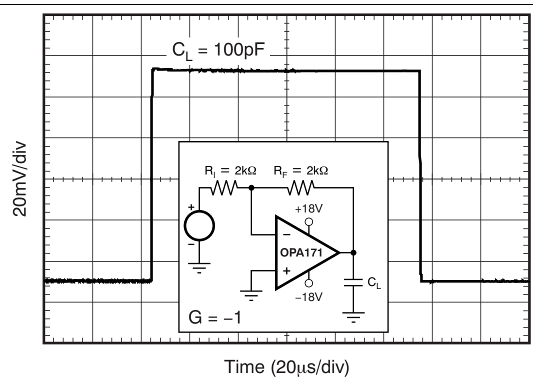


Figure 29. Small-Signal Step Response (100 mV)

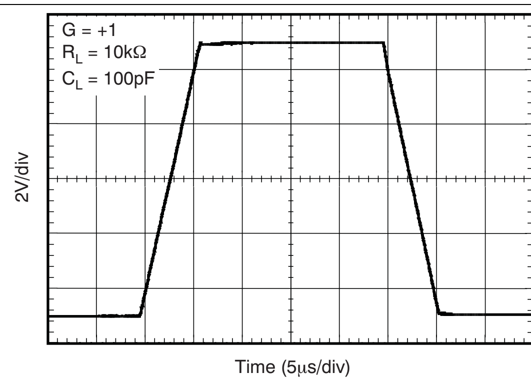


Figure 30. Large-Signal Step Response

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

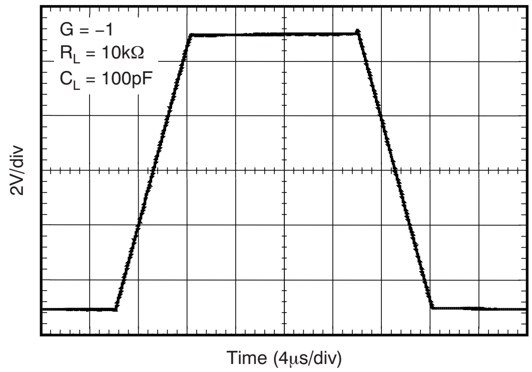


Figure 31. Large-Signal Step Response

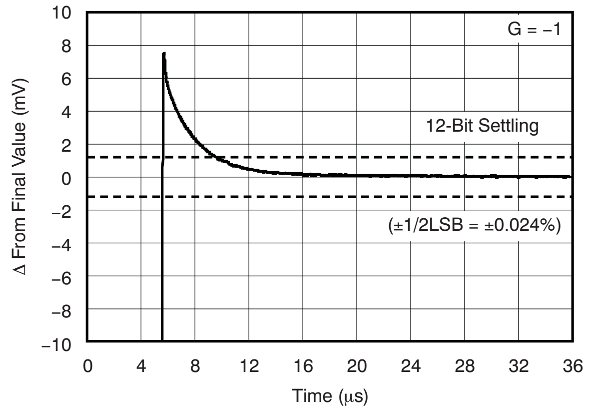


Figure 32. Large-Signal Settling Time (10-V Positive Step)

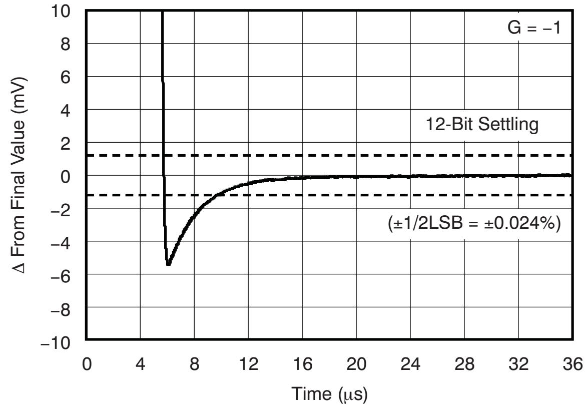


Figure 33. Large-Signal Settling Time (10-V Negative Step)

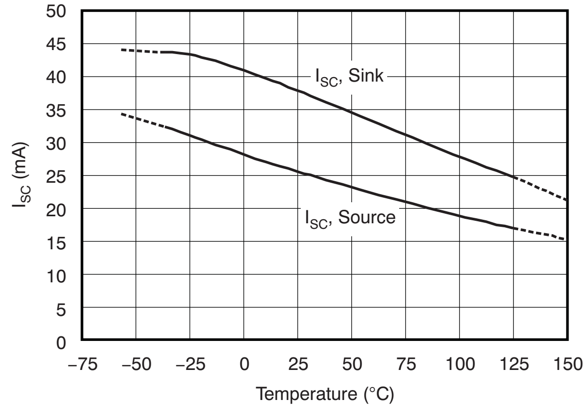


Figure 34. Short-Circuit Current vs Temperature

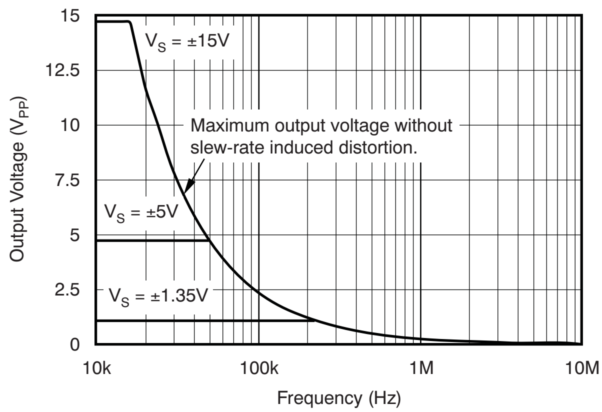


Figure 35. Maximum Output Voltage vs Frequency

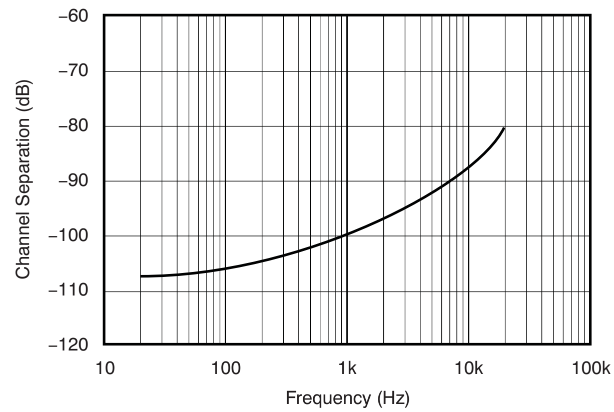


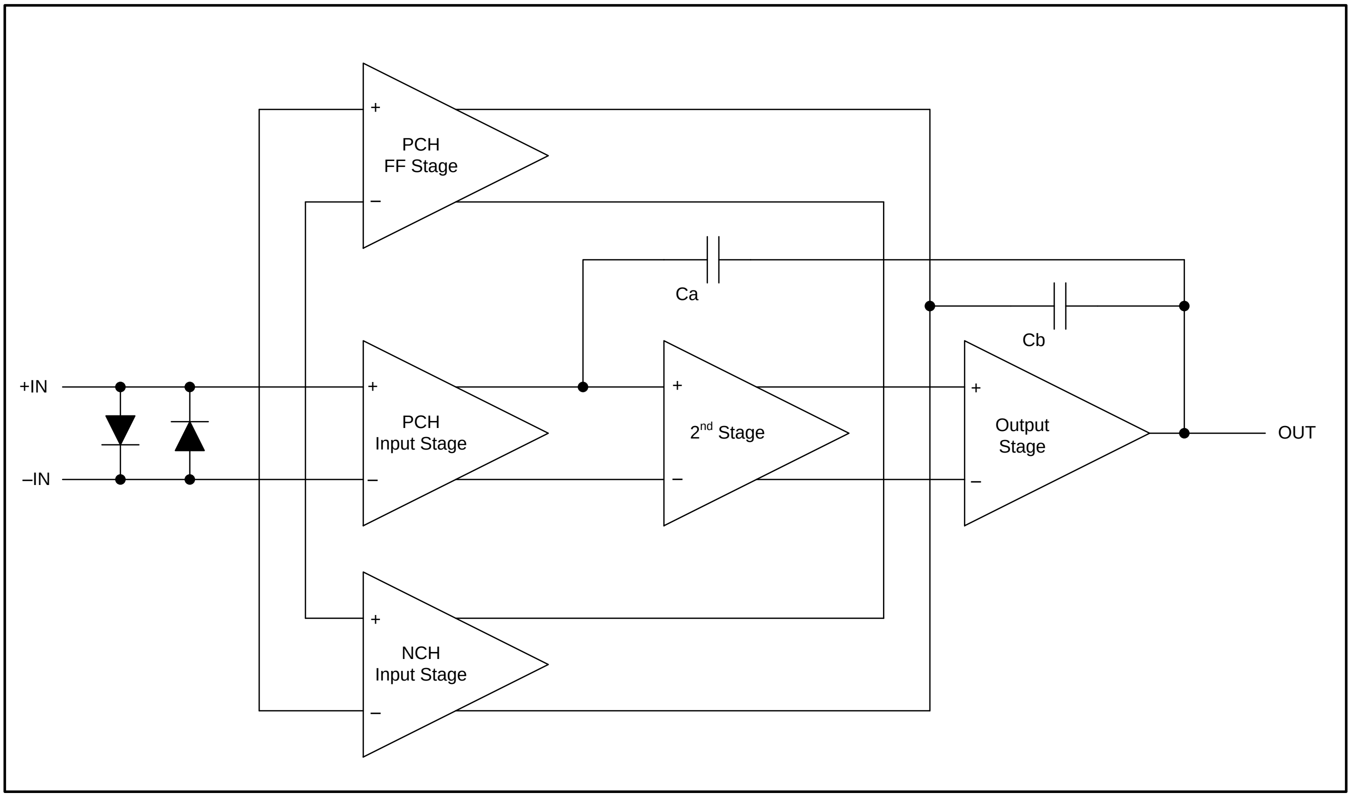
Figure 36. Channel Separation vs Frequency

7 Detailed Description

7.1 Overview

The OPA2171-EP operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPA2171-EP amplifier is specified for operation from 2.7 to 36 V (±1.35 to ±18 V). Many of the specifications apply from –55°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

7.3.2 Phase-Reversal Protection

The OPA2171-EP has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA2171-EP prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 37 shows this performance.

Feature Description (continued)

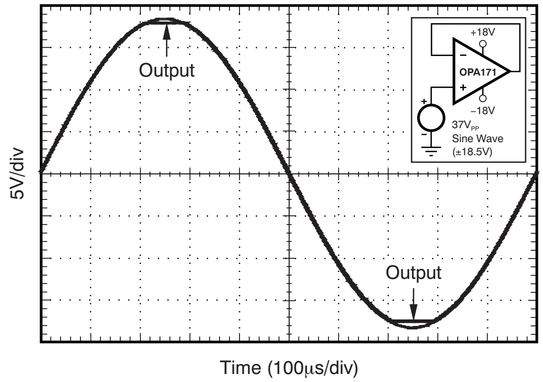


Figure 37. No Phase Reversal

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPA2171-EP extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. Table 2 summarizes the typical performance in this range.

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	**(V+) – 2**		**(V+) + 0.1**	**V**
Offset voltage		7		mV
vs Temperature		**12**		**µV/°C**
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at *f* = 1kHz		30		nV/√Hz

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Electrical Overstress

Designers often ask about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in *Absolute Maximum Ratings*. Figure 38 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

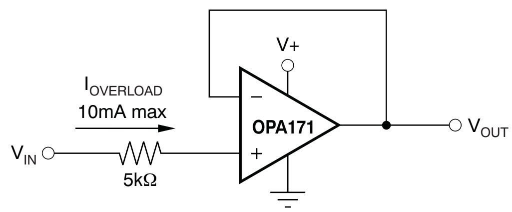


Figure 38. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins. Select the Zener voltage such that the diode does not turn on during normal operation.

However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.2 Typical Application

Figure 39 shows a capacitive load drive solution using an isolation resistor. The OPA2171-EP device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

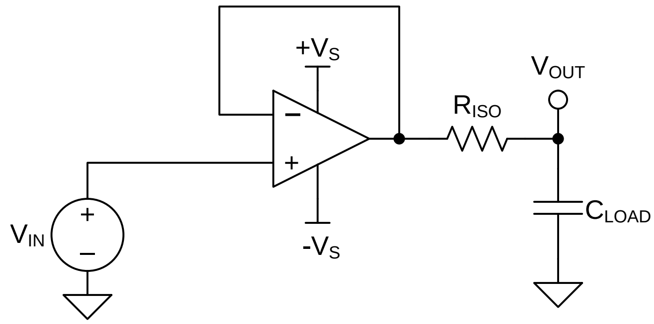


Figure 39. Unity-Gain Buffer with R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

Figure 39 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 39. Not shown in Figure 39 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade. Figure 40 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

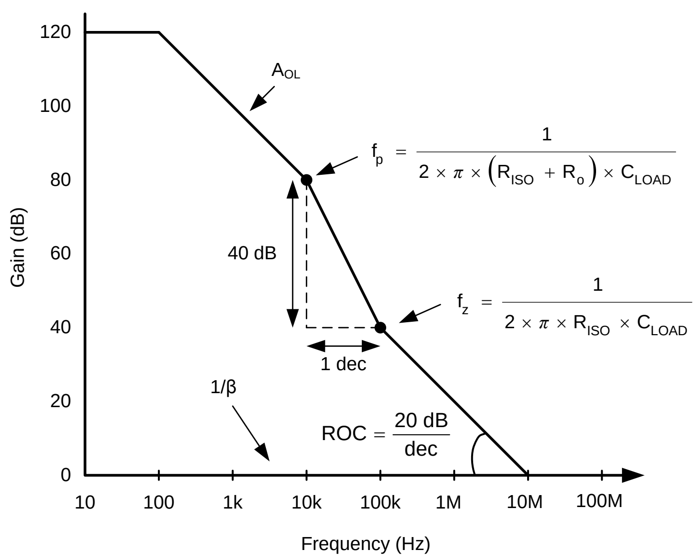


Figure 40. Unity-Gain Amplifier with R_{ISO} Compensation

Typical Application (continued)

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA171, refer to the Precision Design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.2.1 Capacitive Load and Stability

The dynamic characteristics of the OPA2171-EP have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to *Applications Bulletin AB-028* (SBOA015), available for download from www.ti.com for details of analysis techniques and application circuits.

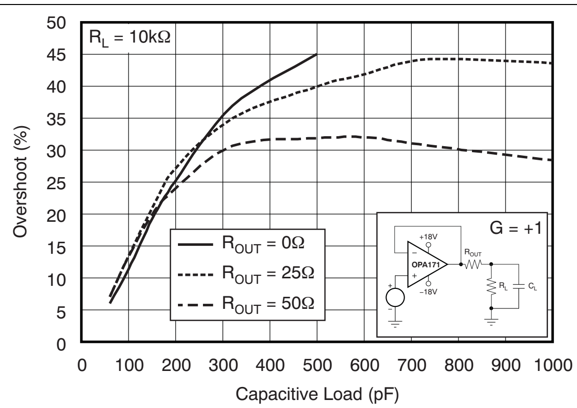


Figure 41. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

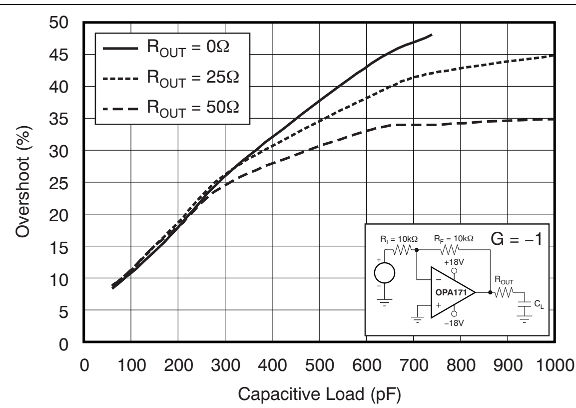


Figure 42. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.2.3 Application Curve

The OPA2171-EP device meets the supply voltage requirements of 30 V. The OPA2171-EP device was tested for various capacitive loads and R_{ISO} was adjusted to achieve an overshoot corresponding to Table 3. Figure 43 shows the test results.

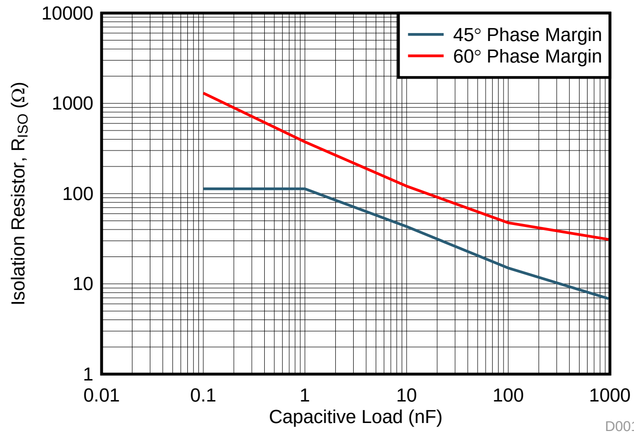


Figure 43. R_{ISO} vs C_{LOAD}

9 Power Supply Recommendations

The OPA2171-EP is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

> **CAUTION**
>
> Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the *Layout* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, TI recommends good printed circuit board (PCB) layout practices. Low-loss, 0.1-µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

10.2 Layout Example

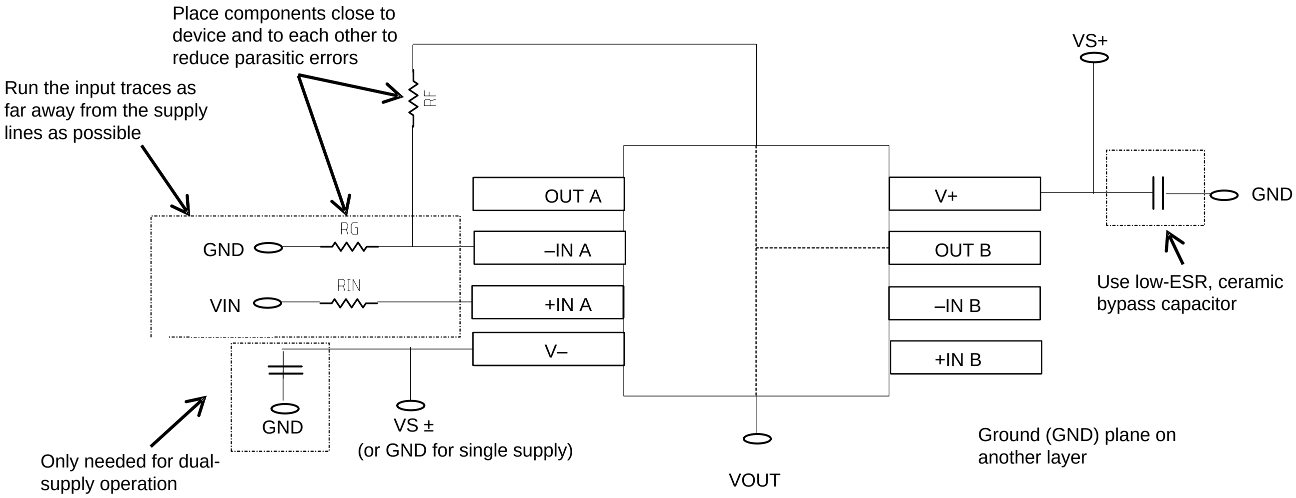


Figure 44. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2171MDCUTEP	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA	Samples
V62/15605-01XE	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

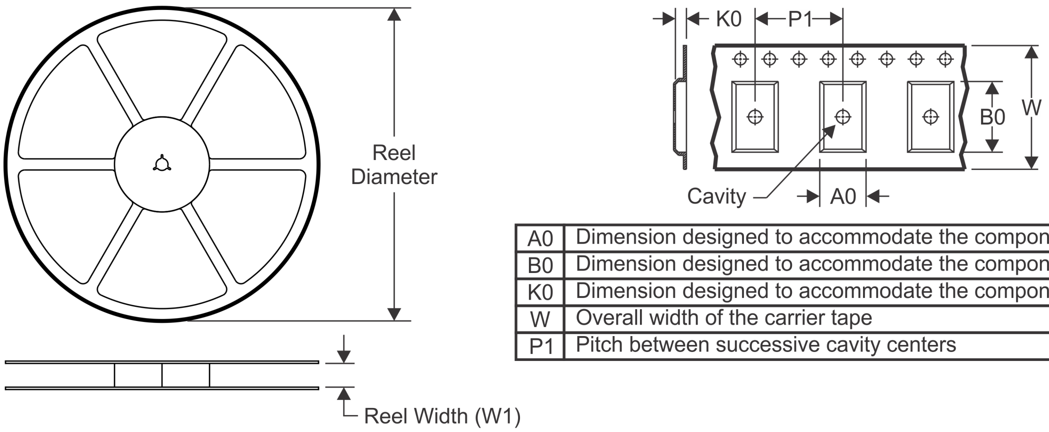
OTHER QUALIFIED VERSIONS OF OPA2171-EP :

- Catalog: OPA2171
- Automotive: OPA2171-Q1

NOTE: Qualified Version Definitions:

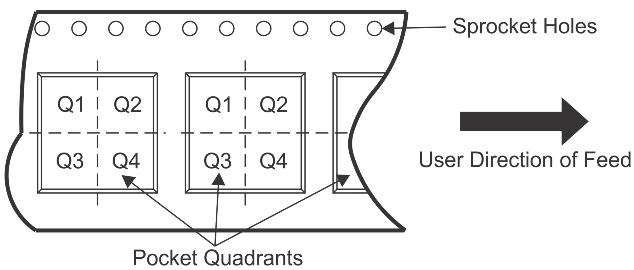
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

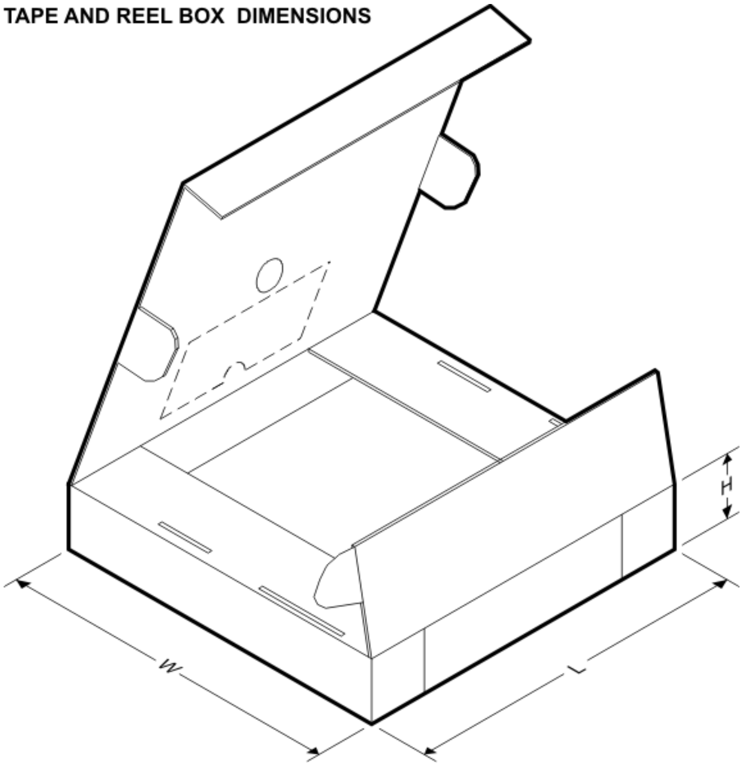
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2171MDCUTEP	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

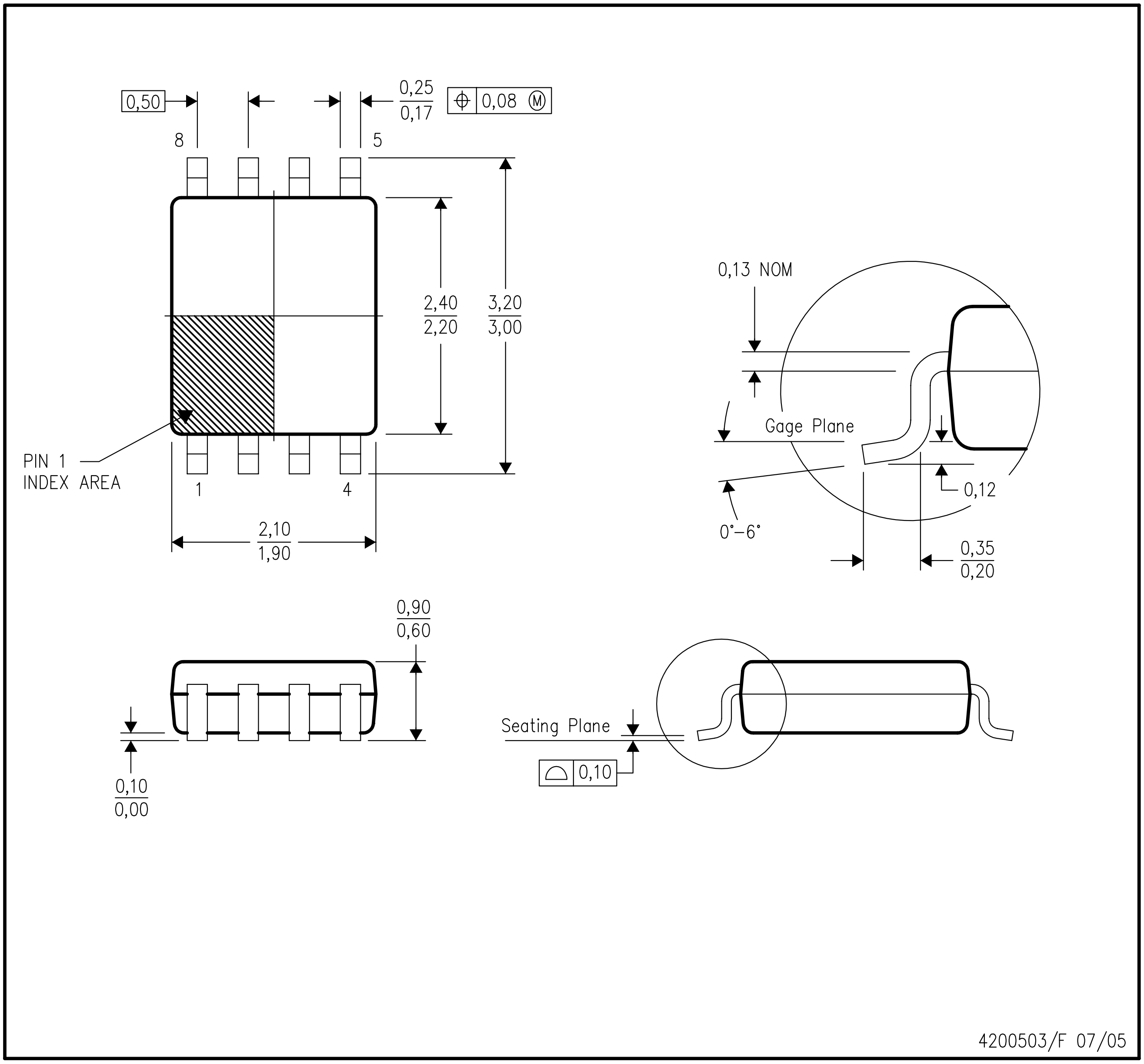
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

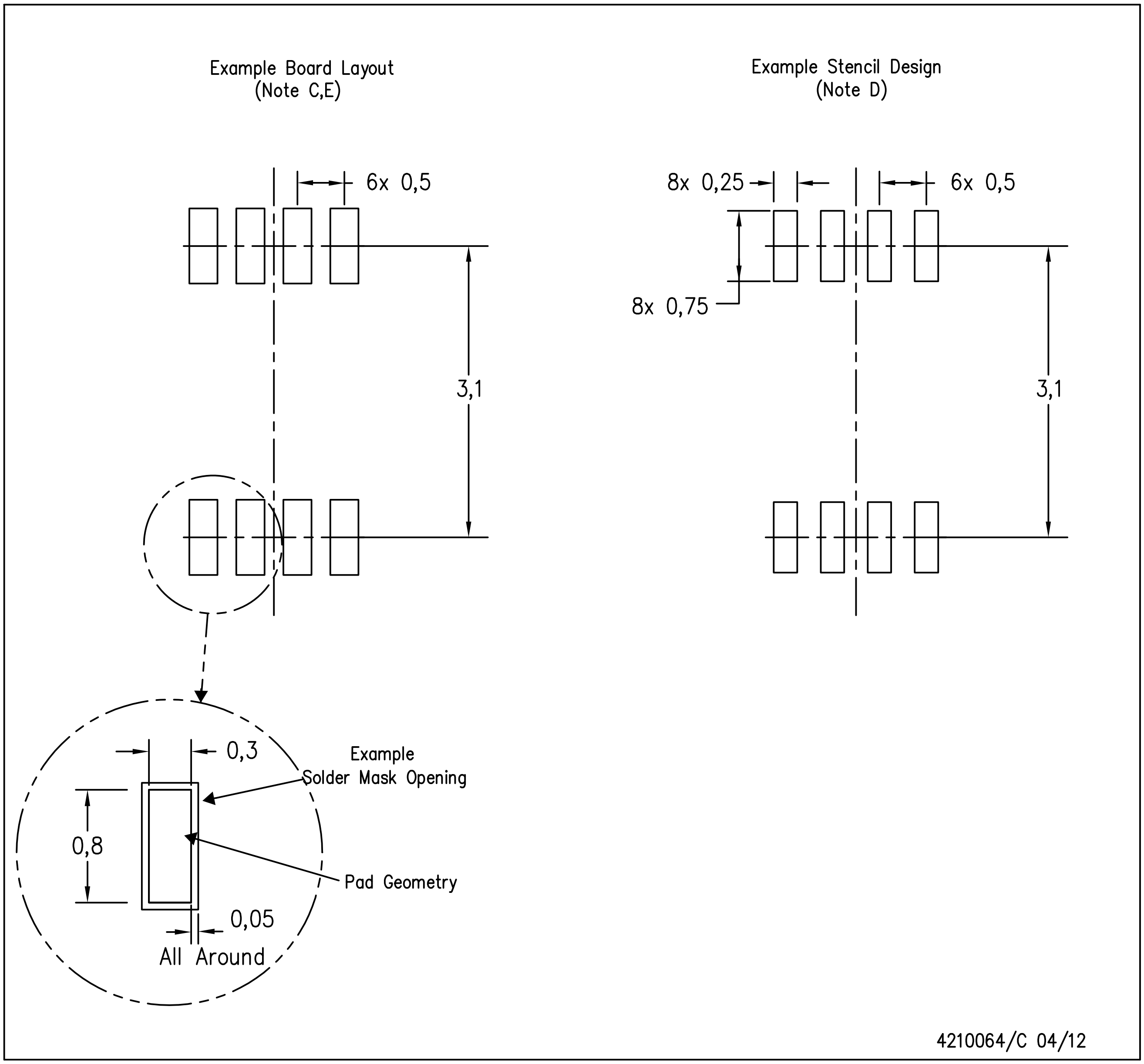
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2171MDCUTEP	VSSOP	DCU	8	250	202.0	201.0	28.0

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.