TEXAS INSTRUMENTS

**OPA170-Q1, OPA2170-Q1, OPA4170-Q1**

SBOS834 – DECEMBER 2016

# OPAx170-Q1 36-V, Single-Supply, Low-Power, Automotive Grade Operational Amplifiers

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C
    Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C5
- Supply Range: 2.7 V to 36 V, ±1.35 V to ±18 V
- Low Noise: 19 nV/$\sqrt{\text{Hz}}$
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 1.2 MHz
- Low Quiescent Current: 110 µA per Amplifier
- High Common-Mode Rejection: 120 dB
- Low Bias Current: 15 pA (Maximum)
- Number of Channels:
  - OPA170-Q1: 1
  - OPA2170-Q1: 2
  - OPA4170-Q1: 4
- Industry-Standard Packages and *Micro* Packages Available

## 2 Applications

- Automotive
- HEV and EV Power Trains
- Advanced Driver Assist (ADAS)
- Automatic Climate Controls
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators

## 3 Description

The OPA170-Q1, OPA2170-Q1, and OPA4170-Q1 devices (OPAx170-Q1) are a family of 36-V, single-supply, low-noise operational amplifiers that feature micro packages with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). They offer good offset, drift, and bandwidth with low quiescent current. The single-, dual-, and quad-versions all have identical specifications for maximum design flexibility.
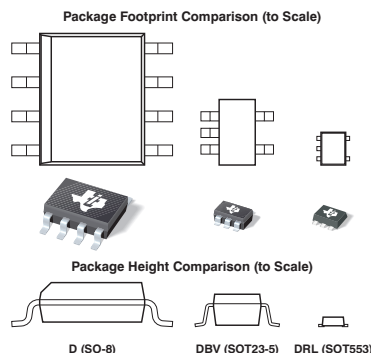
Unlike most operational amplifiers, which are specified at only one supply voltage, the OPAx170-Q1 family of operational amplifiers is specified from 2.7 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The OPAx170-Q1 family is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the positive rail for normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the positive rail, but with reduced performance within 2 V of the positive rail. The OPAx170-Q1 operational amplifiers are specified from –40°C to +125°C.

### Device Information[(1)]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA170-Q1 | SOIC (8) | 4.90 mm × 3.91 mm |
| | SOT (5) | 1.60 mm × 1.20 mm |
| | SOT-23 (5) | 2.90 mm × 1.60 mm |
| OPA2170-Q1 | SOIC (8) | 4.90 mm × 3.91 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |
| | VSSOP (8), *Micro* size | 2.30 mm × 2.00 mm |
| OPA4170-Q1 | SOIC (14) | 8.65 mm × 3.91 mm |
| | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

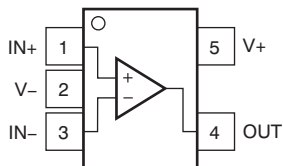**Smallest Packaging for 36-V Operational Amplifiers**



Package Footprint Comparison (to Scale)

Package Height Comparison (to Scale)

D (SO-8)          DBV (SOT23-5)          DRL (SOT553)

# Table of Contents

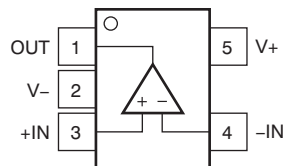# 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| December 2016 | SBOS834* | Initial release. |

# 5 Pin Configuration and Functions

**OPA170-Q1 DRL Package**
**5-Pin SOT**
**Top View**



**OPA170-Q1 DBV Package**
**5-Pin SOT-23**
**Top View**



**OPA170-Q1 D Package**
**8-Pin SOIC**
**Top View**
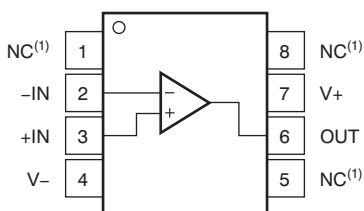


## Pin Functions: OPA170-Q1

| NAME | PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| | DRL (SOT) | DBV (SOT-23) | D (SOIC) | | |
| IN– (–IN) | 3 | 4 | 2 | I | Negative (inverting) input |
| IN+ (+IN) | 1 | 3 | 3 | I | Positive (noninverting) input |
| NC[1] | — | — | 1, 5, 8 | — | No internal connection (can be left floating) |
| OUT | 4 | 1 | 6 | O | Output |
| V– | 2 | 2 | 4 | — | Negative (lowest) power supply |
| V+ | 5 | 5 | 7 | — | Positive (highest) power supply |

(1) NC indicates no internal connection.

**OPA2170-Q1 D, DGK, and DCU Packages**
**8-Pin SOIC, VSSOP, and VSSOP (*Micro* size)**
**Top View**

```
OUT A   1        8   V+
-IN A   2        7   OUT B
+IN A   3        6   -IN B
V-      4        5   +IN B
```
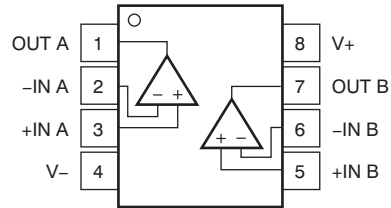
**Pin Functions: OPA2170-Q1**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V– | 4 | — | Negative (lowest) power supply |
| V+ | 8 | — | Positive (highest) power supply |

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

**OPA4170-Q1 D and PW Packages**
**14-Pin SOIC and TSSOP**
**Top View**
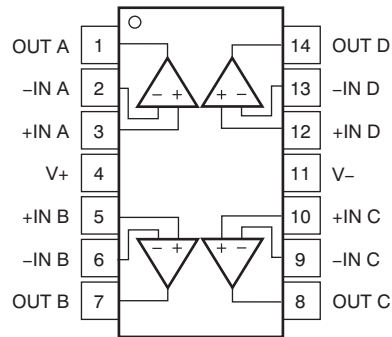


## Pin Functions: OPA4170-Q1

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| +IN C | 10 | I | Noninverting input, channel C |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) power supply |
| V+ | 4 | — | Positive (highest) power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted. [1]

|  | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage | −20 | 20 | V |
| Single supply voltage |  | 40 | V |
| Signal input pin voltage | (V−) − 0.5 | (V+) + 0.5 | V |
| Signal input pin current | −10 | 10 | mA |
| Output short-circuit current [2] | Continuous | | |
| Operating ambient temperature, $T_A$ | −55 | 150 | °C |
| Junction temperature, $T_J$ |  | 150 | °C |
| Storage temperature, $T_{stg}$ | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 [1] | ±4000 | V |
|  |  | Charged-device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage (V+ − V−) | 2.7 | 36 | V |
| $T_A$ | Operating temperature | −40 | 125 | °C |

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

## 6.4 Thermal Information: OPA170-Q1

| THERMAL METRIC[1] | OPA170-Q1 | | | UNIT |
| --- | --- | --- | --- | --- |
| | D (SOIC) | DBV (SOT-23) | DRL (SOT) | |
| | 8 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 149.5 | 245.8 | 208.1 | °C/W |
| $R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance | 97.9 | 133.9 | 0.1 | °C/W |
| $R_{\theta JB}$ Junction-to-board thermal resistance | 87.7 | 83.6 | 42.4 | °C/W |
| $\psi_{JT}$ Junction-to-top characterization parameter | 35.5 | 18.2 | 0.5 | °C/W |
| $\psi_{JB}$ Junction-to-board characterization parameter | 89.5 | 83.1 | 42.2 | °C/W |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1)   For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

## 6.5 Thermal Information: OPA2170-Q1

| THERMAL METRIC[1] | OPA2170-Q1 | | | UNIT |
| --- | --- | --- | --- | --- |
| | D (SOIC) | DCU (VSSOP) | DGK (VSSOP) | |
| | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 134.3 | 175.2 | 180 | °C/W |
| $R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance | 72.1 | 74.9 | 55 | °C/W |
| $R_{\theta JB}$ Junction-to-board thermal resistance | 60.6 | 22.2 | 130 | °C/W |
| $\psi_{JT}$ Junction-to-top characterization parameter | 18.2 | 1.6 | 5.3 | °C/W |
| $\psi_{JB}$ Junction-to-board characterization parameter | 53.8 | 22.8 | 120 | °C/W |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1)   For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

## 6.6 Thermal Information: OPA4170-Q1

| THERMAL METRIC[1] | OPA4170-Q1 | | UNIT |
| --- | --- | --- | --- |
| | D (SOIC) | PW (TSSOP) | |
| | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 93.2 | 106.9 | °C/W |
| $R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance | 51.8 | 24.4 | °C/W |
| $R_{\theta JB}$ Junction-to-board thermal resistance | 49.4 | 59.3 | °C/W |
| $\psi_{JT}$ Junction-to-top characterization parameter | 13.5 | 0.6 | °C/W |
| $\psi_{JB}$ Junction-to-board characterization parameter | 42.2 | 54.3 | °C/W |
| $R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1)   For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics (SPRA953).

## 6.7 Electrical Characteristics

at $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2 (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C | | 0.25 | ±1.8 | mV |
| | | $T_A$ = −40°C to 125°C | | | ±2 | mV |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_A$ = −40°C to 125°C | | ±0.3 | ±2 | µV/°C |
| PSRR | Input offset voltage vs power supply | $V_S$ = 4 V to 36 V, $T_A$ = −40°C to 125°C | | 1 | ±5 | µV/V |
| | Channel separation, dc | | | 5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | ±8 | ±15 | pA |
| | | $T_A$ = −40°C to 125°C | | | ±3.5 | nA |
| $I_{OS}$ | Input offset current | $T_A$ = 25°C | | ±4 | ±15 | pA |
| | | $T_A$ = −40°C to 125°C | | | ±3.5 | nA |
| **NOISE** | | | | | | |
| | Input voltage noise | $f$ = 0.1 Hz to 10 Hz | | 2 | | µV$_{PP}$ |
| $e_n$ | Input voltage noise density | $f$ = 100 Hz | | 22 | | nV/√Hz |
| | | $f$ = 1 kHz | | 19 | | nV/√Hz |
| **INPUT VOLTAGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range[(1)] | | (V−) − 0.1 | | (V+) − 2 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = ±2 V, (V−) - 0.1 V < $V_{CM}$ < (V+) - 2 V, $T_A$ = −40°C to 125°C | 90 | 104 | | dB |
| | | $V_S$ = ±18 V, (V−) - 0.1 V < $V_{CM}$ < (V+) - 2 V, $T_A$ = −40°C to 125°C | 104 | 120 | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| | Differential | | | 100 ‖ 3 | | MΩ ‖ pF |
| | Common-mode | | | 6 ‖ 3 | | $10^{12}$ Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 4 V to 36 V, (V−) + 0.35 V < $V_O$ < (V+) - 0.35 V, $T_A$ = −40°C to 125°C | 110 | 130 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| GBP | Gain bandwidth product | | | 1.2 | | MHz |
| SR | Slew rate | G = +1 | | 0.4 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = ±18 V, G = +1, 10-V step | | 20 | | µs |
| | | To 0.01% (12-bit), $V_S$ = ±18 V, G = +1, 10-V step | | 28 | | µs |
| | Overload recovery time | $V_{IN}$ × Gain > $V_S$ | | 2 | | µs |
| THD+N | Total harmonic distortion + noise | G = 1, $f$ = 1 kHz, $V_O$ = 3 V$_{RMS}$ | | 0.0002% | | |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from positive rail | $I_L$ = 0 mA, $V_S$ = 4 V to 36 V | 10 | | | mV |
| | | $I_L$ sourcing 1 mA, $V_S$ = 4 V to 36 V | 115 | | | mV |
| $V_O$ | Voltage output swing from negative rail | $I_L$ = 0 mA, $V_S$ = 4 V to 36 V | | | 8 | mV |
| | | $I_L$ sinking 1 mA, $V_S$ = 4 V to 36 V | | | 70 | mV |
| $V_O$ | Voltage output swing from rail | $V_S$ = 5 V, $R_L$ = 10 kΩ; $T_A$ = −40°C to 125°C | (V−) + 0.03 | | (V+) − 0.05 | V |
| | | $R_L$ = 10 kΩ, $A_{OL}$ ≥ 110 dB, $T_A$ = −40°C to 125°C | (V−) + 0.35 | | (V+) − 0.35 | V |
| $I_{SC}$ | Short-circuit current | | −20 | | 17 | mA |
| $C_{LOAD}$ | Capacitive load drive | | | See *Typical Characteristics* | | pF |
| $R_O$ | Open-loop output resistance | $f$ = 1 MHz, $I_O$ = 0 A | | 900 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 2.7 | | 36 | V |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A; $T_A$ = 25°C | | 110 | 145 | µA |
| | | $I_O$ = 0 A; $T_A$ = −40°C to 125°C | | | 155 | µA |
| **TEMPERATURE** | | | | | | |
| | Specified range | | −40 | | 125 | °C |
| | Operating range | | −55 | | 150 | °C |

(1) The input range can be extended beyond (V+) − 2 V up to V+. See the *Typical Characteristics* and *Application and Implementation* sections for additional information.

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

## 6.8 Typical Characteristics: Table of Graphs

### Table 1. Characteristic Performance Measurements

| DESCRIPTION | FIGURE |
|---|---|
| Offset Voltage Production Distribution | Figure 1 |
| Offset Voltage Drift Distribution | Figure 2 |
| Offset Voltage vs Temperature | Figure 3 |
| Offset Voltage vs Common-Mode Voltage | Figure 4 |
| Offset Voltage vs Common-Mode Voltage (Upper Stage) | Figure 5 |
| Offset Voltage vs Power Supply | Figure 6 |
| $I_B$ and $I_{OS}$ vs Common-Mode Voltage | Figure 7 |
| Input Bias Current vs Temperature | Figure 8 |
| Output Voltage Swing vs Output Current (Maximum Supply) | Figure 9 |
| CMRR and PSRR vs Frequency (Referred-to-Input) | Figure 10 |
| CMRR vs Temperature | Figure 11 |
| PSRR vs Temperature | Figure 12 |
| 0.1-Hz to 10-Hz Noise | Figure 13 |
| Input Voltage Noise Spectral Density vs Frequency | Figure 14 |
| THD+N Ratio vs Frequency | Figure 15 |
| THD+N vs Output Amplitude | Figure 16 |
| Quiescent Current vs Temperature | Figure 17 |
| Quiescent Current vs Supply Voltage | Figure 18 |
| Open-Loop Gain and Phase vs Frequency | Figure 19 |
| Closed-Loop Gain vs Frequency | Figure 20 |
| Open-Loop Gain vs Temperature | Figure 21 |
| Open-Loop Output Impedance vs Frequency | Figure 22 |
| Small-Signal Overshoot vs Capacitive Load (100-mV Output Step) | Figure 23, Figure 24 |
| No Phase Reversal | Figure 25 |
| Positive Overload Recovery | Figure 26 |
| Negative Overload Recovery | Figure 27 |
| Small-Signal Step Response (100 mV) | Figure 28, Figure 29 |
| Large-Signal Step Response | Figure 30, Figure 31 |
| Large-Signal Settling Time (10-V Positive Step) | Figure 32 |
| Large-Signal Settling Time (10-V Negative Step) | Figure 33 |
| Short-Circuit Current vs Temperature | Figure 34 |
| Maximum Output Voltage vs Frequency | Figure 35 |
| EMIRR IN+ vs Frequency | Figure 36 |

## 6.9 Typical Characteristics

$V_S = \pm 18$ V, $V_{CM} = V_S / 2$, $R_{LOAD} = 10$ kΩ connected to $V_S / 2$, and $C_L = 100$ pF, unless otherwise noted.
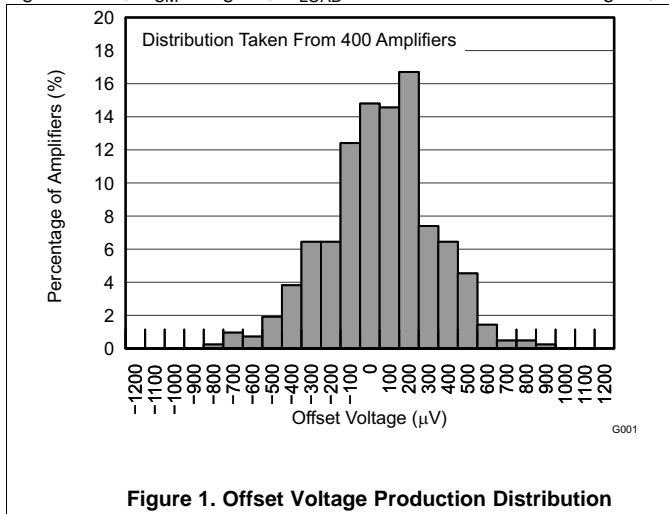


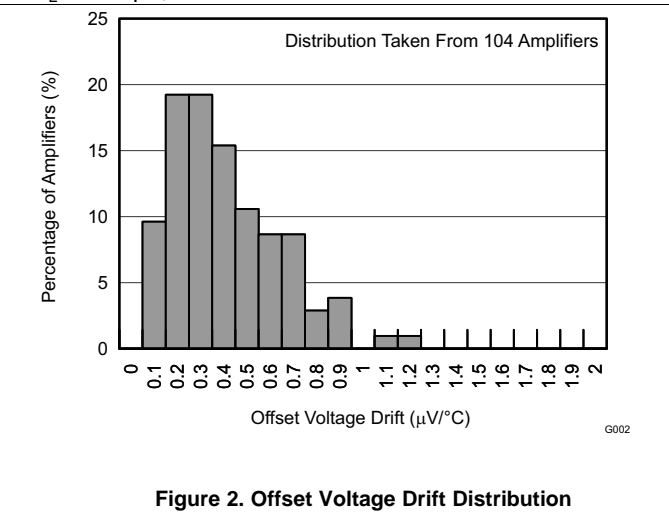**Figure 1. Offset Voltage Production Distribution**



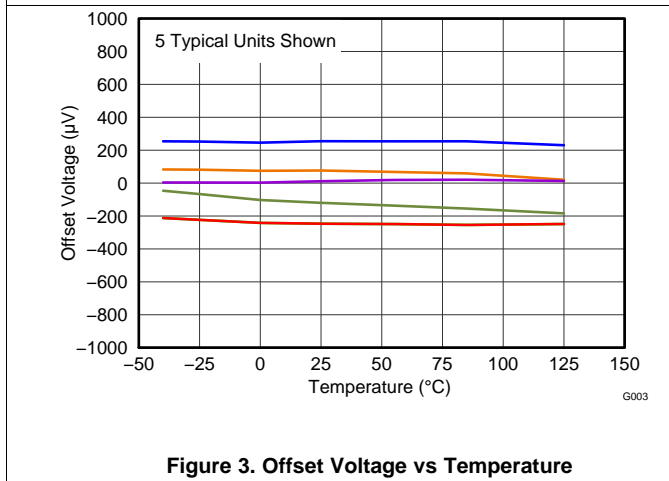**Figure 2. Offset Voltage Drift Distribution**
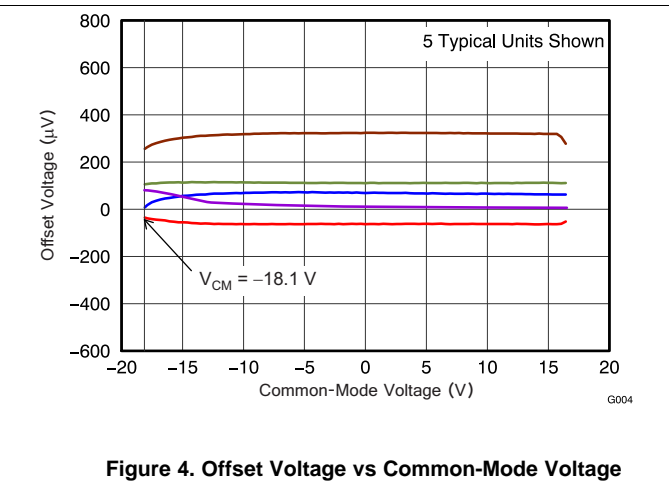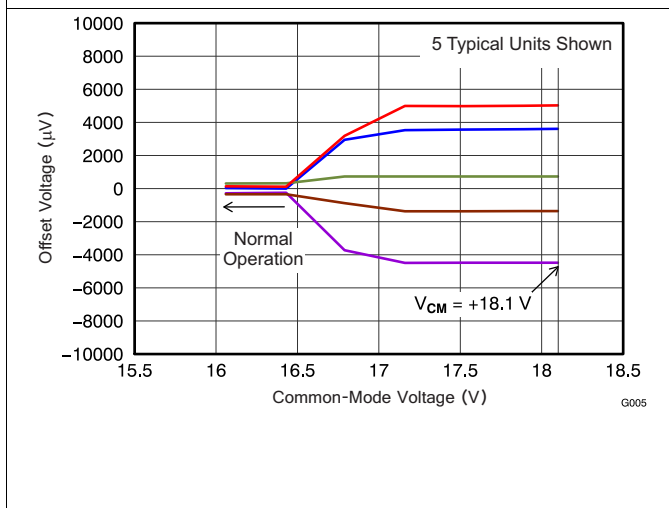


**Figure 3. Offset Voltage vs Temperature**



**Figure 4. Offset Voltage vs Common-Mode Voltage**



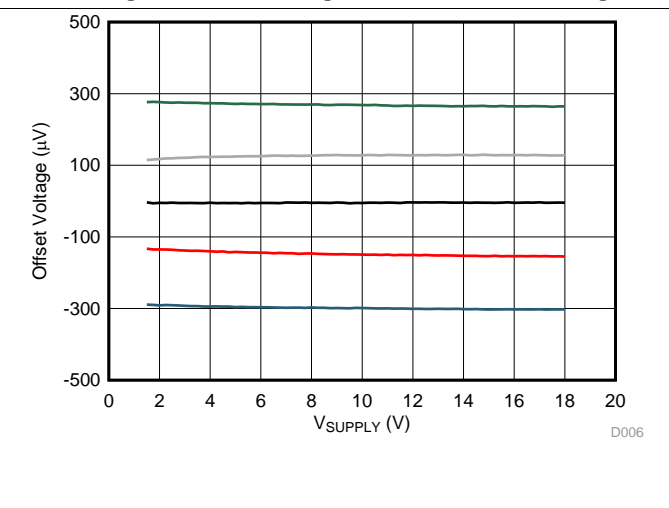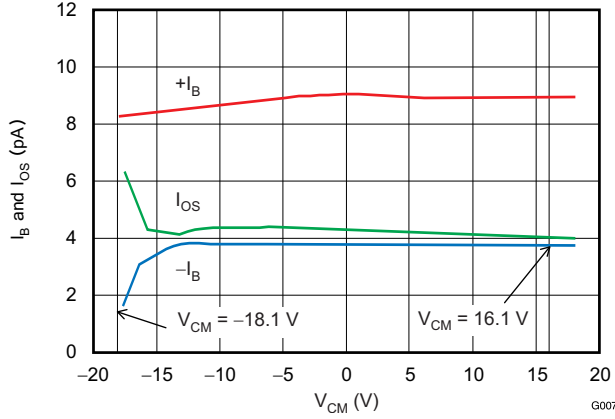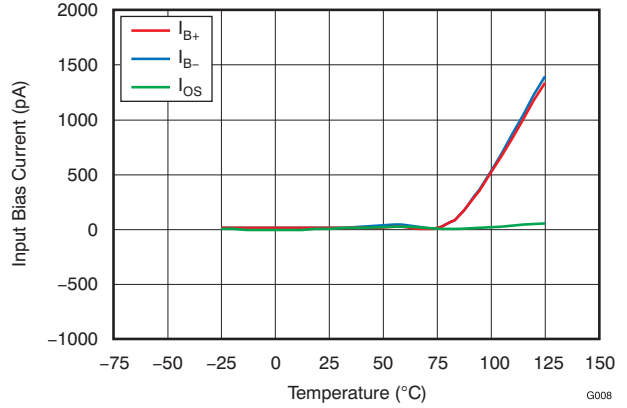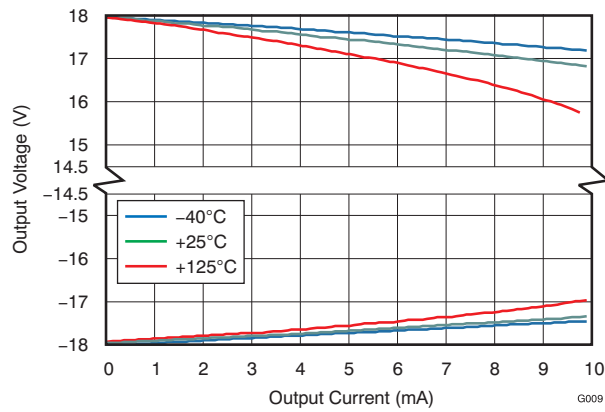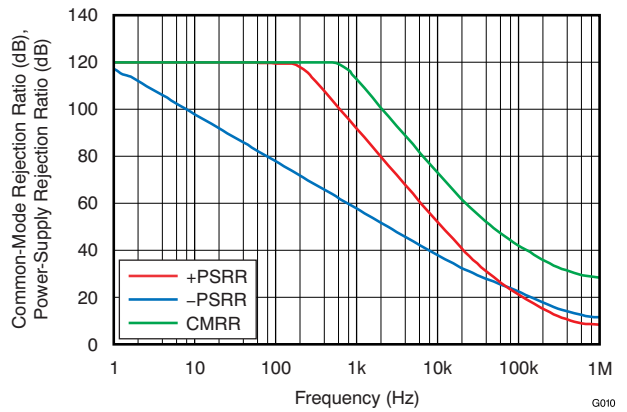**Figure 5. Offset Voltage vs Common-Mode Voltage
(Upper Stage)**



**Figure 6. Offset Voltage vs Power Supply**

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

Figure 7. I$_B$ and I$_{OS}$ vs Common-Mode Voltage



Figure 8. Input Bias Current vs Temperature



Figure 9. Output Voltage Swing vs Output Current
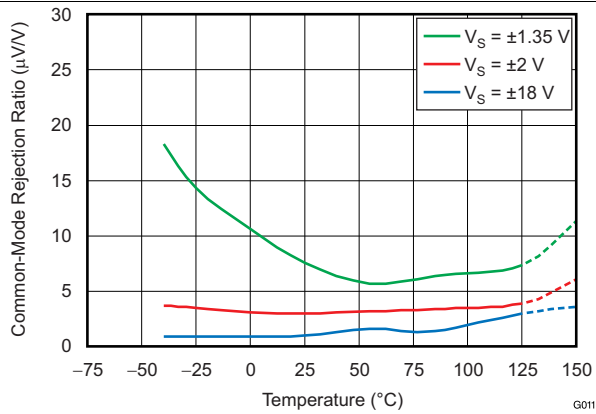(Maximum Supply)



Figure 10. CMRR and PSRR vs Frequency
(Referred to Input)
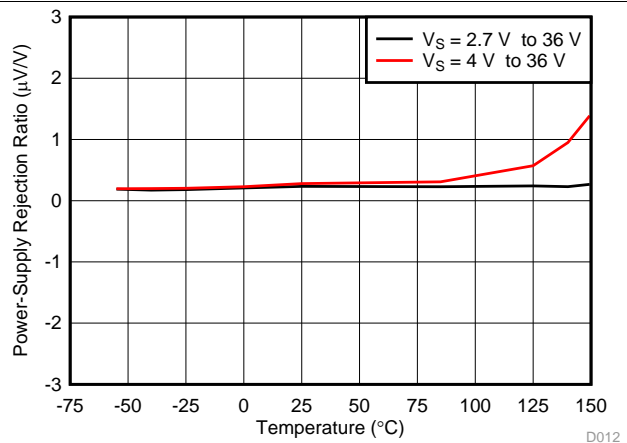


Figure 11. CMRR vs Temperature



Figure 12. PSRR vs Temperature

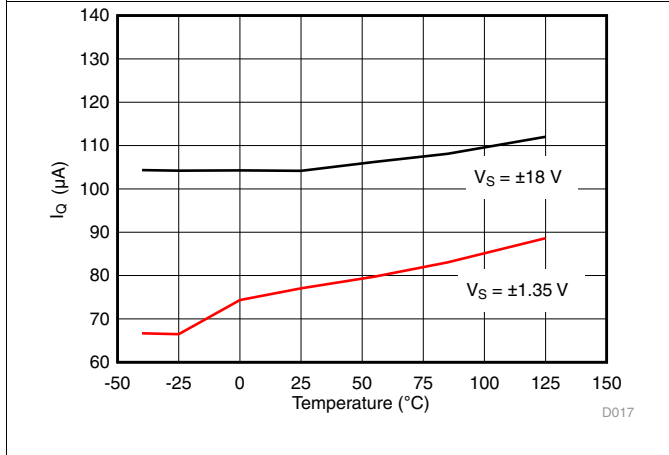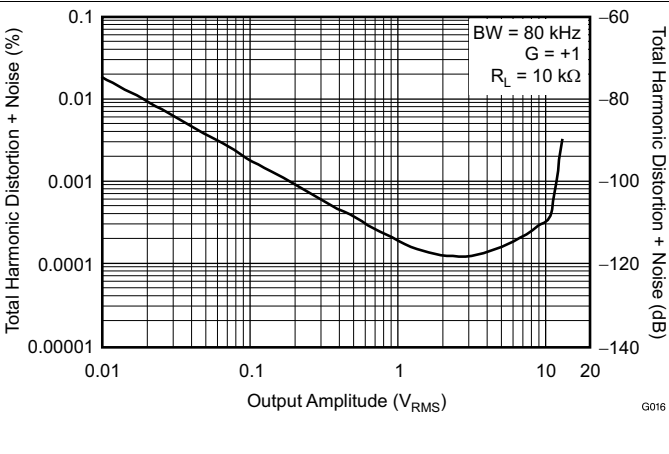Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

**Figure 13. 0.1-Hz to 10-Hz Noise**



**Figure 14. Input Voltage Noise Spectral Density vs Frequency**



**Figure 15. THD + N Ratio vs Frequency**



**Figure 16. THD + N vs Output Amplitude**



**Figure 17. Quiescent Current vs Temperature**



**Figure 18. Quiescent Current vs Supply Voltage**
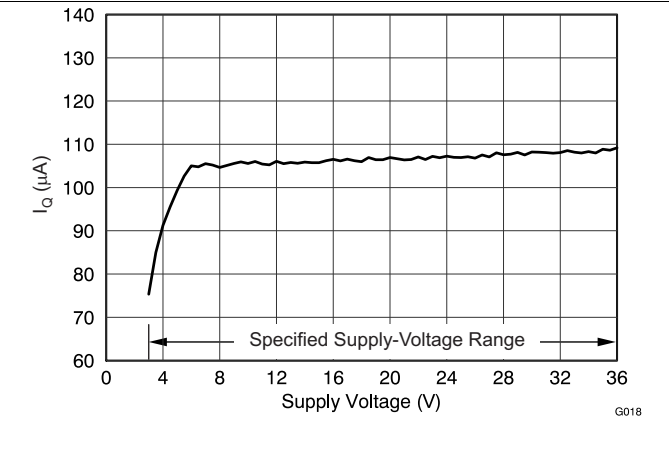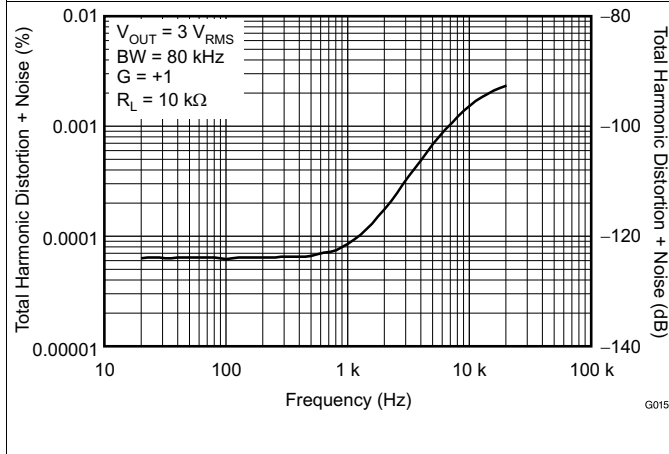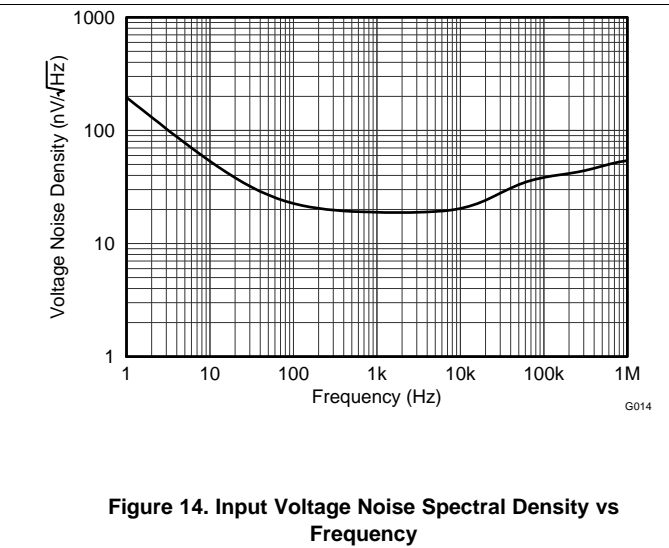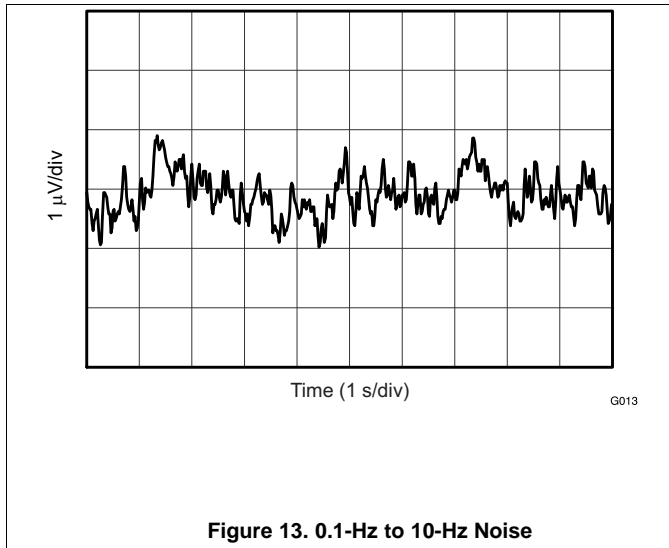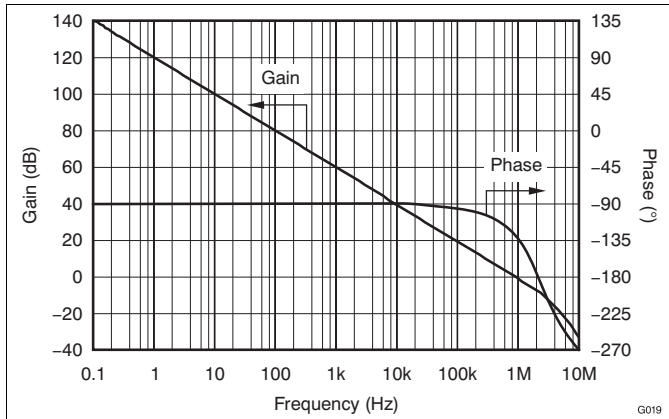
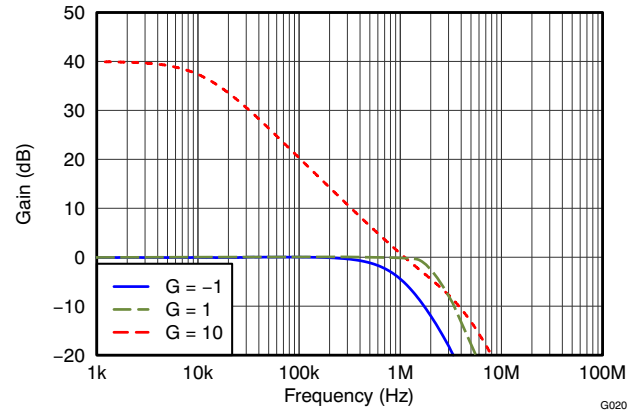**Figure 19. Open-Loop Gain and Phase vs Frequency**



**Figure 20. Closed-Loop Gain vs Frequency**
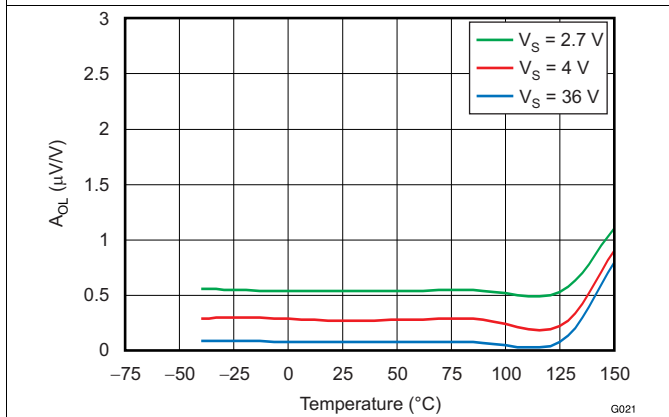


**Figure 21. Open-Loop Gain vs Temperature**
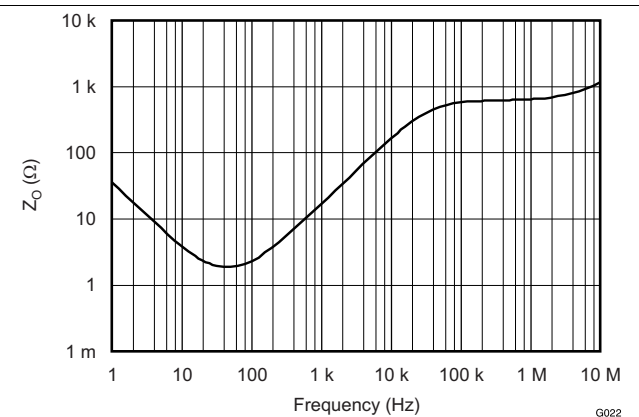


**Figure 22. Open-Loop Output Impedance vs Frequency**



100-mV output step
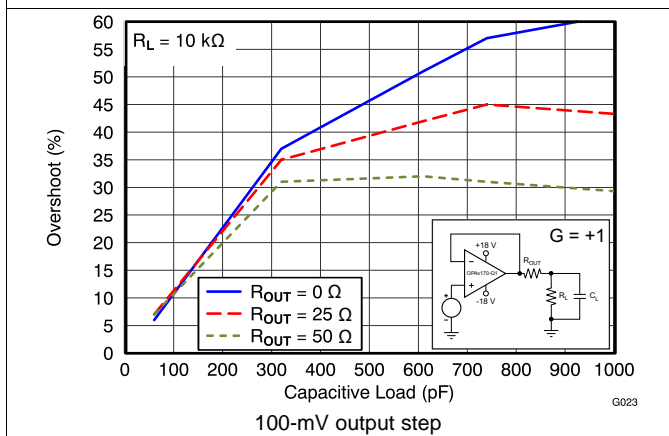
**Figure 23. Small-Signal Overshoot vs Capacitive Load**



100-mV output step
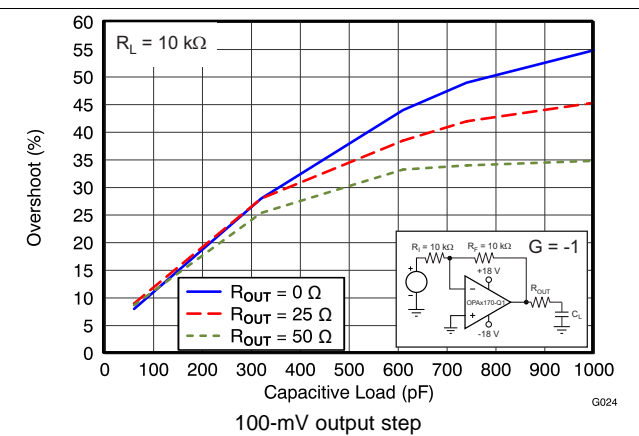
**Figure 24. Small-Signal Overshoot vs Capacitive Load**

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*
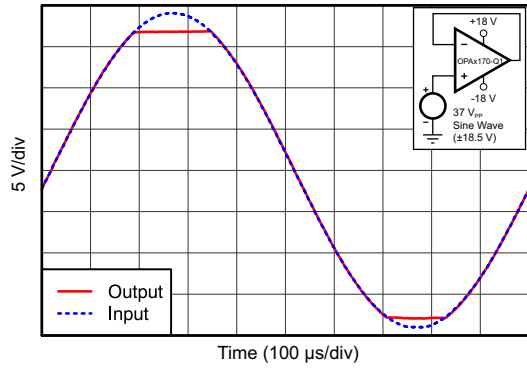
**Figure 25. No Phase Reversal**
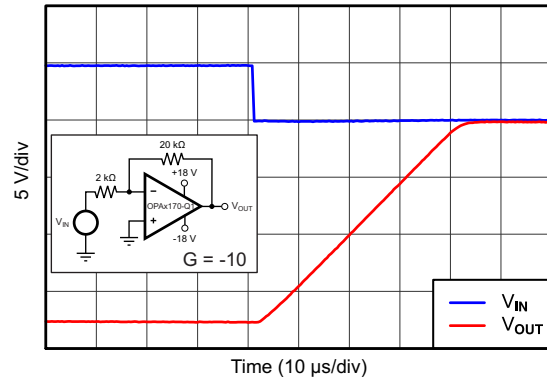


**Figure 26. Positive Overload Recovery**
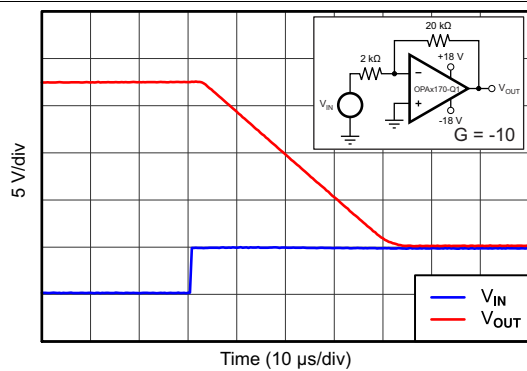


**Figure 27. Negative Overload Recovery**
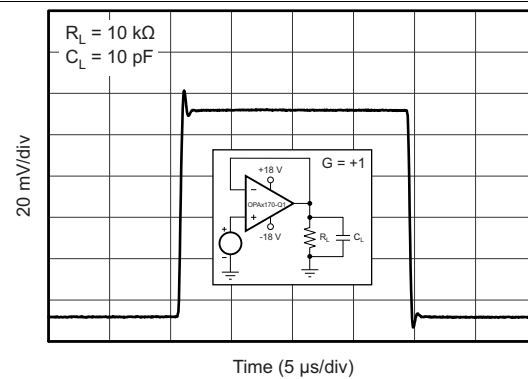


**Figure 28. Small-Signal Step Response (100-mV)**
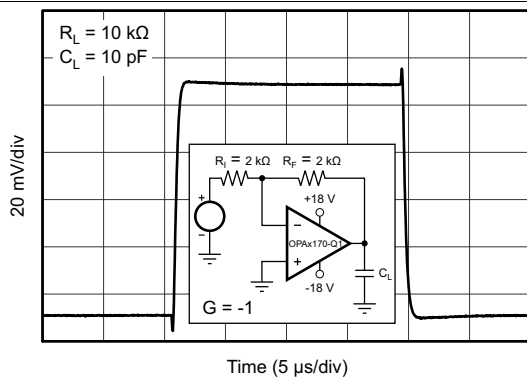


**Figure 29. Small-Signal Step Response (100-mV)**
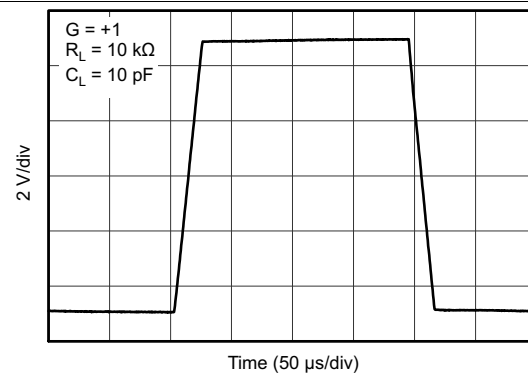


**Figure 30. Large-Signal Step Response**
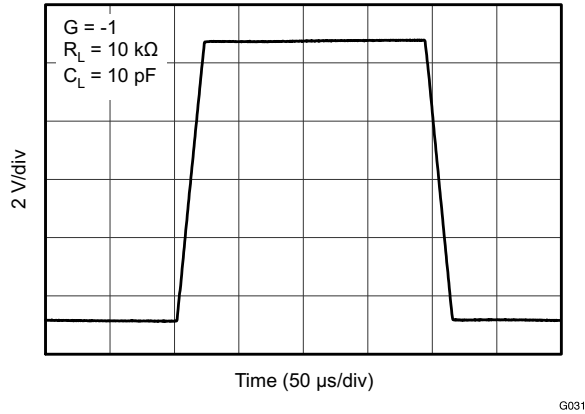
Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

**Figure 31. Large-Signal Step Response**



10-V positive step

**Figure 32. Large-Signal Settling Time**



10-V negative step
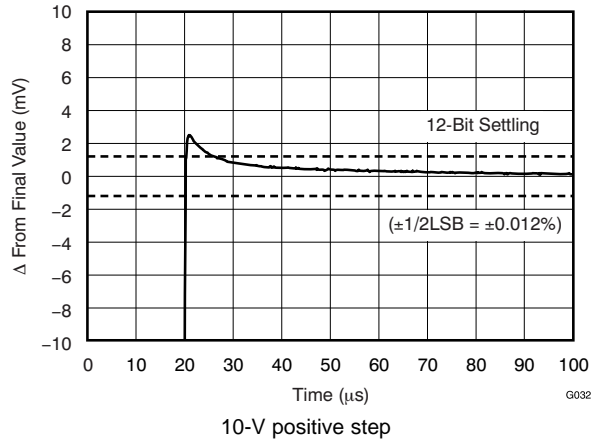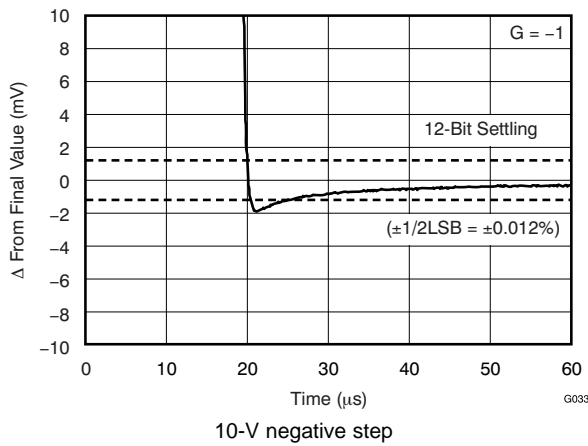
**Figure 33. Large-Signal Settling Time**



10-V negative step
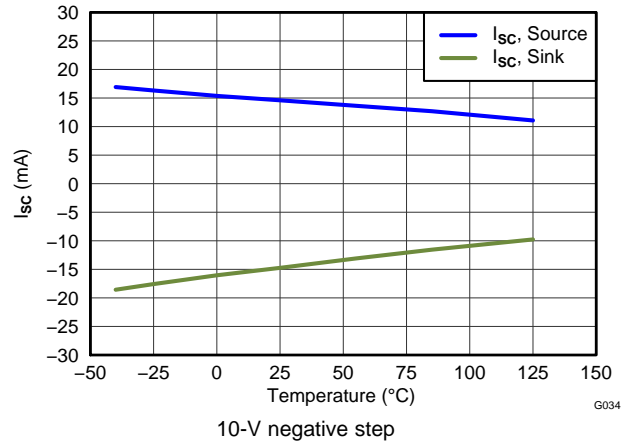
**Figure 34. Short-Circuit Current vs Temperature**
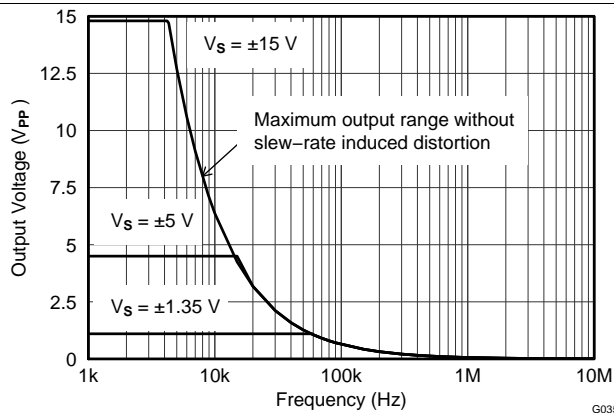


**Figure 35. Maximum Output Voltage vs Frequency**
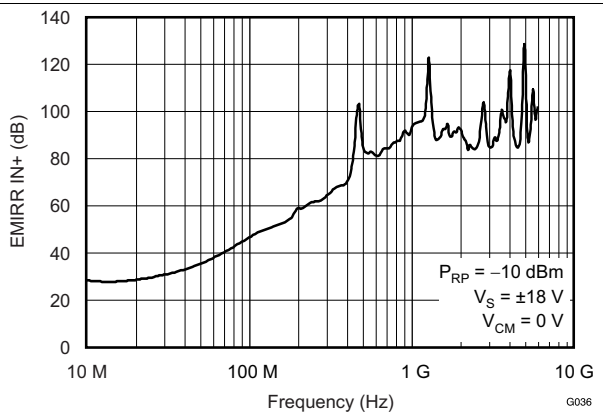


**Figure 36. EMIRR IN+ vs Frequency**

# 7 Detailed Description

## 7.1 Overview

The OPAx170-Q1 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2 $\mu$V/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and $A_{OL}$.

## 7.2 Functional Block Diagram
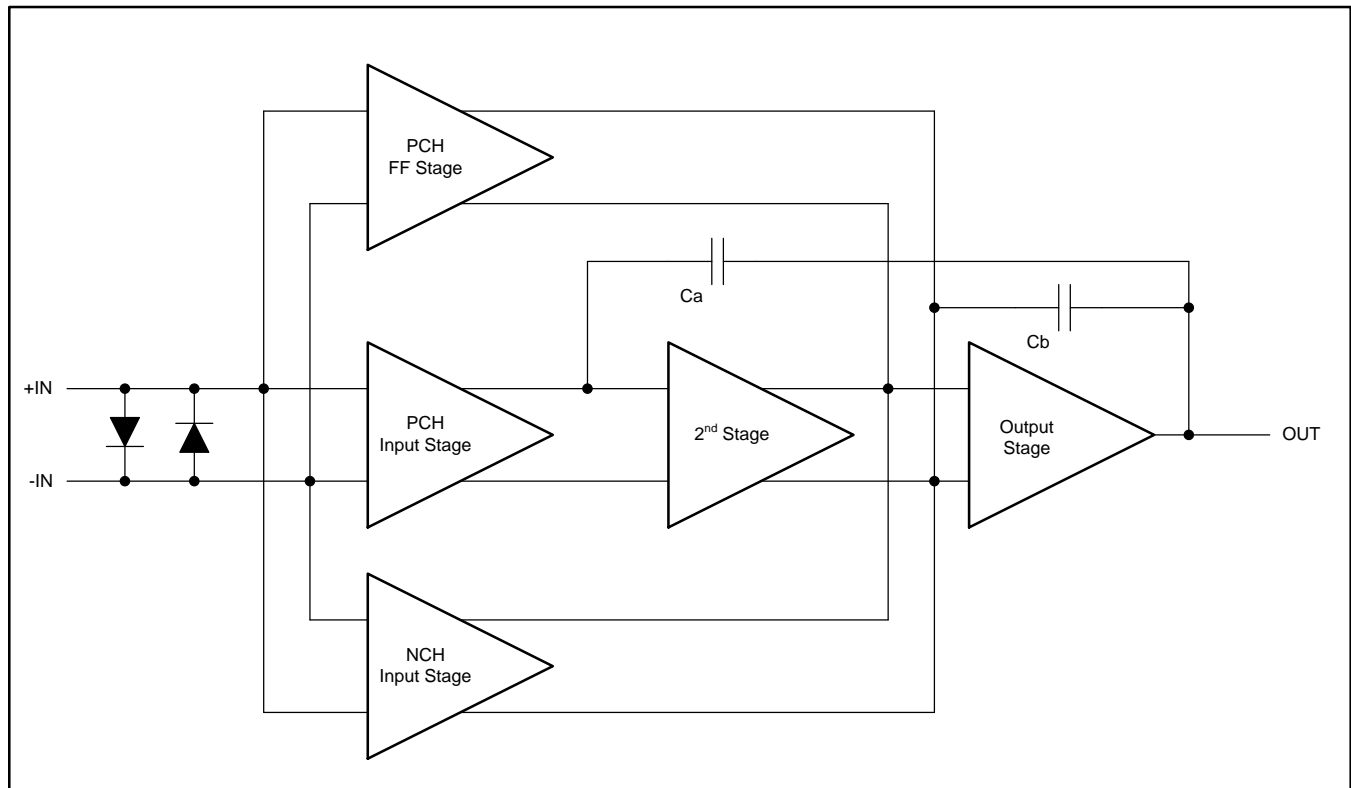


## 7.3 Feature Description

### 7.3.1 Operating Characteristics

The OPAx170-Q1 family of amplifiers is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are listed in *Table 1*.

# Feature Description (continued)

## 7.3.2  Phase-Reversal Protection

The OPAx170-Q1 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx170-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 37 shows this performance.
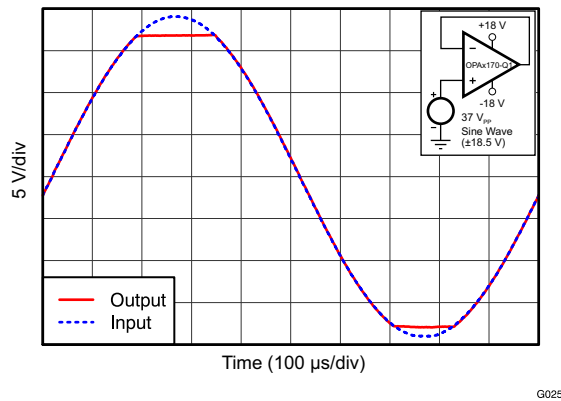


**Figure 37.  No Phase Reversal**

## 7.3.3  Electrical Overstress

Designers typically ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions typically focus on the device inputs, but may involve the supply voltage pins or the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of basic ESD circuitry and the relevance of the circuitry to an electrical overstress event is helpful. Figure 38 illustrates the ESD circuits (indicated by the dashed line area) in the OPAx170-Q1. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

## Feature Description (continued)
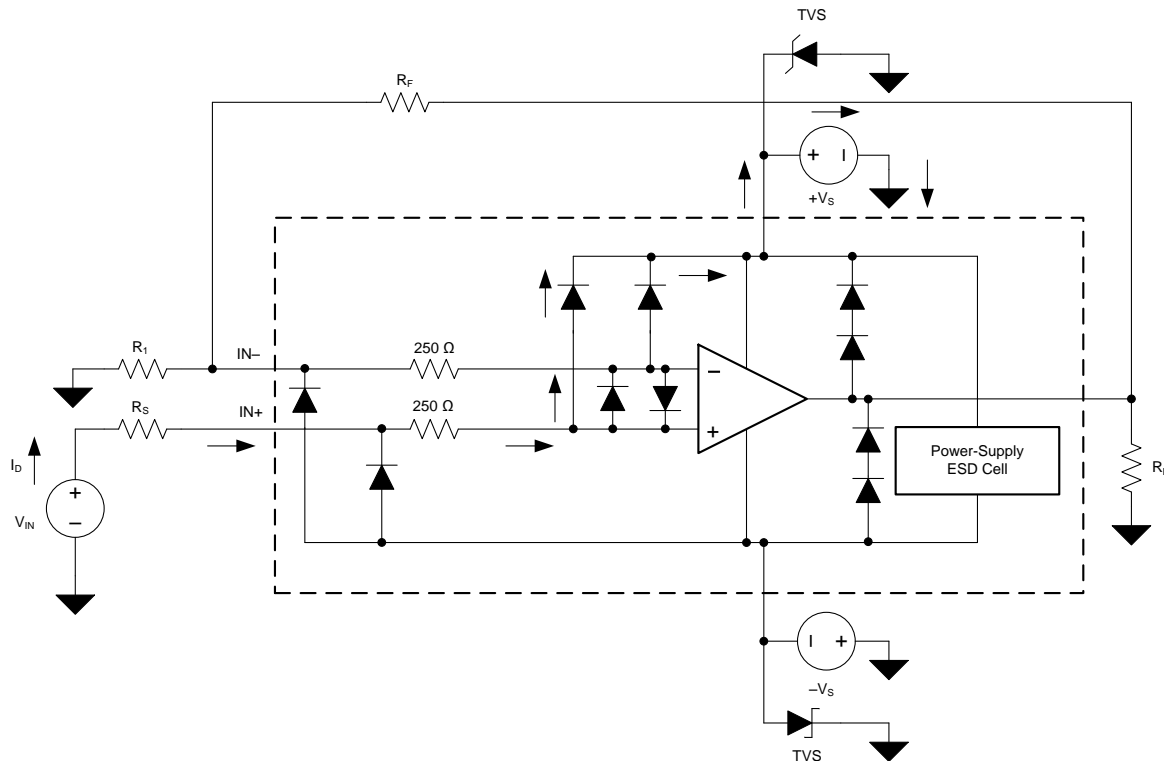


**Figure 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. The absorption device can activate depending on the path of the current. The absorption device has a trigger (or threshold voltage) that is above the normal operating voltage of the OPAx170-Q1, but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see Figure 38), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 38 shows a specific example where the input voltage ($V_{IN}$) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, $V_{IN}$ can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.
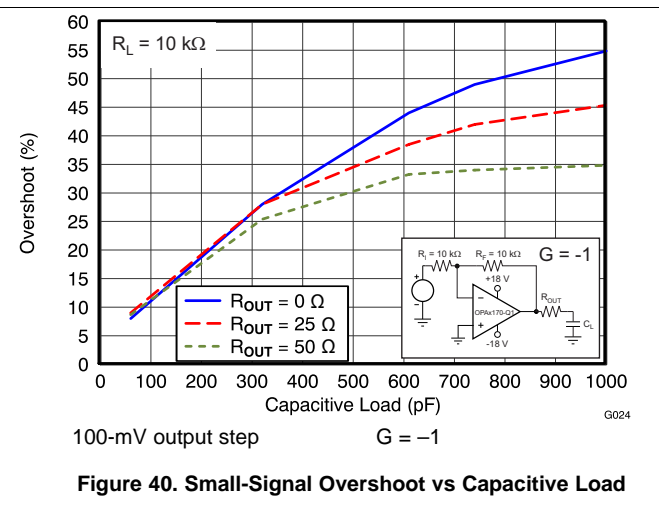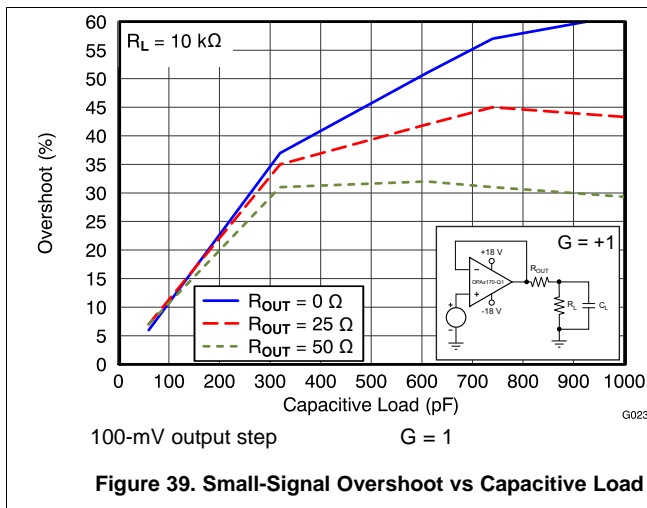
## Feature Description (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see Figure 38. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPAx170-Q1 input pins are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 38. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx170-Q1. Figure 38 illustrates an example configuration that implements a current-limiting feedback resistor.

### 7.3.4  Capacitive Load and Stability

The dynamic characteristics of the OPAx170-Q1 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ equal to 50 $\Omega$) in series with the output. Figure 39 and Figure 40 illustrate graphs of small-signal overshoot versus capacitive load for several values of $R_{OUT}$. See *Feedback Plots Define Op Amp AC Performance* (SBOA015) for details of analysis techniques and application circuits.



| | |
|---|---|
| 100-mV output step          G = 1 | 100-mV output step          G = −1 |
| **Figure 39. Small-Signal Overshoot vs Capacitive Load** | **Figure 40. Small-Signal Overshoot vs Capacitive Load** |

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

## 7.4 Device Functional Modes

### 7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx170-Q1 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 2.

**Table 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input common-mode voltage | | (V+) − 2 | | (V+) + 0.1 | V |
| Offset voltage | | | 7 | | mV |
| | vs temperature | | 12 | | µV/°C |
| Common-mode rejection | | | 65 | | dB |
| Open-loop gain | | | 60 | | dB |
| Gain-bandwidth product | | | 0.3 | | MHz |
| Slew rate | | | 0.3 | | V/µs |

### 7.4.2 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from the saturated state to the linear state. The output devices of the operational amplifier enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx170-Q1 is approximately 2 µs.

Product Folder Links: *OPA170-Q1  OPA2170-Q1  OPA4170-Q1*

# 8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The OPAx170-Q1 family of operational amplifiers provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, capacitors with a value of 0.1 µF are adequate. Follow the additional recommendations in the *Layout Guidelines* section to achieve the maximum performance from this device. Many applications may introduce capacitive loading to the output of the amplifier that may cause instability. Adding an isolation resistor between the amplifier output and the capacitive load stabilizes the amplifier. The design process for selecting this resistor is shown in the *Typical Application* section.

## 8.2 Typical Application

This circuit can drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor ($R_{ISO}$) to stabilize the output of an operational amplifier. $R_{ISO}$ modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.
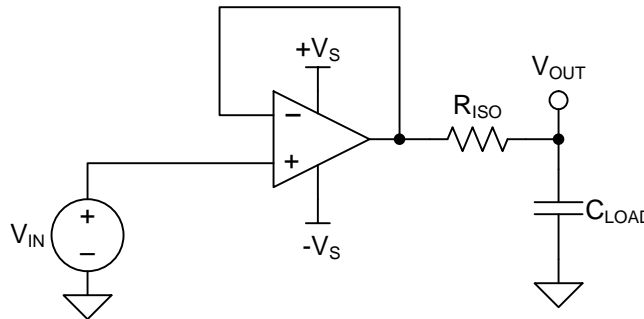


**Figure 41. Unity-Gain Buffer With $R_{ISO}$ Stability Compensation**

### 8.2.1 Design Requirements

The design requirements are:
- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100-pF, 1000-pF, 0.01-µF, 0.1-µF, and 1-µF
- Phase margin: 45° and 60°

### 8.2.2 Detailed Design Procedure

Figure 41 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 41. Not shown in Figure 41 is the open-loop output resistance of the operational amplifier, $R_O$.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s}$$

(1)

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole ($f_p$) is determined by ($R_O + R_{ISO}$) and $C_{LOAD}$. $R_{ISO}$ and $C_{LOAD}$ determine the frequency of the zero ($f_z$). A stable system is obtained by selecting $R_{ISO}$, so the rate of closure (ROC) between the open-loop gain ($A_{OL}$) and 1/β is 20 dB / decade. Figure 42 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

## Typical Application (continued)



The figure shows a Bode plot of Gain (dB) versus Frequency (Hz) with curves labeled $A_{OL}$ and $1/\beta$. Annotations indicate:

$$f_p = \frac{1}{2 \times \pi \times (R_{ISO} + R_o) \times C_{LOAD}}$$

$$f_z = \frac{1}{2 \times \pi \times R_{ISO} \times C_{LOAD}}$$

40 dB, 1 dec,
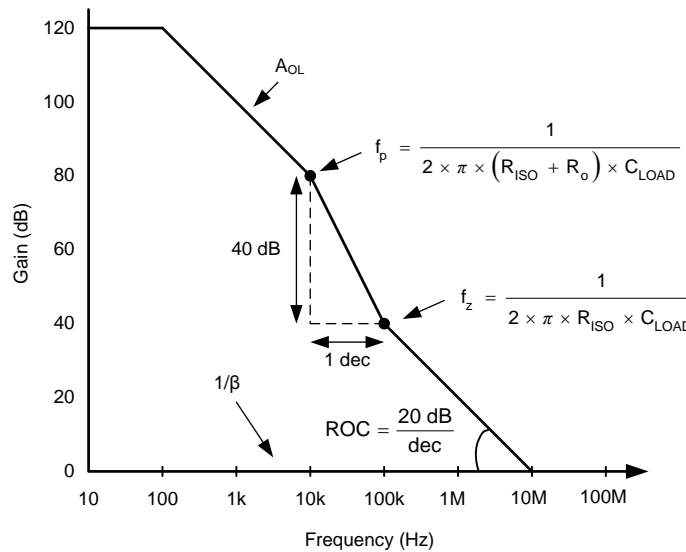
$$ROC = \frac{20 \text{ dB}}{\text{dec}}$$

**Figure 42. Unity-Gain Amplifier With $R_{ISO}$ Compensation**

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of $R_O$. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and ac gain peaking that correspond to 45° and 60° phase margins. For more details on this design and other alternative devices that can be used in place of the OPAx170-Q1, see *Capacitive Load Drive Solution Using an Isolation Resistor* (TIPD128).

**Table 3. Phase Margin versus Overshoot and AC Gain Peaking**

| PHASE MARGIN | OVERSHOOT | AC GAIN PEAKING |
|---|---|---|
| 45° | 23.3% | 2.35 dB |
| 60° | 8.8% | 0.28 dB |

### 8.2.3 Application Curve

Using the described methodology, the values of $R_{ISO}$ that yield phase margins of 45º and 60º for various capacitive loads were determined. Figure 43 shows the results.
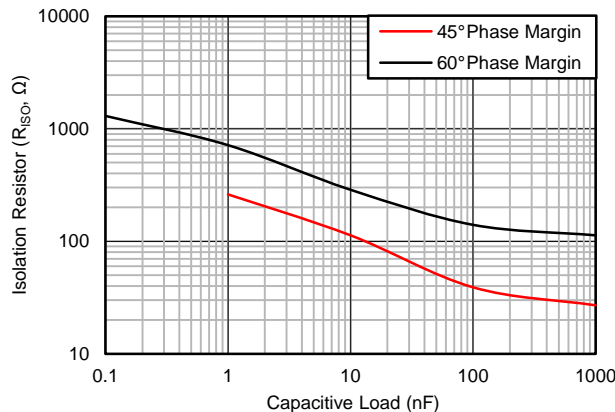


**Figure 43. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin**

# 9 Power Supply Recommendations

The OPAx170-Q1 family is specified for operation from 2.7 V to 36 V (±1.35 V to ±18 V); many specifications apply from –40°C to +85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Table 1*.

---

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

---

Place 0.1-$\mu$F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.
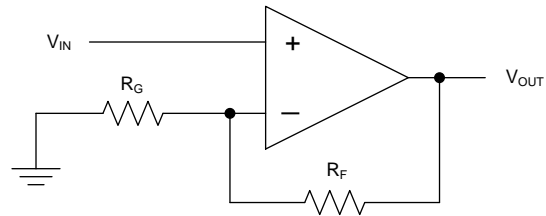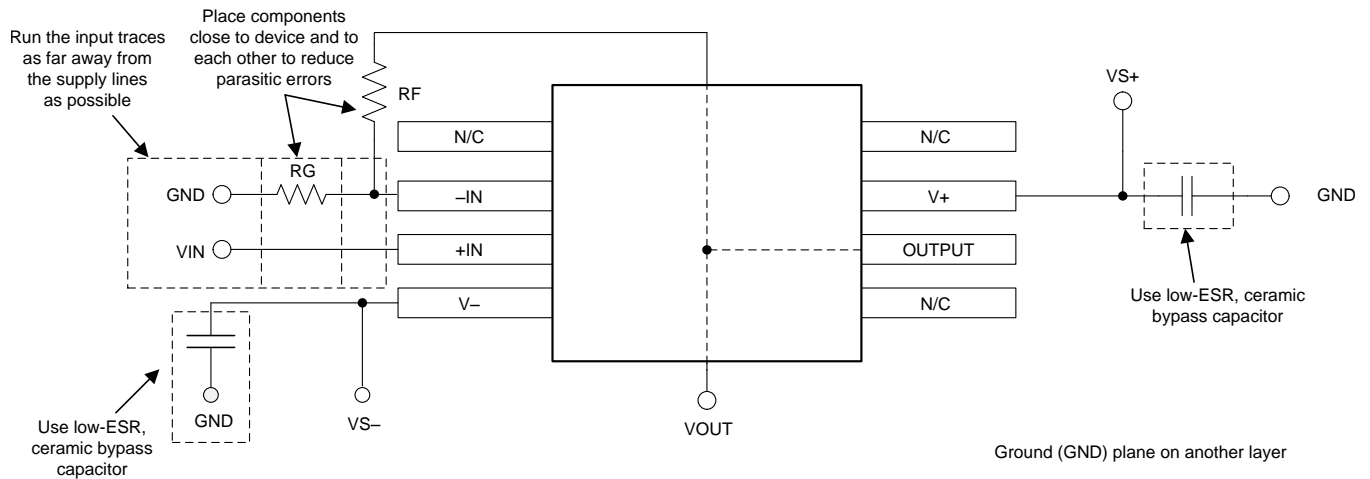
# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
    - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 45, keeping $R_F$ and $R_G$ close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 10.2 Layout Example



**Figure 44. Schematic Representation of a Noninverting Configuration**



**Figure 45. Operational Amplifier Board Layout for a Noninverting Configuration**

# 11   Device and Documentation Support

## 11.1   Device Support

### 11.1.1   Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 11.1.2   Development Support

#### 11.1.2.1   TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

#### 11.1.2.2   DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount devices. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

#### 11.1.2.3   Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT-23 packages are all supported.

**NOTE**

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

#### 11.1.2.4   TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

## Device Support (continued)

### 11.1.2.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer allows the user create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation, see the following (available for download from www.ti.com):
* *Feedback Plots Define Op Amp AC Performance* (SBOA015).
* *Capacitive Load Drive Solution Using an Isolation Resistor* (TIPD128).

## 11.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| OPA170-Q1 | Click here | Click here | Click here | Click here | Click here |
| OPA2170-Q1 | Click here | Click here | Click here | Click here | Click here |
| OPA4170-Q1 | Click here | Click here | Click here | Click here | Click here |

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.
    This glossary lists and explains terms, acronyms, and definitions.

## 12  Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA170AQDBVRQ1 | PREVIEW | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | 170Q | |
| OPA2170AQDGKRQ1 | PREVIEW | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2170 | |
| OPA4170AQPWRQ1 | PREVIEW | TSSOP | PW | 14 | 2000 | TBD | Call TI | Call TI | -40 to 125 | | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA170-Q1, OPA2170-Q1, OPA4170-Q1 :**

● Catalog: OPA170, OPA2170, OPA4170

● Enhanced Product: OPA170-EP

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

PW (R−PDSO−G14)                                        PLASTIC SMALL OUTLINE

0,65        ←  →        0,30 / 0,19        ⊕ | 0,10 (M)

14                      8

⟨D⟩  4,50 / 4,30        6,60 / 6,20

1                       7

5,10 / 4,90

⟨C⟩

0,15 NOM

Gage Plane

0°−8°                    0,25

0,75 / 0,50

1,20 MAX        0,15 / 0,05

Seating Plane        ◯ | 0,10

4040064−3/G  02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         ⟨C⟩  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         ⟨D⟩  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

DBV (R−PDSO−G5)                    PLASTIC SMALL−OUTLINE PACKAGE



0,95

5X $\frac{0,50}{0,30}$   ⌖ |0,20 Ⓜ|

5

4

$\frac{1,75}{1,45}$   $\frac{3,00}{2,60}$

$\frac{0,22}{0,08}$

Gage Plane

Pin 1
Index Area
(Optional)

1

3

$\frac{3,05}{2,75}$

|0,25|

0°−8°

$\frac{0,60}{0,30}$

1,45 MAX

$\frac{0,15}{0,00}$

Seating Plane

⌒ |0,10|
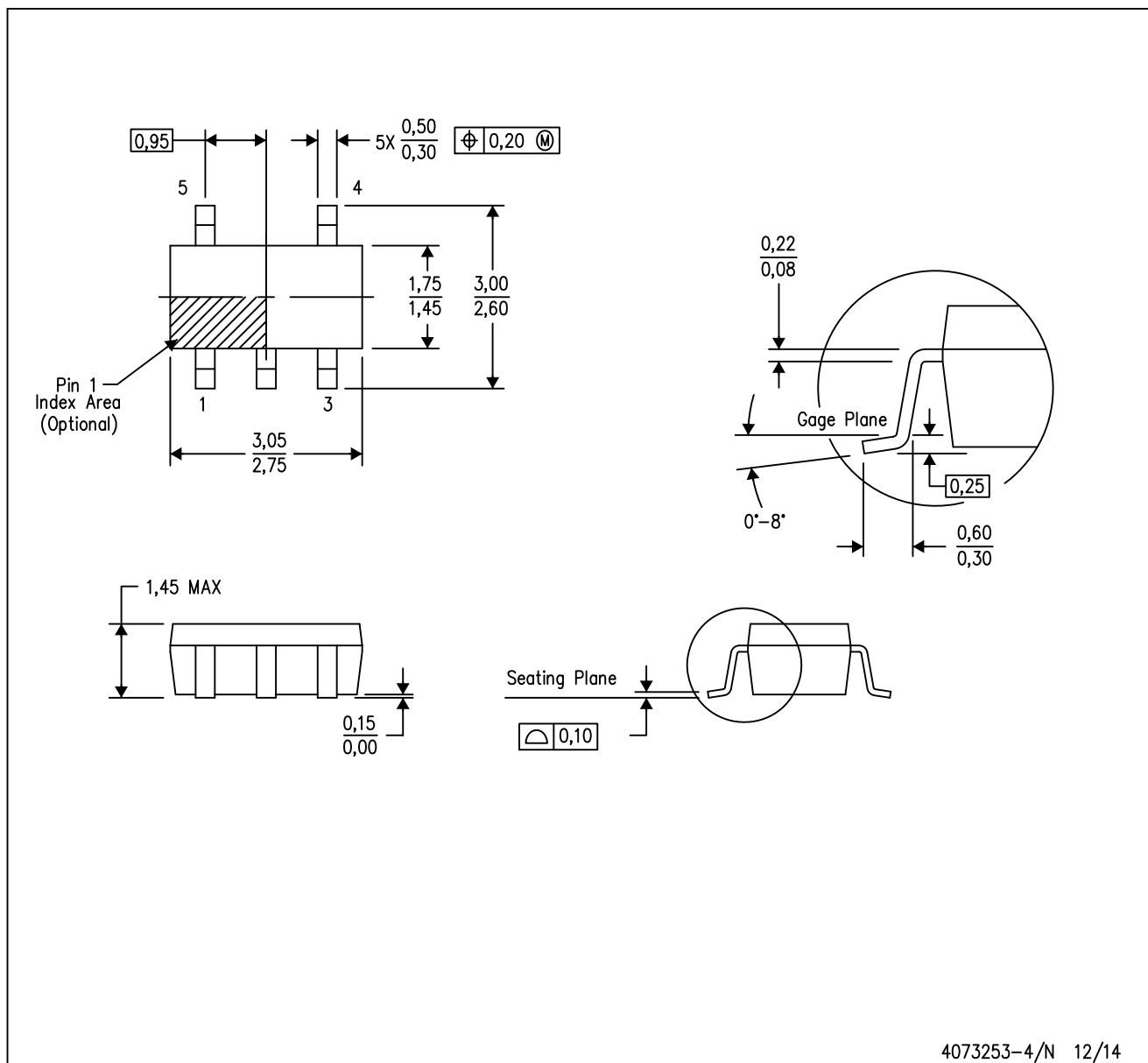
4073253−4/N  12/14

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−178 Variation AA.

DBV (R−PDSO−G5)                                    PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90

1,90

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−3/C 08/11

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations.  Example stencil design based on a 50% volumetric
              metal load solder paste.  Refer to IPC−7525 for other stencil recommendations.

DGK (S−PDSO−G8)                    PLASTIC SMALL−OUTLINE PACKAGE
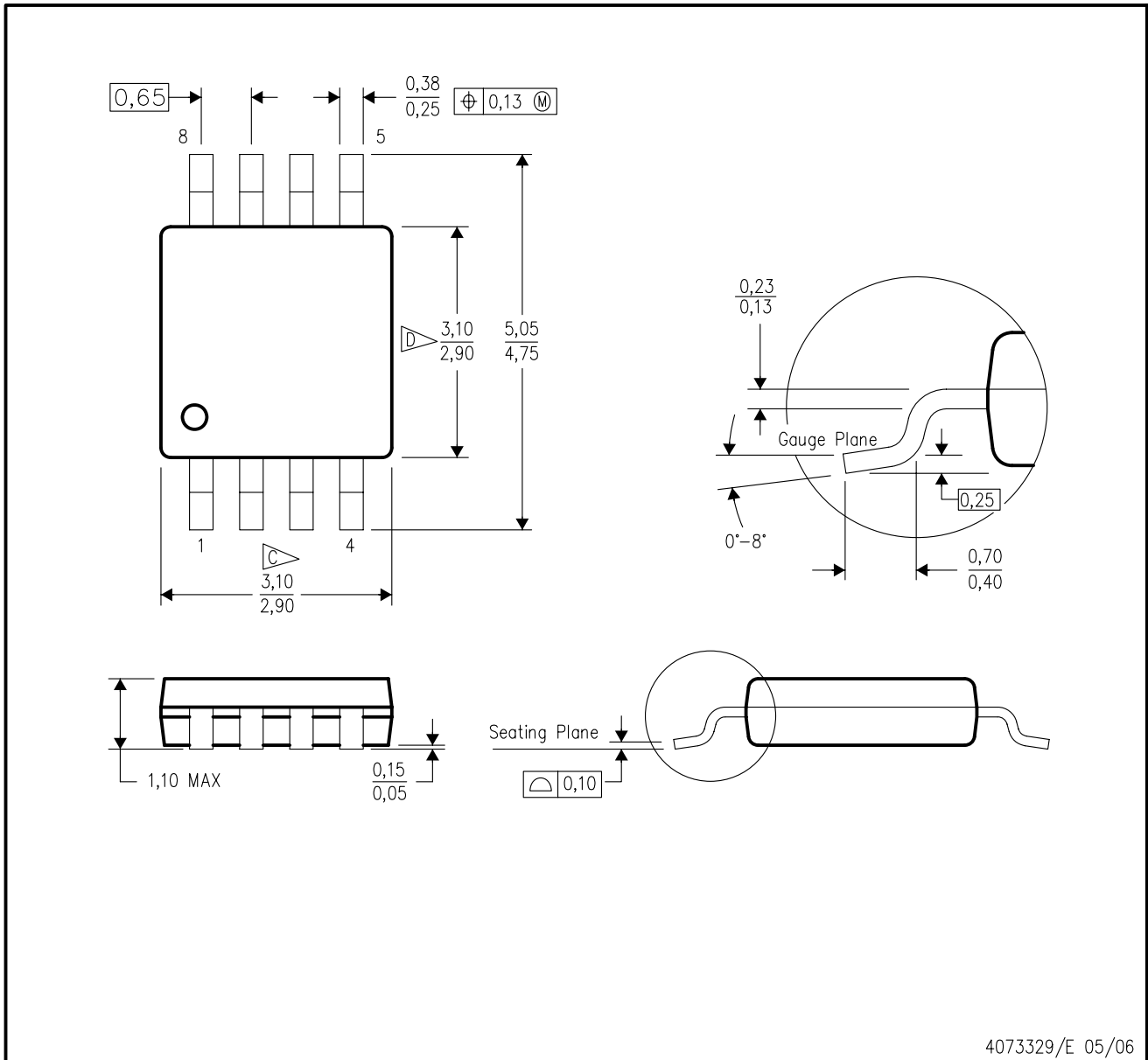


0,65

8         5

0,38
0,25    ⊕ 0,13 Ⓜ

D▷ 3,10
   2,90      5,05
             4,75

1         4

C▷
3,10
2,90

1,10 MAX        0,15
                0,05

0,23
0,13

Gauge Plane

0°−8°          0,25

0,70
0,40

Seating Plane

◠ 0,10

4073329/E 05/06

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
      C▷ Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed 0.15 per end.
      D▷ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
         E.  Falls within JEDEC MO−187 variation AA, except interlead flash.

TEXAS
INSTRUMENTS
www.ti.com

# IMPORTANT NOTICE

| Products | | Applications | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |