OP-07

OP-07 Low Offset, Low Drift Operational Amplifier

Literature Number: SNOS556A

National Semiconductor

December 1994

OP-07 Low Offset, Low Drift Operational Amplifier

General Description

The OP-07 has very low input offset voltage which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current and high open-loop gain. The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of ±13V minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

Features

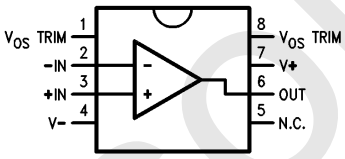
- Low V_{OS} — 75 μV Max
- Low V_{OS} Drift — 0.6 μV/°C Max
- Ultra-Stable vs Time — 1.0 μV/Month Max
- Low Noise — 0.6 μVp-p Max
- Wide Input Voltage Range — ±14V
- Wide Supply Voltage Range — ±3V to ±18V
- Fits 725/108A/308A, 741, AD510 Sockets
- Replaces the μA714

Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

Connection Diagram

Dual-In-Line Package



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See NS Package Number N08E

Ordering Information

T_A = 25°C V_{OS}Max (μV)	N08E Plastic	Operating Temperature Range
75	OP07EP	COM
150	OP07CP	COM
150	OP07DP	COM

*Also available per SMD #8203602

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

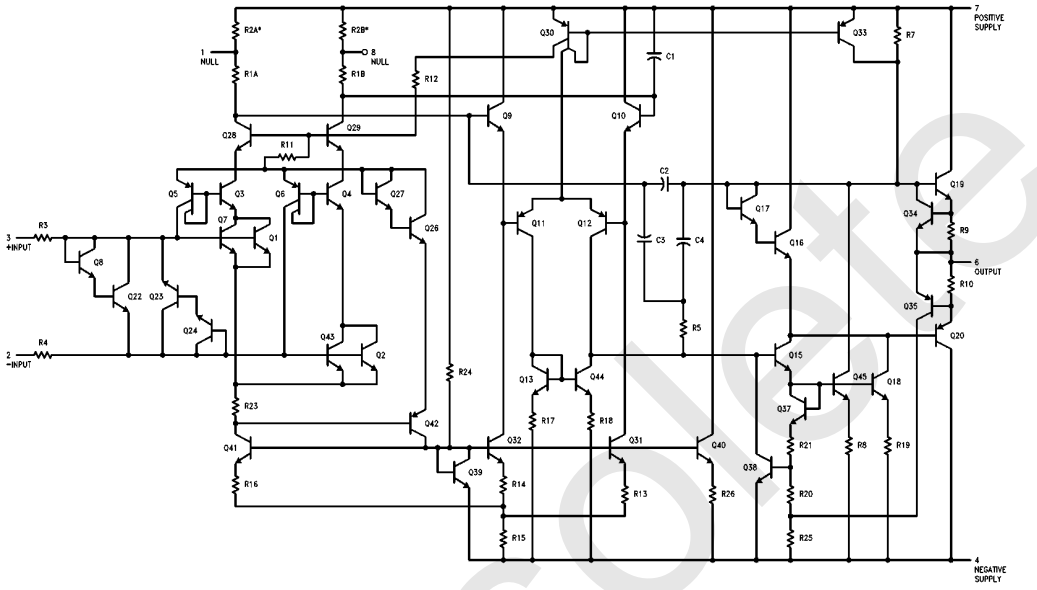
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 5)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 6)	±22V
Output Short-Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	260°C
Junction Temperature	−65°C to +150°C

Operating Temperature Range

OP-07E, OP-07C, OP-07D	0°C to +70°C

Simplified Schematic



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*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \leq T_A \leq 70°C$

Symbol	Parameter	Conditions	OP-07E			OP-07C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		30 **45**	75 **130**		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.3	1.5		0.4	2.0	$\mu V/Mo$
I_{OS}	Input Offset Current			0.5 **0.9**	3.8 **5.3**		0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			± 1.2 $\pm$ **1.5**	± 4.0 $\pm$ **5.5**		± 1.8 $\pm$ **2.2**	± 7.0 $\pm$ **9.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.38	0.65	μV_{p-p}
e_n	Input Noise Voltage Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		15	35	pA_{p-p}
i_n	Input Noise Current Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	15	50		8	33		MΩ
R_{INCM}	Input Resistance Common-Mode			160			120		GΩ
IVR	Input Voltage Range		± 13.0	± 14.0		± 13	± 14		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	106 **103**	123 **123**		100 **97**	120 **120**		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$ $V_S = \pm 3V$ to $\pm 18V$		5 **7**	20 **32**		7 **10**	32 **51**	$\mu V/V$
A_{VO}	Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_O = \pm 10V$ $R_L \geq 2$ kΩ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4)	200 **180** 150	500 **450** 400		120 **100** 100	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \geq 10$ kΩ $R_L \geq 2$ kΩ $R_L \geq 2$ kΩ $R_L \geq 1$ kΩ	± 12.5 ± 12.0 $\pm$ **12.0** ± 10.5	± 13.0 ± 12.8 $\pm$ **12.6** ± 12.0		± 12.0 ± 11.5 $\pm$ **11.0**	± 13.0 ± 12.8 $\pm$ **12.6** ± 12.0		V
SR	Slew Rate	$R_L \geq 2$ kΩ (Note 3)	0.1	0.3		0.1	0.3		$V/\mu s$
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		0.4	0.6		MHz
R_O	Output Resistance	$V_O = 0$, $I_O = 0$		60			60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		75 4	120 6		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20$ kΩ		± 4			± 4		mV
TCV_{OS} TCV_{OSn}	Average Input Offset Voltage Drift Without External Trim With External Trim	(Note 4) $R_P = 20$ kΩ (Note 4)		**0.3** **0.3**	**1.3** **1.3**		**0.5** **0.4**	**1.8** **1.6**	$\mu V/°C$
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**35**		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**13**	**35**		**18**	**50**	pA/°C

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Conditions	OP-07D			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.5	3.0	$\mu V/Mo$
I_{OS}	Input Offset Current			0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			± 2.0 $\pm$**3.0**	± 12.0 $\pm$**14.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		10.5 10.3 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	pAp-p
i_n	Input Noise Current Density	$f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	7	31		$M\Omega$
R_{INCM}	Input Resistance Common-Mode			120		$G\Omega$
IVR	Input Voltage Range		± 13	± 14		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	94 **94**	110 **106**		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		7 **10**	32 **51**	$\mu V/V$
A_{VO}	Large Signal Voltage Gain	$R_L \leq 2 k\Omega$, $V_O = \pm 10V$ $R_L = 2 k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S \pm 3V$ (Note 4)	120 **100**	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \geq 10 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 1 k\Omega$	± 12.0 ± 11.5 $\pm$**11.0**	± 13.0 ± 12.8 $\pm$**12.6** ± 12.0		V
SR	Slew Rate	$R_L \geq 2 k\Omega$ (Note 3)	0.1	0.3		$V/\mu s$
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
RO	Output Resistance	$V_O = 0$, $I_O = 0$		60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20 k\Omega$		± 4		mV
TCV_{OS} $TCV_{OS}n$	Average Input Offset Voltage Drift Without External Trim With External Trim	(Note 4) $R_P = 20 k\Omega$ (Note 4)		**0.7** **0.7**	**2.5** **2.5**	$\mu V/°C$ $\mu V/°C$
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**18**	**50**	pA/°C

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

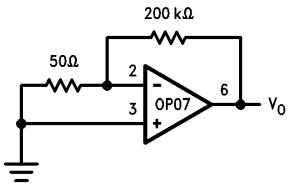
Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

Note 3: Sample Tested.

Note 4: Guaranteed by design.

Test Circuits

Offset Voltage Test Circuit



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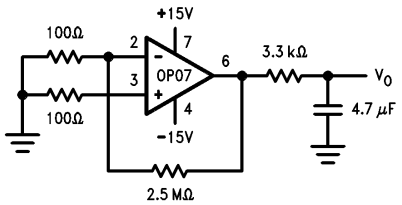
Low Frequency Noise Test Circuit



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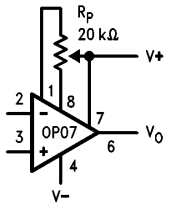
Optional Offset Nulling Circuit



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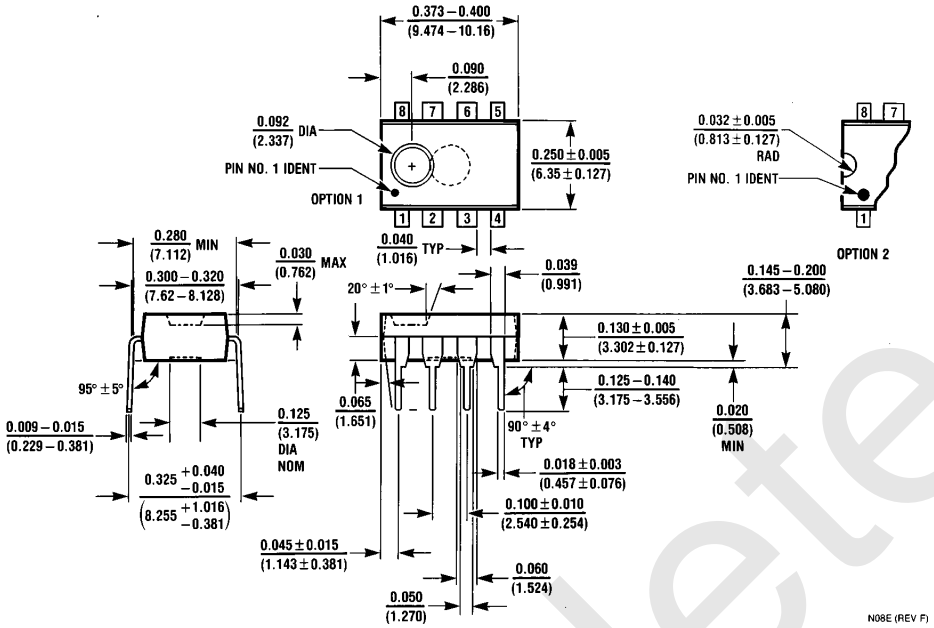
Physical Dimensions inches (millimeters) (Continued)



Order Number OP-07EP, OP-07CP or OP-07DP
NS Package Number N08E

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