# MOSFET – Power, N-Channel
## 100 V, 17 A, 81 mΩ

# NTD6416AN, NVD6416AN

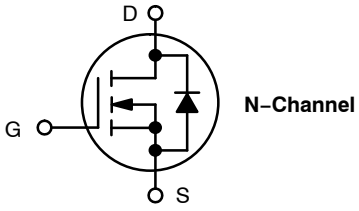
**ON Semiconductor®**

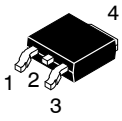
**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX (Note 1) |
|---|---|---|
| 100 V | 81 mΩ @ 10 V | 17 A |

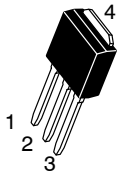
### Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant




**DPAK**
**CASE 369AA**
**STYLE 2**




**IPAK**
**CASE 369D**
**STYLE 2**

### MAXIMUM RATINGS ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 100 | V |
| Gate−to−Source Voltage − Continuous | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | Steady State | $T_C$ = 25°C | $I_D$ | 17 | A |
| | | $T_C$ = 100°C | | 11 | |
| Power Dissipation | Steady State | $T_C$ = 25°C | $P_D$ | 71 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | 62 | A |
| Operating and Storage Temperature Range | | | $T_J$, $T_{stg}$ | −55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 17 | A |
| Single Pulse Drain−to−Source Avalanche Energy ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, $I_{L(pk)}$ = 17 A, L = 0.3 mH, $R_G$ = 25 Ω) | | | $E_{AS}$ | 43 | mJ |
| Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds | | | $T_L$ | 260 | °C |

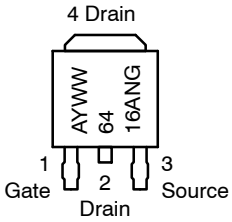
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

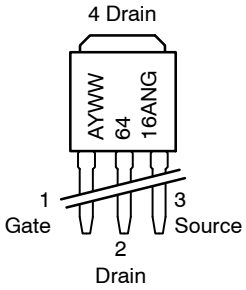
### THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) Steady State | $R_{\theta JC}$ | 2.1 | °C/W |
| Junction−to−Ambient (Note 1) | $R_{\theta JA}$ | 40 | |

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

### MARKING DIAGRAM & PIN ASSIGNMENTS




| | |
|---|---|
| A | = Assembly Location* |
| Y | = Year |
| WW | = Work Week |
| 6416AN | = Device Code |
| G | = Pb−Free Package |

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 100 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 112 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 2.0 | | 4.0 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 7.7 | | mV/°C |
| Drain−to−Source On−Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 17 A | | | 73 | 81 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 5 V, $I_D$ = 10 A | | | 12 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 25 V | | | 620 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 110 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 50 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 80 V, $I_D$ = 17 A | | | 20 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.0 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 3.6 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 10 | | |
| Plateau Voltage | $V_{GP}$ | | | | 5.8 | | V |
| Gate Resistance | $R_G$ | | | | 2.4 | | Ω |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 80 V, $I_D$ = 17 A, $R_G$ = 6.1 Ω | | | 9.2 | | ns |
| Rise Time | $t_r$ | | | | 22 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 24 | | |
| Fall Time | $t_f$ | | | | 20 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 17 A | $T_J$ = 25°C | | 0.85 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.7 | | |
| Reverse Recovery Time | $t_{rr}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs, $I_S$ = 17 A | | | 56 | | ns |
| Charge Time | $t_a$ | | | | 41 | | |
| Discharge Time | $t_b$ | | | | 15 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 135 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

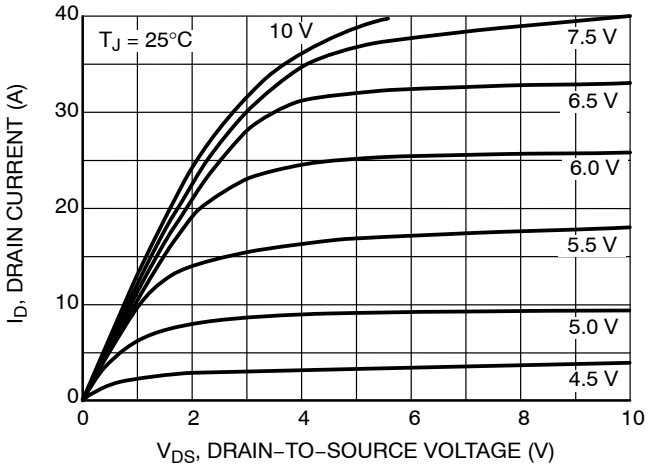



**Figure 1. On−Region Characteristics**

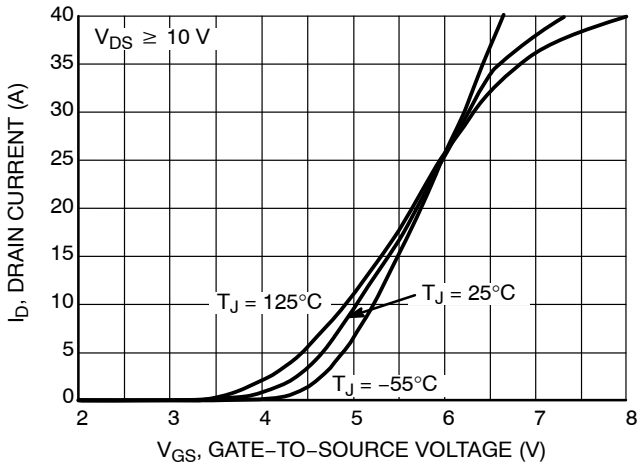



**Figure 2. Transfer Characteristics**

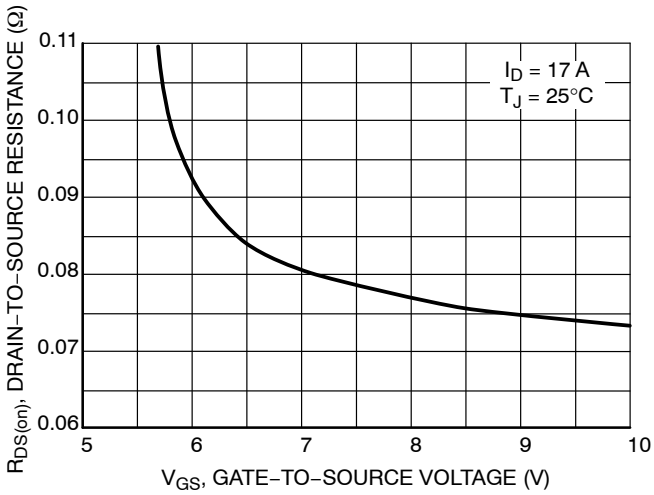



**Figure 3. On−Region versus Gate Voltage**

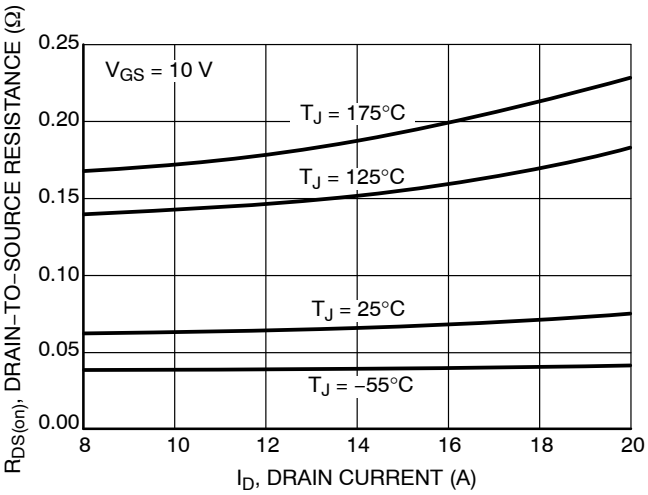



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

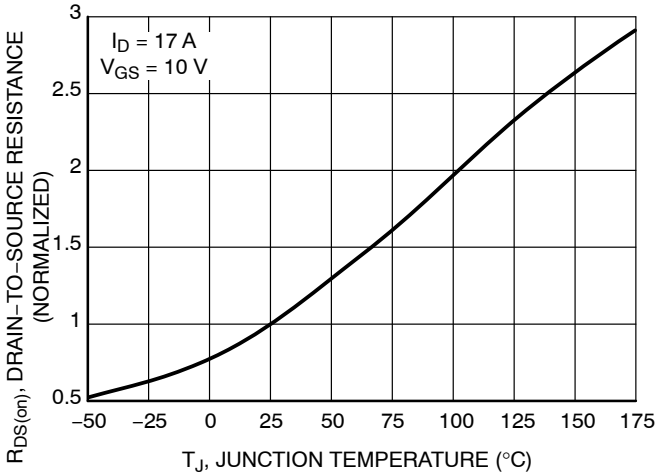



**Figure 5. On−Resistance Variation with Temperature**

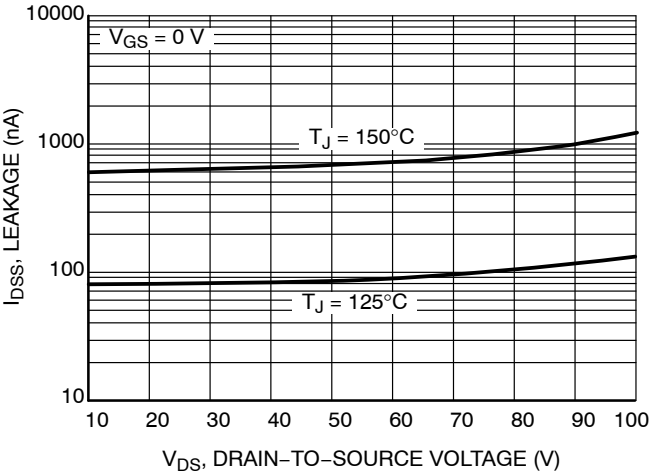



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

## TYPICAL CHARACTERISTICS

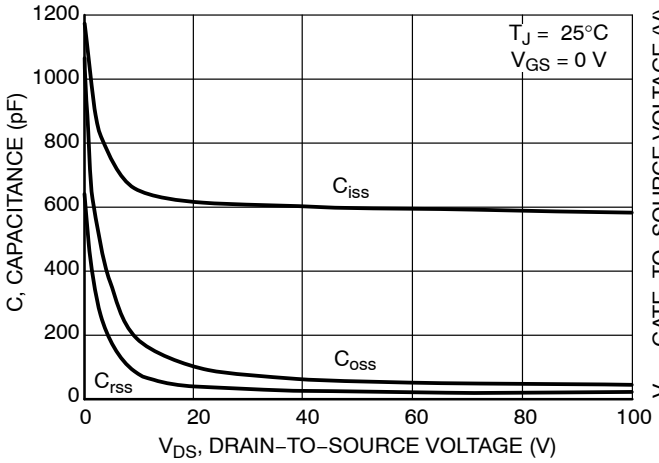



**Figure 7. Capacitance Variation**

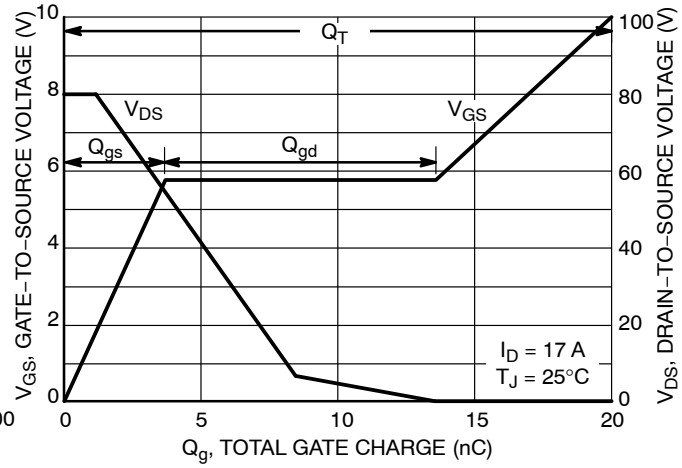



**Figure 8. Gate−to−Source Voltage and Drain−to−Source Voltage versus Total Charge**

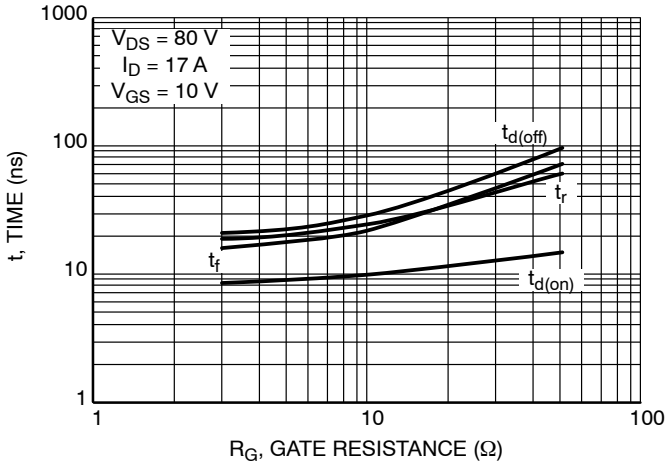



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

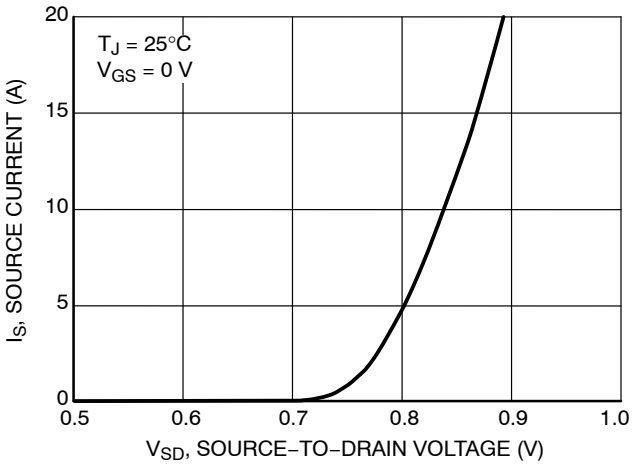



**Figure 10. Diode Forward Voltage versus Current**

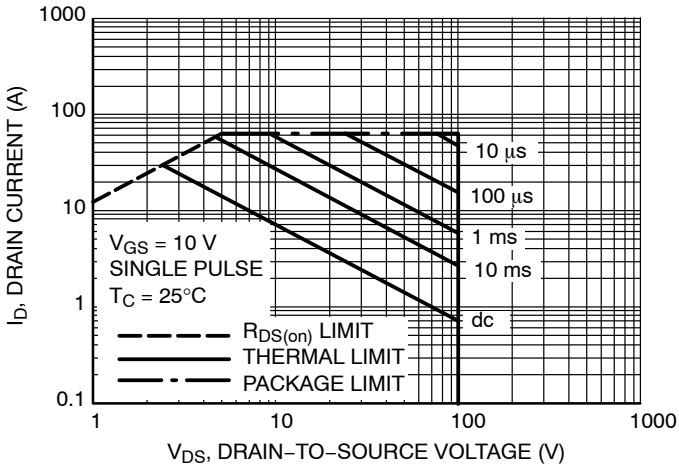



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

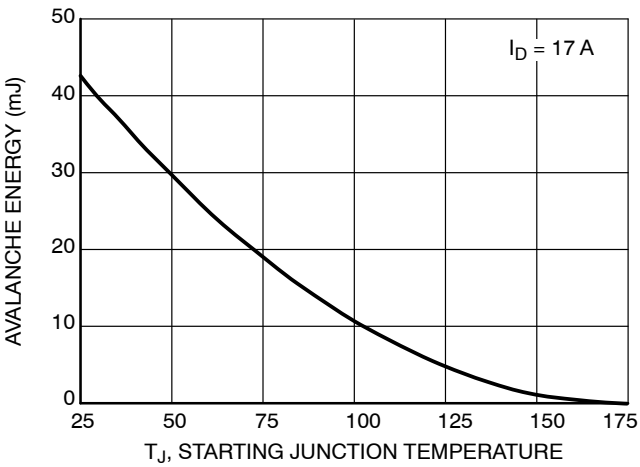



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL CHARACTERISTICS

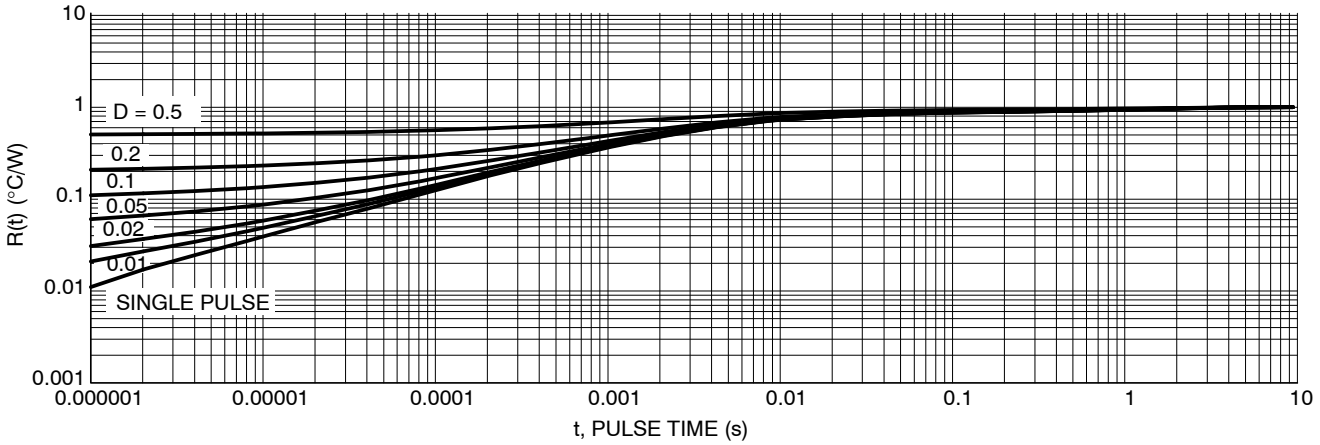



**Figure 13. Thermal Response**

### ORDERING INFORMATION

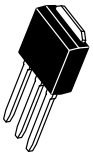
| Device | Package | Shipping† |
|---|---|---|
| NTD6416ANT4G | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NTD6416AN−1G | IPAK (Pb−Free) | 75 Units / Rail |
| NVD6416ANT4G* | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NVD6416ANT4G−VF01* | DPAK (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

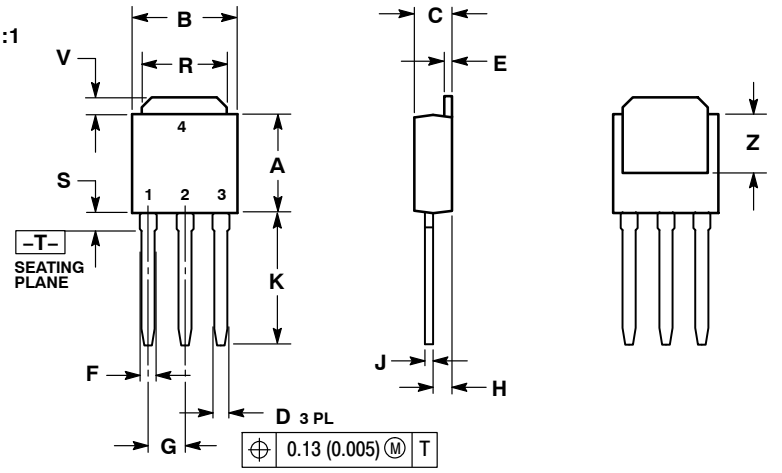
*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

**IPAK**
CASE 369D–01
ISSUE C

DATE 15 DEC 2010



SCALE 1:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

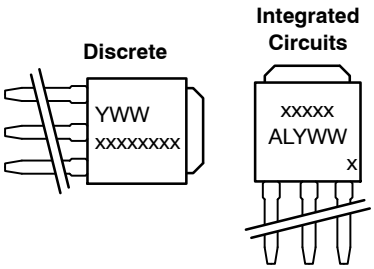
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## MARKING DIAGRAMS

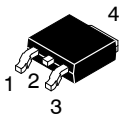



xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

| DOCUMENT NUMBER: | 98AON10528D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | IPAK (DPAK INSERTION MOUNT) | PAGE 1 OF 1 |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

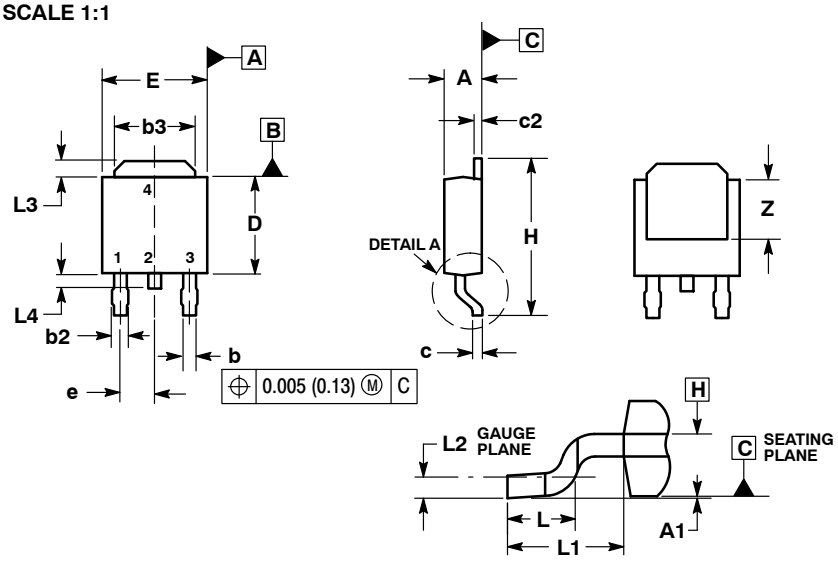
ON Semiconductor®




SCALE 1:1

**DPAK (SINGLE GUAGE)**
CASE 369AA−01
ISSUE B

DATE 03 JUN 2010




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | −−− | 0.040 | −−− | 1.01 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
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STYLE 3:
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3. ANODE
4. CATHODE

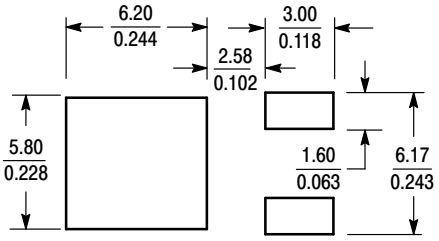
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

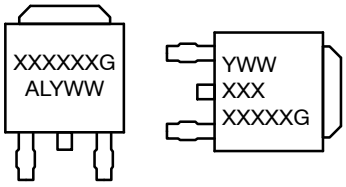
### SOLDERING FOOTPRINT*




SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

| | | |
|---|---|---|
| DOCUMENT NUMBER: | 98AON13126D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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