

NLAS7222B, NLAS7222C

High-Speed USB 2.0 (480 Mbps) DPDT Switches

ON Semiconductor's NLAS7222B and NLAS7222C are part of a series of analog switch circuits that are produced using the company's advanced sub-micron CMOS technology, achieving industry-leading performance.

Both the NLAS7222B and NLAS7222C are 2- to 1-port analog switches. Their wide bandwidth and low bit-to-bit skew allow them to pass high-speed differential signals with good signal integrity. Each switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Industry-leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Their high channel-to-channel crosstalk rejection results in minimal noise interference. Their bandwidth is wide enough to pass High-Speed USB 2.0 differential signals (480 Mb/s).

Features

- R_{ON} is Typically 8.0Ω at $V_{CC} = 3.3 V$
- Low Bit-to-Bit Skew: Typically 50 ps
- Low Crosstalk: -30 dB @ 250 MHz
- Low Current Consumption: $1.0 \mu A$
- Near-Zero Propagation Delay: 250 ps
- Channel On-Capacitance: 8.0 pF (Typical)
- V_{CC} Operating Range: 1.65 V to 4.5 V
- > 700 MHz Bandwidth (or Data Frequency)
- These are Pb-Free Devices

Typical Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

Important Information

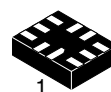
- Continuous Current Rating Through Each Switch $\pm 50 mA$
- 8 kV I/O to GND ESD Protection



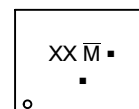
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



UQFN-10
CASE 488AT



XX = Device Code
xx = 2A or Y
M = Date Code
▪ = Pb-Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NLAS7222B, NLAS7222C

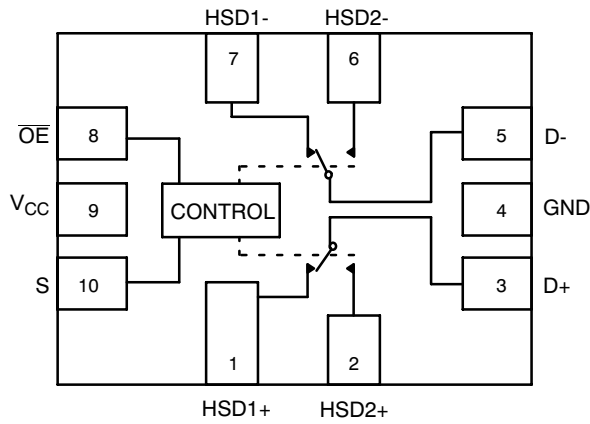


Figure 1. Pin Connections and Logic Diagram
(NLAS7222B, Top View)

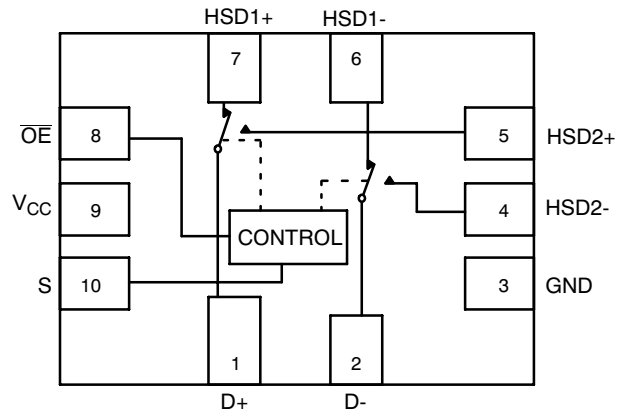


Figure 2. Pin Connections and Logic Diagram
(NLAS7222C, Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Select Input
\overline{OE}	Output Enable
HSD1+, HSD1-, HSD2+, HSD2-, D+, D-	Data Ports

Table 2. TRUTH TABLE

\overline{OE}	S	HSD1+, HSD1-	HSD2+, HSD2-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	-0.5 to +5.5	V
V_{IS}	HSD1+, HSD1- HSD2+, HSD2-	Analog Signal Voltage	-0.5 to $V_{CC} + 0.3$	V
	D+, D-		-0.5 to +5.5	
V_{IN}	\overline{OE}	Control Input Voltage	-0.5 to +5.5	V
I_{CC}	V_{CC}	Positive DC Supply Current	50	mA
T_S		Storage Temperature	-65 to +150	°C
I_{IS_CON}	HSD1+, HSD1- HSD2+, HSD2- D+, D-	Analog Signal Continuous Current-Closed Switch	± 300	mA
I_{IS_PK}	HSD1+, HSD1- HSD2+, HSD2- D+, D-	Analog Signal Continuous Current 10% Duty Cycle	± 500	mA
I_{IN}	\overline{OE}	Control Input Current	± 20	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}		Positive DC Supply Voltage	1.65	4.5	V
V_{IS}	HSD1+, HSD1- HSD2+, HSD2-	Analog Signal Voltage	GND	V_{CC}	V
	D+, D-		GND	4.5	
V_{IN}	\overline{OE}	Digital Select Input Voltage	GND	V_{CC}	V
T_A		Operating Temperature Range	-40	+85	°C

Minimum and maximum values are guaranteed through test or design across the Recommended Operating Conditions, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

NLAS7222B, NLAS7222C

ESD PROTECTION

Symbol	Parameter	Value	Unit
ESD	Human Body Model - All Pins	2.0	kV
ESD	Human Body Model - I/O to GND	8.0	kV

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
V _{IH}	OE	Control Input HIGH Voltage (See Figure 3)		2.7	1.3	-	-	V
				3.3	1.4			
				4.2	1.6			
V _{IL}	OE	Control Input LOW Voltage (See Figure 3)		2.7	-		0.4	V
				3.3			0.4	
				4.2			0.5	
I _{IN}	OE	Control Input Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	1.65 - 4.5	-	-	±1.0	μA

SUPPLY AND LEAKAGE CURRENT (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
I _{CC}	V _{CC}	Quiescent Supply Current	V _{IS} = V _{CC} or GND; I _{OUT} = 0 A	1.65 - 4.5	-	-	1.0	μA
I _{CC} T	V _{CC}	Increase in I _{CC} per Control Voltage	V _{IN} = 2.6 V	3.6	-	-	10	μA
I _{OZ}	HSD1+, HSD1-, HSD2+, HSD2-	OFF State Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	1.65 - 4.5	-	-	±1.0	μA
I _{OFF}	D+, D-	Power OFF Leakage Current	0 ≤ V _{IS} ≤ 4.5 V	0	-	-	±1.0	μA

HIGH SPEED ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R _{ON}		On-Resistance	V _{IS} = 0 V to 0.4 V, I _{ON} = 8 mA	2.7	-	9.0	12	Ω
				3.3		8.0	10	
				4.2		7.0	8.0	
R _{FLAT}		On-Resistance Flatness	V _{IS} = 0 V to 1.0 V, I _{ON} = 8 mA	2.7	-	1.6	-	Ω
				3.3		1.5		
				4.2		1.4		
ΔR _{ON}		On-Resistance Matching	V _{IS} = 0 V to 0.4 V, I _{ON} = 8 mA	2.7	-	1.05	-	Ω
				3.3		0.85		
				4.2		0.65		

NLAS7222B, NLAS7222C

DC ELECTRICAL CHARACTERISTICS (continued)

FULL SPEED ON RESISTANCE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R _{ON}		On-Resistance	V _{IS} = 0 V to V _{CC} , I _{ON} = 8 mA	2.7	9.0	12	Ω	
				3.3				
				4.2				
R _{FLAT}		On-Resistance Flatness	V _{IS} = 0 V to 1.0 V, I _{ON} = 8 mA	2.7	1.6		Ω	
				3.3				
				4.2				
ΔR _{ON}		On-Resistance Matching	V _{IS} = 0 V to V _{CC} , I _{ON} = 8 mA	2.7	2.20		Ω	
				3.3				
				4.2				

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
t _{ON}	Closed to Open	Turn-ON Time		1.65 - 4.5	-	14	30	ns
t _{OFF}	Open to Closed	Turn-OFF Time		1.65 - 4.5	-	10	20	ns
t _{BBM}		Break-Before-Make Delay		1.65 - 4.5	3.0	4.4	7.0	ns
BW		-3 dB Bandwidth	C _L = 5 pF	1.65 - 4.5	-	500	-	MHz
			C _L = 0 pF		-	750	-	

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
O _{IRR}	Open	OFF-Isolation	f = 250 MHz	1.65 - 4.5	-	-22	-	dB
X _{TALK}	HSD1+ to HSD1-	Non-Adjacent Channel Crosstalk	f = 250 MHz	1.65 - 4.5	-	-30	-	dB

NLAS7222B CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
C _{IN}	\overline{OE}	Control Pin Input Capacitance	V _{CC} = 0 V	-	3.0	-	pF
C _{ON}	D+ to HSD1+ or HSD2+	ON Capacitance	V _{CC} = 3.3 V; \overline{OE} = 0 V	-	8.0	-	pF
C _{OFF}	HSD2+, HSD2-	OFF Capacitance	V _{CC} = V _{IS} = 3.3 V; \overline{OE} = 3.3 V	-	4.5	-	pF

NLAS7222C CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
C _{IN}	\overline{OE}	Control Pin Input Capacitance	V _{CC} = 0 V	-	3.0	-	pF
C _{ON}	D+ to HSD1+ or HSD2+	ON Capacitance	V _{CC} = 3.3 V; \overline{OE} = 0 V	-	10	-	pF
C _{OFF}	HSD2+, HSD2-	OFF Capacitance	V _{CC} = V _{IS} = 3.3 V; \overline{OE} = 3.3 V	-	5.5	-	pF

NLAS7222B, NLAS7222C

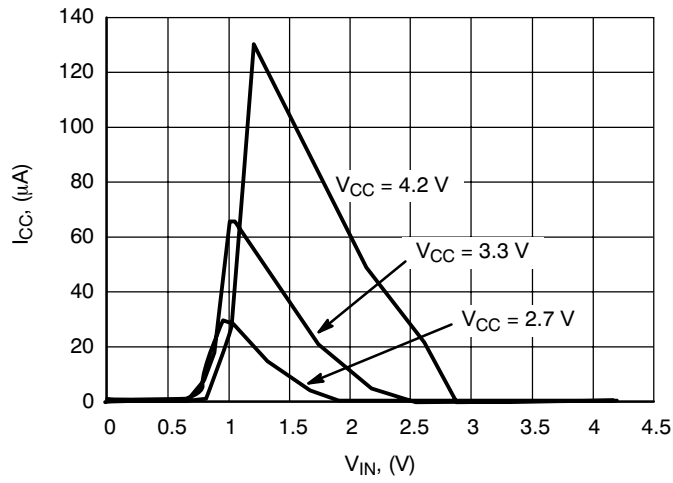


Figure 3. I_{CC} vs. V_{IN}

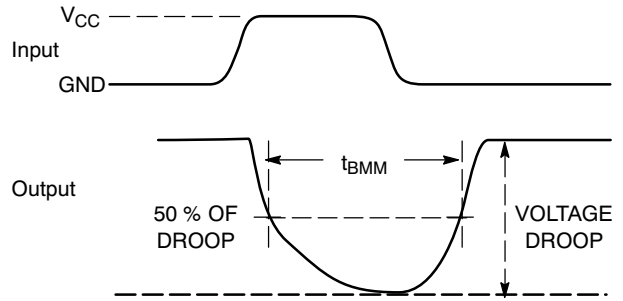
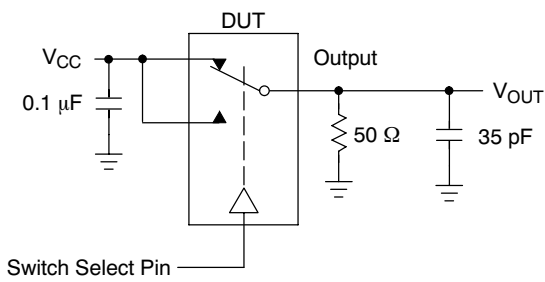


Figure 4. t_{BMM} (Time Break-Before-Make)

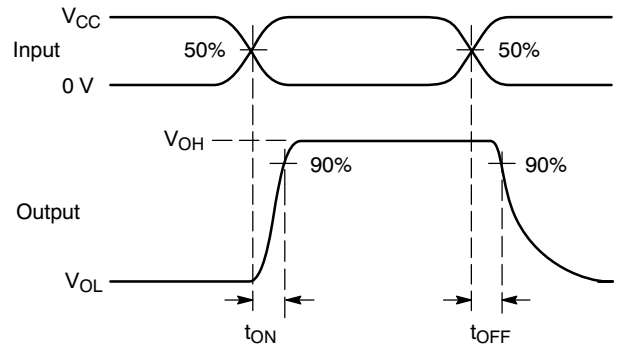
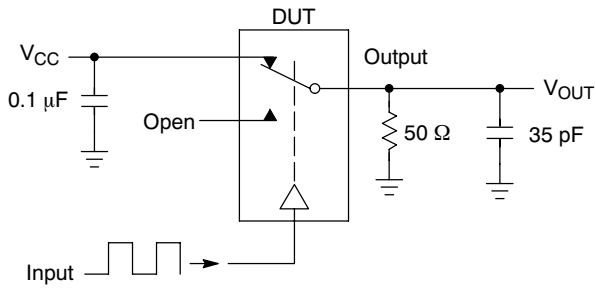


Figure 5. t_{ON}/t_{OFF}

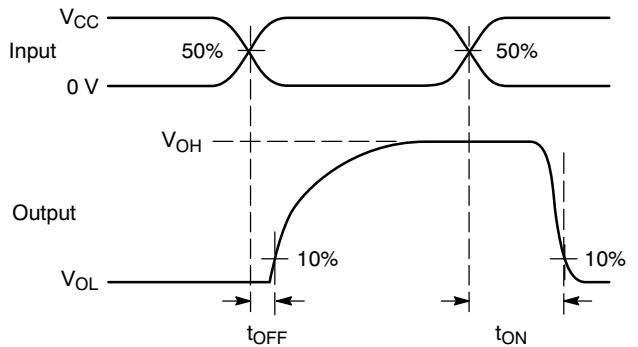
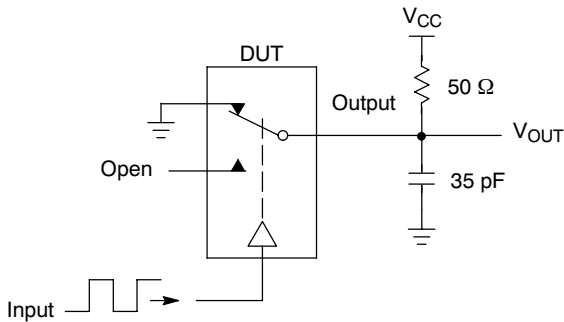
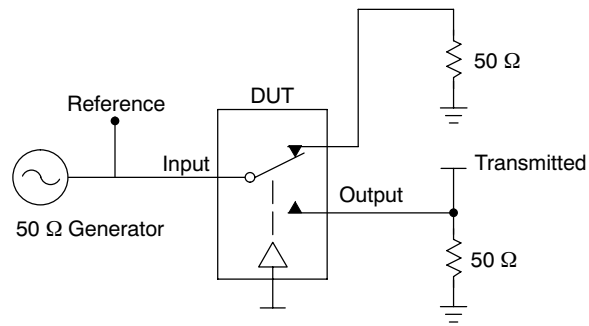


Figure 6. t_{ON}/t_{OFF}

NLAS7222B, NLAS7222C



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

NLAS7222B, NLAS7222C

APPLICATIONS INFORMATION

The low on resistance and capacitance of the NLAS7222B provides for a high bandwidth analog switch suitable for applications such as USB data switching. Results for the USB 2.0 signal quality tests will be shown in this section, along with a description of the evaluation test board. The data for the eye diagram signal quality and jitter tests verifies that the NLAS7222B can be used as a data switch in low, full and high speed USB 2.0 systems.

Figures 8, 9 and 10 provide a description of the test evaluation board. The USB tests were conducted per the procedures provided by the USB Implementers Forum

(www.usb.org), the industry group responsible for defining the USB certification requirements. The test patterns were generated by a PC and MATLAB software, and were inputted to the analog switch through USB connectors J1 (HSD1) or J2 (HSD2). A USB certified device was plugged into connector J4 to function as a data transceiver. The high speed and full speed tests used a flash memory device, while the low speed tests used a mouse. Test connectors J3 and J5 provide a direct connection of the USB device and were used to verify that the analog switch does not distort the data signals.

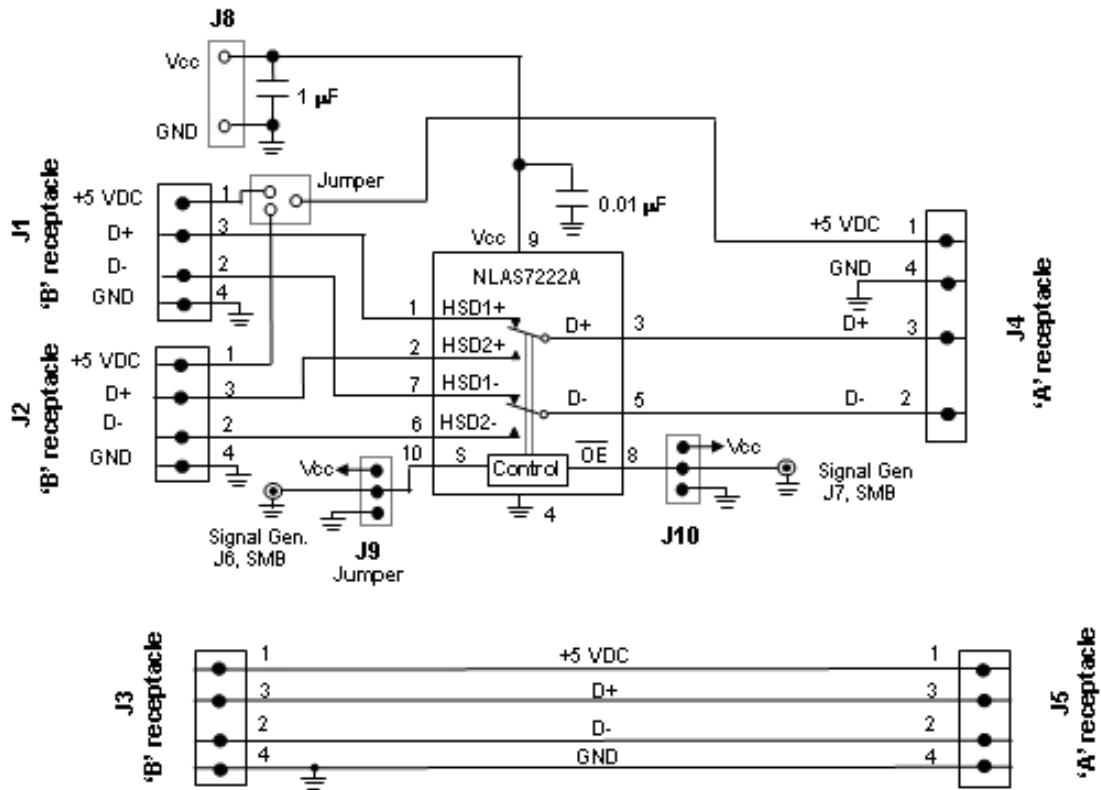


Figure 8. Schematic of the NLAS7222B USB Demo Board

NLAS7222B, NLAS7222C

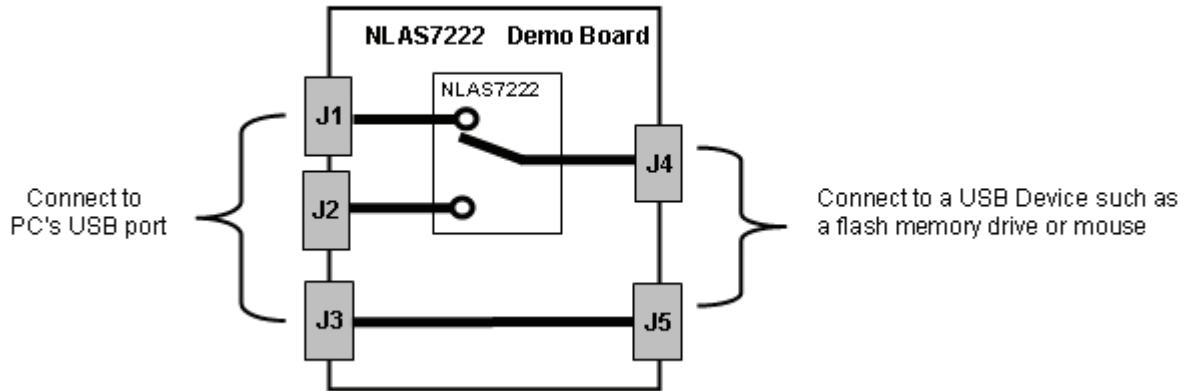


Figure 9. Block Diagram of the NLAS7222B USB Demo Board

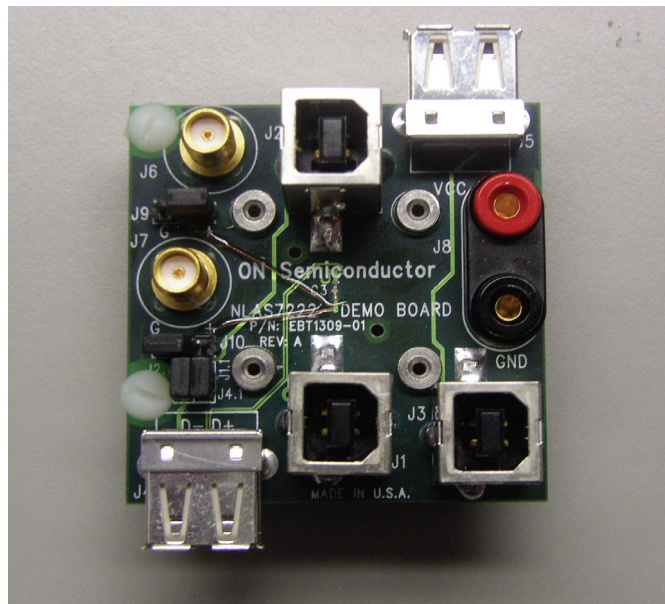


Figure 10. Photograph of the NLAS7222B USB Demo Board

ORDERING INFORMATION

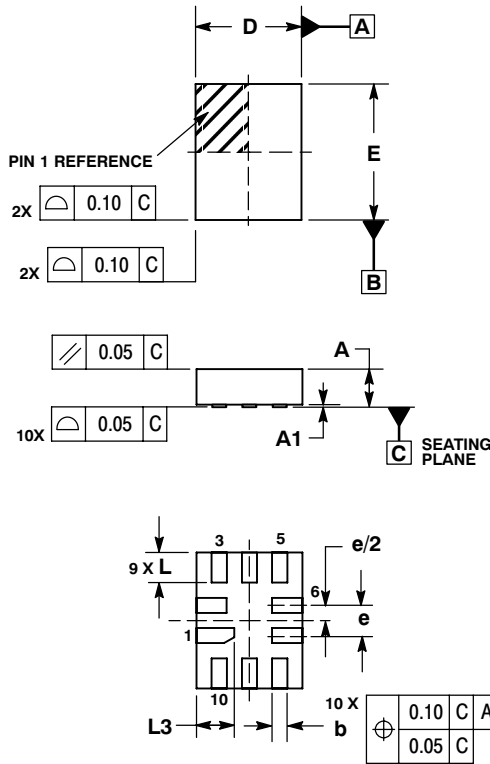
Device	Package	Shipping†
NLAS7222BMUTBG	UQFN-10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLAS7222B, NLAS7222C

PACKAGE DIMENSIONS

10 PIN UQFN, 1.4x1.8, 0.4P
CASE 488AT-01
ISSUE O

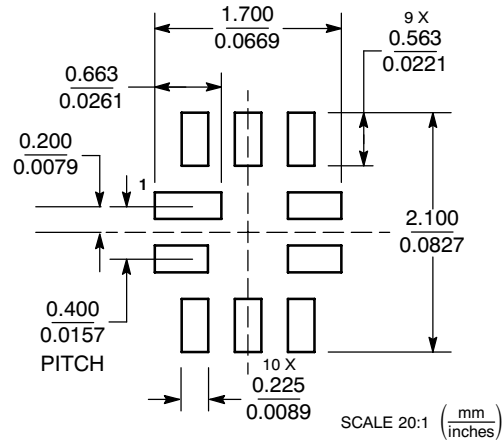


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L3	0.40	0.60

MOUNTING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative