# NCP81075

# High Performance Dual MOSFET Gate Driver

## Introduction

The NCP81075 is a high performance dual MOSFET gate driver optimized to drive the gates of both high and low side power MOSFETs in a synchronous buck converter. The NCP81075 uses an on−chip bootstrap diode to eliminate the external discrete diode. A high floating top driver design can accommodate HB voltage as high as 180 V. The low−side and high−side are independently controlled and match to 4 ns between the turn−on and turn−off of each other. Independent Under−Voltage lockout is provided for the high side and low side driver forcing the output low when the drive voltage is below a specific threshold.

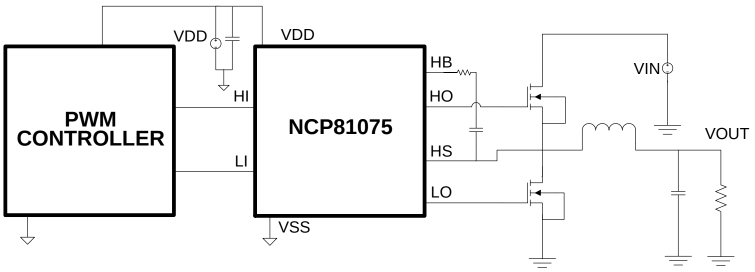
## Features

- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration
- Floating Top Driver Accommodates Boost Voltage up to 180 V
- Switching Frequency up to 1 MHz
- 20 ns Propagation Delay Times
- 4 A Sink, 4 A Source Output Currents
- 8 ns Rise / 7 ns Fall Times with 1000 pF Load
- UVLO Protection
- Specified from −40°C to 140°C
- Offered in SOIC−8 (D), DFN8 (MN), WDFN10 (MT) Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

## Applications

- Telecom and Datacom
- Isolated Non−Isolated Power Supply Architectures
- Class D Audio Amplifiers
- Two Switch and Active Clamp Forward Converters

## Simplified Application Diagram



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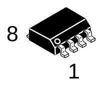
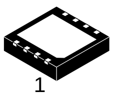
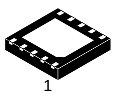


**SOIC−8 NB**
**CASE 751−07**

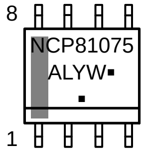


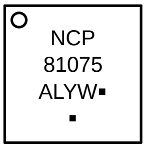
**DFN8**
**CASE 506CY**



**WDFN10**
**CASE 511CE**

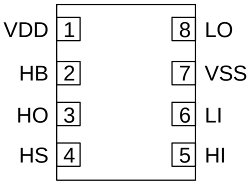
## MARKING DIAGRAMS



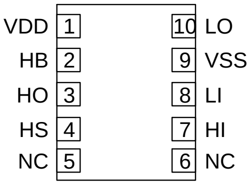


NCP81075 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

## PINOUT DIAGRAMS



SOIC/DFN8



WDFN10

NCP81075
(top views)

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCP81075DR2G | SOIC8<br>(Pb−Free) | 2500 /<br>Tape & Reel |
| NCP81075MNTXG | DFN8<br>(Pb−Free) | 4000 /<br>Tape & Reel |
| NCP81075MTTXG | WDFN10<br>(Pb−Free) | 4000 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

October, 2017 − Rev. 1

### Table 1. PIN DESCRIPTION

| Pin No. SOIC/DFN8 | Pin No. WDFN10 | Symbol | Description |
|---|---|---|---|
| 1 | 1 | VDD | Positive Supply to the Lower Gate Driver |
| 2 | 2 | HB | High Side Bootstrap Supply |
| 3 | 3 | HO | High Side Output |
| 4 | 4 | HS | High−Side Source |
| 5 | 7 | HI | High−Side Input |
| 6 | 8 | LI | Low−Side Input |
| 7 | 9 | VSS | Negative Supply Return |
| 8 | 10 | LO | Low−Side Output |
| − | 5,6 | NC | No Connect |

### Table 2. MAXIMUM RATINGS

| Parameter | | Value | Units |
|---|---|---|---|
| VDD | | −0.3 to 24 | V |
| $V_{HB}$ | | −0.3 to 200 | V |
| $V_{HO}$ | DC | $V_{HS}$ – 0.3 to $V_{HB}$ + 0.3 | V |
| | Repetitive Pulse < 100 ns | $V_{HS}$ − 2 to $V_{HB}$ + 0.3, ($V_{HB}$ − $V_{HS}$ < 24) | |
| $V_{HS}$ | DC | −20 to 200 − VDD | V |
| $V_{LO}$ | DC | −0.3 to VDD + 0.3 | V |
| | Repetitive pulse < 100 ns | −2 to VDD + 0.3 | |
| $V_{HI}$, $V_{LI}$ | | −10 to 24 | V |
| $V_{HB-HS}$ | | −0.3 to 24 | V |
| Operating Junction Temperature Range, $T_J$ | | −40 to 170 | °C |
| Storage Temperature, $T_{STG}$ | | −65 to 150 | °C |
| Lead Temperature (Soldering, 10 sec) | | +300 | °C |
| HBM | | 1000 | V |
| CDM | | 2000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $V_{HB}$ – $V_{HS}$ should be in the range of −0.3 V to +20 V.

### Table 3. RECOMMENDED OPERATING CONDITIONS

| Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | 8.5 | 12 | 20 | V |
| $V_{HS}$ | Voltage on HS (DC) | −10 | | 180 − VDD | |
| $V_{HB}$ | Voltage on HB | $V_{HS}$ + 8,<br>$V_{DD}$ − 1 | | $V_{HS}$ + 20,<br>180 | |
| | Voltage Slew Rate on HS | | | 50 | V / ns |
| $T_J$ | Operating Junction Temperature Range | −40 | | +140 | °C |
| $V_{HO}$ | | $V_{HS}$ − 0.3 | | $V_{HB}$ + 0.3 | V |
| $V_{LO}$ | | −0.3 | | $V_{DD}$ + 0.3 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ABSOLUTE MAXIMUM RATINGS

**Table 4. ELECTRICAL/THERMAL INFORMATION** (All signals referenced to GND unless noted otherwise, Note 2)

| Thermal Characteristic | SOIC | DFN8 | DFN10 | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ Junction to Ambient thermal resistance | 41 | 36 | 35 | °C/W |
| $\theta_{JC(top)}$ Junction to case (Top) thermal resistance | 50 | 42 | 32 | |
| $\theta_{JB}$ Junction to Board thermal resistance | 10 | 19.1 | 12 | |
| $\theta_{JC(Bottom)}$ Junction to case (Bottom) thermal resistance | 1.5 | 4 | 1.3 | |
| $\psi_{JT}$ Junction to top characterization parameter | 3.1 | 0.6 | 0.2 | |
| $\psi_{JB}$ Junction to board characterization parameter | 10 | 19.3 | 12.2 | |
| Moisture Sensitivity Level (MSL)<br>QFN Package | 1 | | | |

2. This data was taken using the JEDEC proposed High−K Test PCB.

**Table 5. ELECTRICAL CHARACTERISTICS**
Unless otherwise stated: $T_A = T_J = -40°C$ to 140°C; VDD = VHB = 12 V, VHS = VSS = 0 V, No load on LO or HO

| Parameter | | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{DD}$ | VDD quiescent current | $V_{LI} = V_{HI} = 0$ | | 0.85 | 1.8 | mA |
| $I_{DDO}$ | VDD operating current | f = 500 kHz, $C_{LOAD} = 0$ | | 7.3 | 15 | |
| | | f = 300 kHz, $C_{LOAD} = 0$ | | 4.9 | 11 | |
| $I_{HB}$ | Boot voltage quiescent current | $V_{LI} = V_{HI} = 0$ V | | 0.92 | 1.8 | |
| $I_{HBO}$ | Boot voltage operating current | f = 500 kHz, $C_{LOAD} = 0$ | | 6.55 | 12 | |
| | | f = 300 kHz, $C_{LOAD} = 0$ | | 4.5 | 7.0 | |
| $I_{HBS}$ | HB to $V_{SS}$ quiescent current | $V_{HS} = V_{HB} = 110$ V | | 5.0 | 25 | μA |
| $I_{HBSO}$ | HB to $V_{SS}$ operating current | f = 500 kHz, $C_{LOAD} = 0$ | | 0.1 | | mA |
| **INPUT** | | | | | | |
| $V_{HIH}$, $V_{LIH}$ | Input rising threshold | | 2.7 | | | V |
| $V_{HIL}$, $V_{LIL}$ | Input falling threshold | | | | 0.8 | |
| $R_{IN}$ | Input Pulldown Resistance | | 100 | 170 | 350 | kΩ |
| **UNDERVOLTAGE PROTECTION (UVLO)** | | | | | | |
| | VDD rising threshold | | 6.2 | 7.1 | 8.0 | V |
| | VDD threshold hysteresis | | | 0.58 | | |
| | VHB rising threshold | | 5.5 | 6.5 | 7.5 | |
| | VHB threshold hysteresis | | | 0.5 | | |
| **BOOTSTRAP DIODE** | | | | | | |
| $V_F$ | Low−current forward voltage | $I_{VDD}$ − HB = 100 μA | | 0.59 | 0.95 | V |
| $V_{FI}$ | High−current forward voltage | $I_{VDD}$ − HB = 100 mA | | 0.85 | 1.1 | |
| $R_D$ | Dynamic resistance, ΔVF/ΔI | $I_{VDD}$ − HB = 100 mA and 80 mA | | 0.94 | 2.0 | Ω |
| **LO GATE DRIVER** | | | | | | |
| $V_{LOL}$ | Low level output voltage | $I_{LO} = 100$ mA | | 0.1 | 0.40 | V |
| $V_{LOH}$ | High level output voltage | $I_{LO} = -100$ mA, $V_{LOH} = V_{DD} - V_{LO}$ | | 0.15 | 0.40 | |
| | Peak pull−up current | $V_{LO} = 0$ V | | 4 | | A |
| | Peak pull−down current | $V_{LO} = 12$ V | | 4 | | |

### Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise stated: $T_A = T_J = −40°C$ to 140°C; VDD = VHB = 12 V, VHS = VSS = 0 V, No load on LO or HO

| Parameter | | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **HO GATE DRIVER** | | | | | | |
| $V_{HOL}$ | Low level output voltage | $I_{HO}$ = 100 mA | | 0.1 | 0.40 | V |
| $V_{HOH}$ | High level output voltage | $I_{HO}$ = −100 mA, $V_{HOH} = V_{HB} – V_{HO}$ | | 0.15 | 0.40 | |
| | Peak pull−up current | $V_{LO}$ = 0 V | | 4 | | A |
| | Peak pull−down current | $V_{LO}$ = 12 V | | 4 | | |
| **PROPAGATION DELAYS** | | | | | | |
| $t_{DLFF}$ | $V_{LI}$ falling to $V_{LO}$ falling | $C_{LOAD}$ = 0 (−40 to 125°C) | | 20 | 45 | ns |
| | | $C_{LOAD}$ = 0 (−40 to 140°C) | | 20 | 50 | |
| $t_{DHFF}$ | $V_{HI}$ falling to $V_{HO}$ falling | $C_{LOAD}$ = 0 (−40 to 125°C) | | 20 | 45 | |
| | | $C_{LOAD}$ = 0 (−40 to 140°C) | | 20 | 50 | |
| $t_{DLRR}$ | $V_{LI}$ rising to $V_{LO}$ rising | $C_{LOAD}$ = 0 (−40 to 125°C) | | 20 | 45 | |
| | | $C_{LOAD}$ = 0 (−40 to 140°C) | | 20 | 50 | |
| $t_{DHRR}$ | $V_{HI}$ rising to $V_{HO}$ rising | $C_{LOAD}$ = 0 (−40 to 125°C) | | 20 | 45 | |
| | | $C_{LOAD}$ = 0 (−40 to 140°C) | | 20 | 50 | |
| **DELAY MATCHING** | | | | | | |
| tMON | LI ON, HI OFF | | | 3.5 | 14 | ns |
| tMOFF | LI OFF, HI ON | | | 3.5 | 14 | |
| **OUTPUT RISE AND FALL TIME** | | | | | | |
| $t_R$ | LO, HO | $C_{LOAD}$ = 1000 pF | | 8 | | ns |
| $t_F$ | LO, HO | $C_{LOAD}$ = 1000 pF | | 7 | | |
| $t_R$ | LO, HO (3 V to 9 V) | $C_{LOAD}$ = 0.1 μF | | 0.2 | 0.55 | μs |
| $t_F$ | LO, HO (3 V to 9 V) | $C_{LOAD}$ = 0.1 μF | | 0.25 | 0.45 | |
| **MISCELLANEOUS** | | | | | | |
| $t_1$ | Minimum input pulse width that changes the output | | | 30 | | ns |
| $t_2$ | Bootstrap diode turn−off time | $I_F$ = 100 mA, $I_{REV}$ = −100 mA (Notes 3 and 4) | | 50 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Typical values for $T_A$ = 25°C
4. $I_F$: Forward current applied to bootstrap diode, $I_{REV}$: Reverse current applied to bootstrap diode.

## Internal Block Diagram

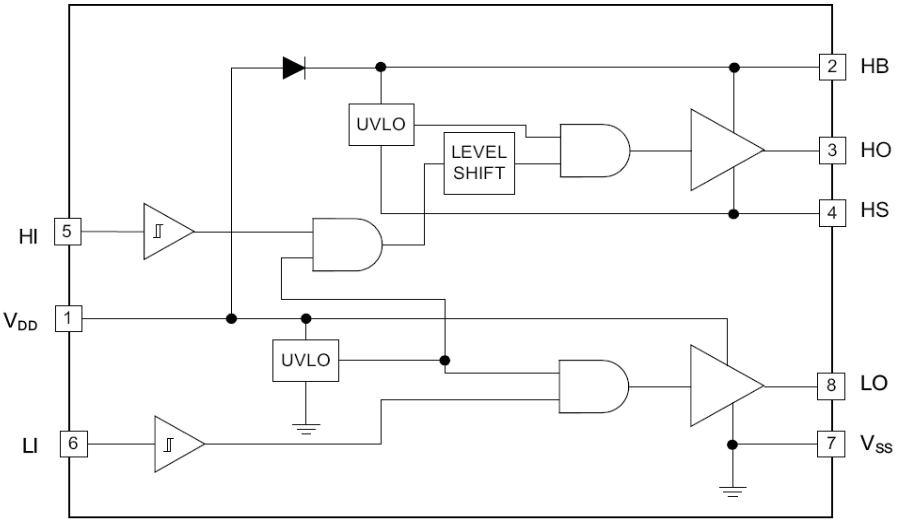
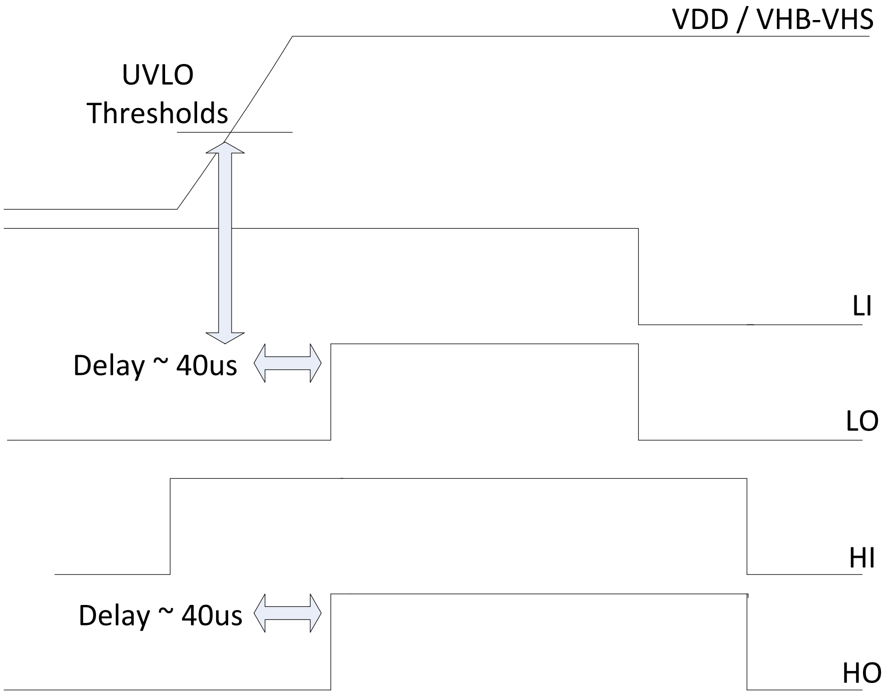


Figure 1. Internal Block Diagram

## Timing Diagrams



Note: If HI is set and the High−Side driver (VHB−VHS) crosses its UVLO threshold 100ns after the VDD UVLO then a rising edge on HI is required to pull HO High.

Figure 2. UVLO

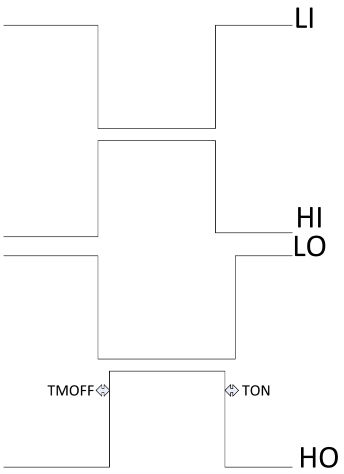


Figure 3. TMON and TMOFF

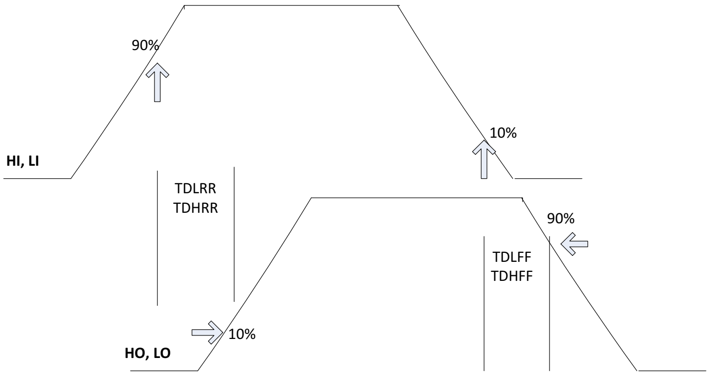
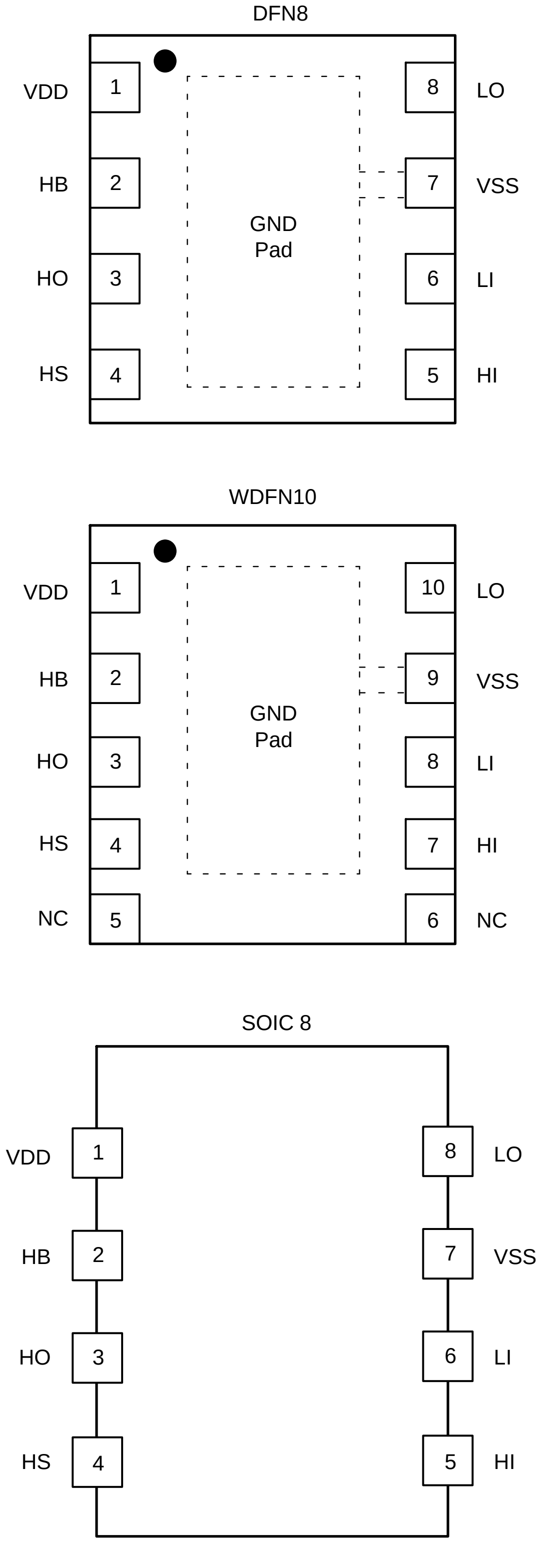


Figure 4. Propagation Delays

## LOGIC TABLE

| HI | LI | HO | LO |
|---|---|---|---|
| L | L | L | L |
| L | H | L | H |
| H | L | H | L |
| H | H | H | H |

## PINOUT DIAGRAMS



Note: The $V_{SS}$ Pin and the GND Pad are internally connected.

**Figure 5. NCP81075 Top View**

## TYPICAL CHARACTERISTICS

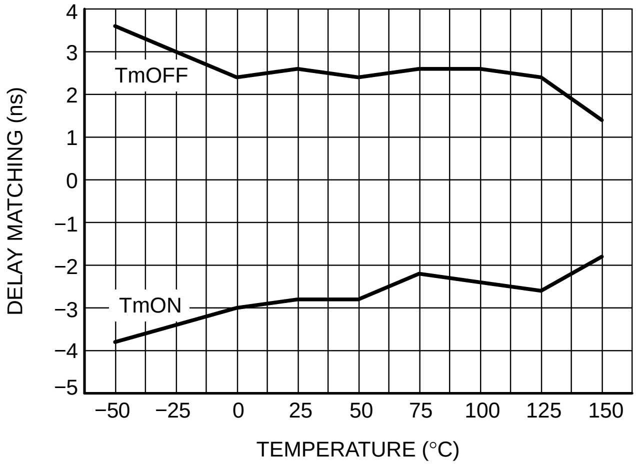


Figure 6. Delay Matching vs. Temperature

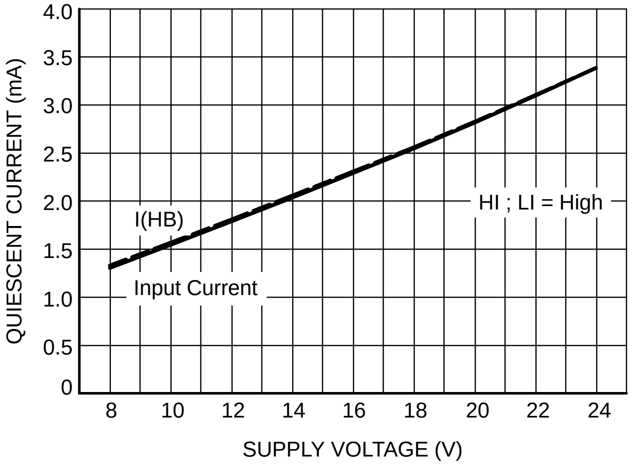


Figure 7. Quiescent Current vs. Supply Voltage High

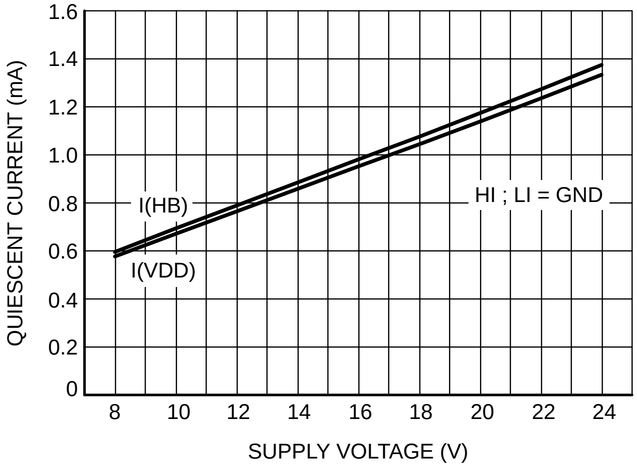


Figure 8. Quiescent Current vs. Supply Voltage Low

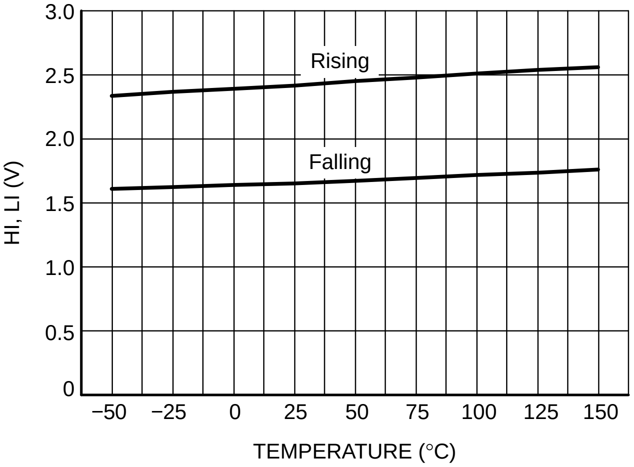


Figure 9. Input Threshold vs. Temperature

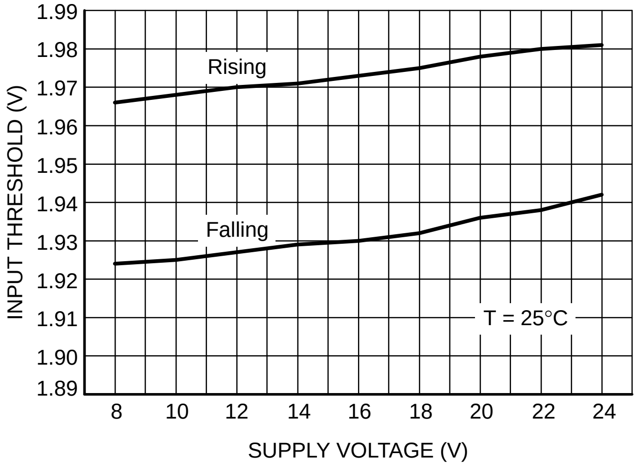


Figure 10. Input Threshold vs. Supply Voltage

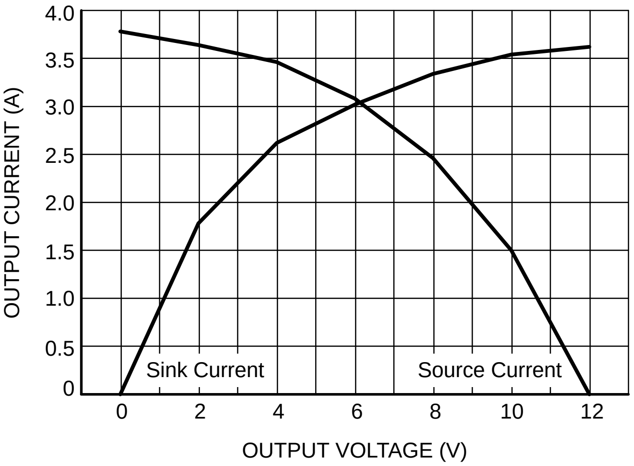


Figure 11. Output Current vs. Output Voltage

## TYPICAL CHARACTERISTICS

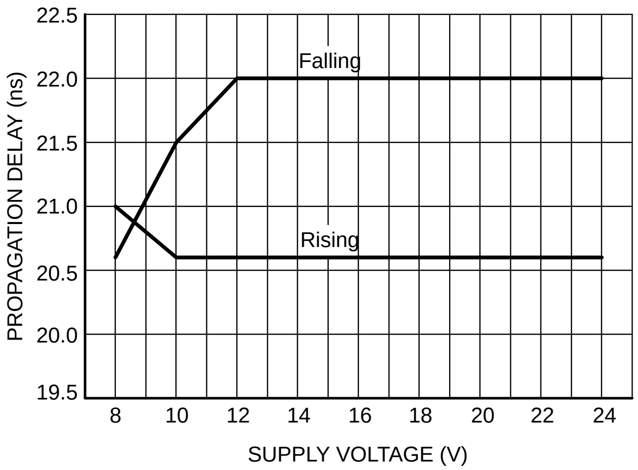


Figure 12. Propagation Delay vs. Supply Voltage

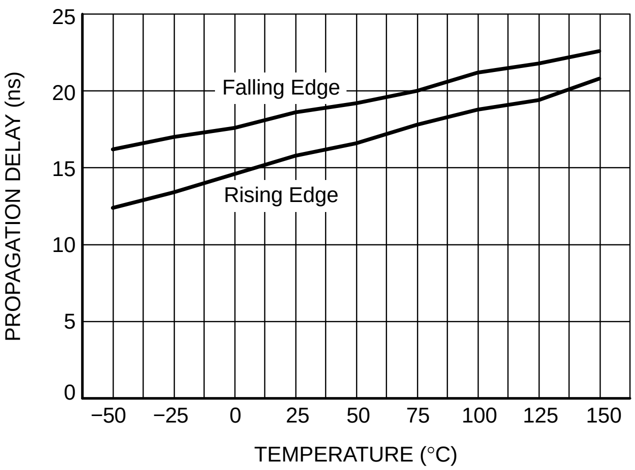


Figure 13. Propagation Delay vs. Temperature

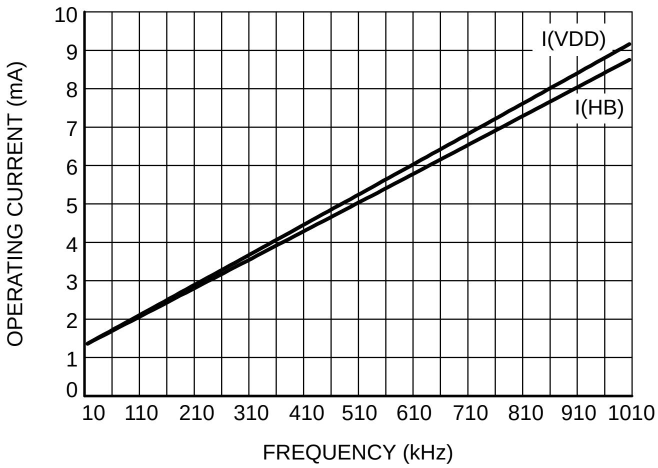


Figure 14. Operating Current vs. Frequency

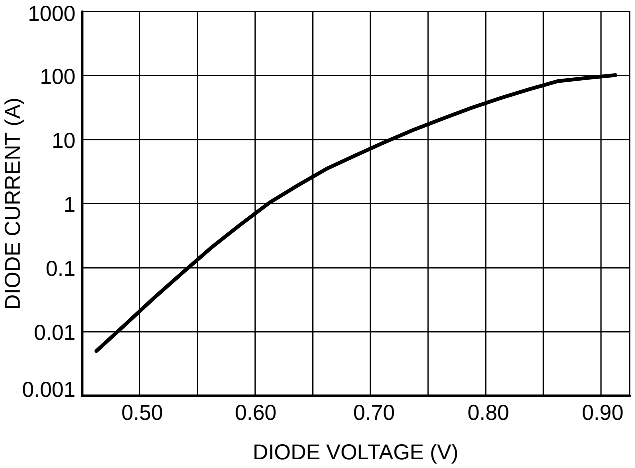


Figure 15. Diode Current vs. Diode Voltage

## APPLICATION INFORMATION

The NCP81075 is a high performance dual MOSFET gate driver optimized for driving the gates of both high side and low side power MOSFETs in a synchronous buck converter topology. A high and a Low input signals are all that is required to properly drive the high side and low side MOSFETs.

### Low−Side Driver

The low side driver is designed to drive low $RDS_{ON}$ N−channel MOSFETs. The typical output resistances for the driver are 1.5 ohms for sourcing and 1 ohm for sinking gate current. Due to the parasitic inductances of the packages, drive circuits and the nonlinearity of the MOSFETs output resistances the recorded peak current is close to 4 A.

The low output resistances allow the driver to have 8 ns rise and 7 ns fall times into a 1 nF load. When the driver is enabled, the driver's output is in phase with LI. When the NCP81075 is disabled, the low side gate is held low.

### High−Side Driver

The high side driver is designed to drive a floating low $RDS_{ON}$ N−channel MOSFET. The output resistances for the driver are 1.5 ohms for sourcing and 1 ohm for sinking gate current. The bias voltage for the high side driver is realized by an external bootstrap supply circuit which is connected between the HB and HS Pins.

The bootstrap circuit comprises only of the bootstrap capacitor since the bootstrap diode is internal. When the NCP81075 is starting up, the HS Pin is at ground, the bootstrap capacitor will charge up to VDD through the internal diode. When the HI goes high, the high side driver will begin to turn the high side MOSFET On by pulling charge out of the bootstrap capacitor. As the external MOSFET turns ON, the HS Pin will rise up to VIN, forcing the HB Pin to VIN + $V_{BstCap}$ which is enough gate to source voltage to hold the switch On. To complete the cycle, the MOSFET is switched OFF by pulling the gate down to the voltage at the HS Pin. When the low side MOSFET turns On, the HS Pin is pulled to ground. This allows the bootstrap capacitor to charge up to VDD again. The high−side driver's output is in phase with the HI input. When the driver is disabled, the high side gate is held low.

**The external BST resistor, which connects HB pin and BST cap, should avoid excessive resistance.** NCP81075 has high−side UVLO protection based on the voltage across HB and HS pins. High resistance on HB pin may falsely trigger UVLO protection at the moment when high−side MOSFET is turning on.

### UVLO (Under Voltage Lockout)

The bias supplies of the high−side and low−side drivers have UVLO protection. The VDD UVLO disables both drivers when the VDD voltage crosses the specified threshold. The typical rising threshold is 7.1 V with 0.58 V hysteresis. The VHB UVLO disables only the high−side driver when the VHB to VHS is below the specified threshold. The typical VHB UVLO rising threshold is 6.5 V with 0.5 V hysteresis. The designer must take into account a 40 μs delay before the output channels can react to a logic input. (Refer to the UVLO Timing Diagram).

### Input Stages

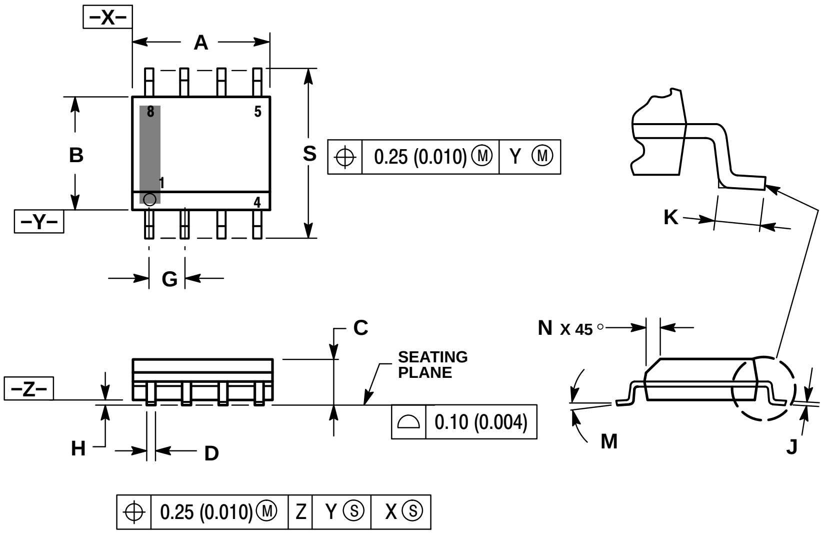
The input stage of the NCP81075 is TTL compatible. The logic rising threshold level is 2.4 V and the logic falling threshold is 1.6 V.

### Layout Guidelines

Gate drivers experience high di/dt during the switching transitions. So, the inductance at the gate drive traces must be minimized to avoid excessive ringing on the switch node. Gate drive traces should be kept as short and wide (> 20 mil) as practical. The input capacitor must be placed as close as possible to the IC. Connect the VSS pin of the NCP81075 as close as possible to the source of the lower MOSFET. The use of vias is highly desirable to maximize thermal conduction away from driver.

## PACKAGE DIMENSIONS

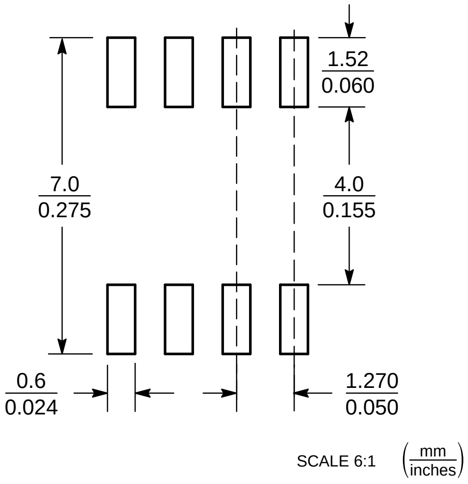
### SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

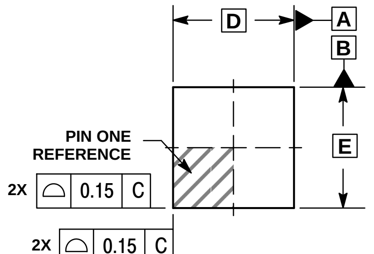
### SOLDERING FOOTPRINT*



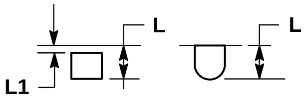
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

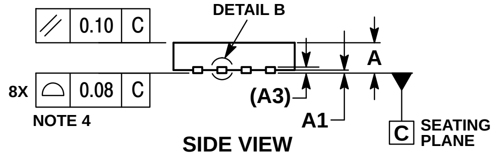
### DFN8, 4x4, 0.8P
CASE 506CY
ISSUE O



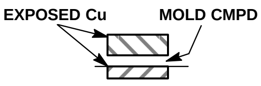
**TOP VIEW**



**DETAIL A**
OPTIONAL CONSTRUCTIONS



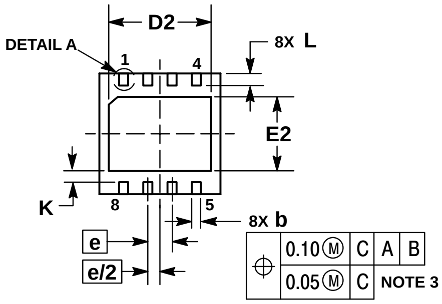
**SIDE VIEW**



**DETAIL B**
ALTERNATE CONSTRUCTION

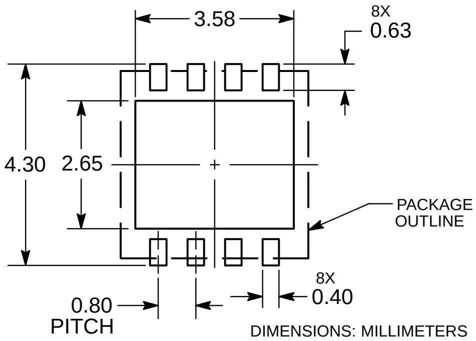
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 4.00 BSC | |
| D2 | 3.28 | 3.48 |
| E | 4.00 BSC | |
| E2 | 2.35 | 2.55 |
| e | 0.80 BSC | |
| K | 0.375 REF | |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |



**BOTTOM VIEW**

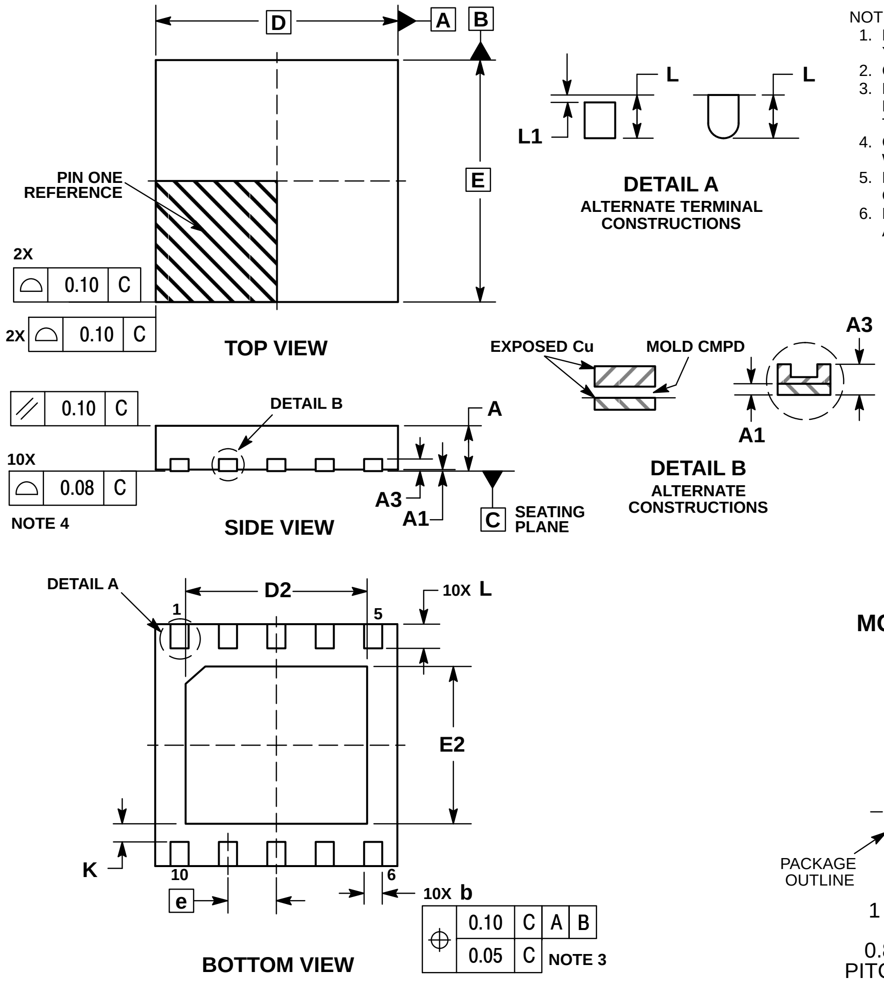
### RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

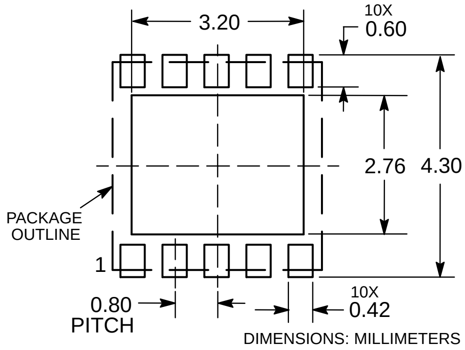
### WDFN10 4x4, 0.8P
CASE 511CE
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 4.00 BSC | |
| D2 | 2.90 | 3.10 |
| E | 4.00 BSC | |
| E2 | 2.50 | 2.70 |
| e | 0.80 BSC | |
| K | 0.30 REF | |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

### RECOMMENDED MOUNTING FOOTPRINT



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