

MSP430FR597x(1), MSP430FR592x(1) MSP430FR587x(1) Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Embedded Microcontroller
 - 16-Bit RISC Architecture up to 16-MHz Clock
 - Wide Supply Voltage Range (1.8 V to 3.6 V) ⁽¹⁾
- Optimized Ultra-Low-Power Modes
 - Active Mode: Approximately 100 μ A/MHz
 - Standby (LPM3 With VLO): 0.4 μ A (Typical)
 - Real-Time Clock (RTC) (LPM3.5): 0.35 μ A (Typical) ⁽²⁾
 - Shutdown (LPM4.5): 0.04 μ A (Typical)
- Ultra-Low-Power Ferroelectric RAM (FRAM)
 - Up to 64KB of Nonvolatile Memory
 - Ultra-Low-Power Writes
 - Fast Write at 125 ns per Word (64KB in 4 ms)
 - Unified Memory = Program + Data + Storage in One Single Space
 - 10^{15} Write Cycle Endurance
 - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
 - 32-Bit Hardware Multiplier (MPY)
 - Three-Channel Internal Direct Memory Access (DMA)
 - RTC With Calendar and Alarm Functions
 - Five 16-Bit Timers With up to Seven Capture/Compare Registers
 - 16-Bit and 32-Bit Cyclic Redundancy Checker (CRC16, CRC32)
- High-Performance Analog
 - Up to 8-Channel Analog Comparator
 - 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference and Sample-and-Hold and up to 8 External Input Channels
- Code Security and Encryption
 - 128-Bit or 256-Bit AES Security Encryption and Decryption Coprocessor (MSP430FR59xx(1) Only)
- True Random Number Seed for Random Number Generation Algorithm
- Lockable Memory Segments for IP Encapsulation and Secure Storage
- Multifunction Input/Output Ports
 - All I/O Pins Support Capacitive Touch Capability Without Need for External Components
 - Accessible Bit-, Byte- and Word-Wise (in Pairs)
 - Edge-Selectable Wakeup From LPM on Ports P1, P2, P3, and P4
 - Programmable Pullup and Pulldown on All Ports
- Enhanced Serial Communication
 - eUSCI_A0 and eUSCI_A1 Support:
 - UART With Automatic Baud-Rate Detection
 - IrDA Encode and Decode
 - SPI at Rates up to 10 Mbps
 - eUSCI_B0 and eUSCI_B1 Support:
 - I²C With Multiple-Slave Addressing
 - SPI at Rates up to 10 Mbps
- Flexible Clock System
 - Fixed-Frequency DCO With 10 Selectable Factory-Trimmed Frequencies
 - Low-Power Low-Frequency Internal Clock Source (VLO)
 - 32-kHz Crystals (LFXT)
 - High-Frequency Crystals (HFXT)
- Development Tools and Software
 - Free Professional Development Environments With [EnergyTrace++™](#) Technology for Power Profiling and Debugging
 - Microcontroller Development Boards Available
- Family Members
 - [Section 3](#) Summarizes the Available Variants and Packages
- For Complete Module Descriptions, See the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* ([SLAU367](#))

(1) Minimum supply voltage is restricted by SVS levels.

(2) The RTC is clocked by a 3.7-pF crystal.



1.2 Applications

- Metering
- Energy Harvested Sensor Nodes
- Wearable Electronics
- Sensor Management
- Data Logging

1.3 Description

This ultra-low-power MSP430FRxx FRAM microcontroller family consists of several devices featuring embedded nonvolatile FRAM, a 16-bit CPU, and different sets of peripherals targeted for various applications. The architecture, FRAM, and peripherals, combined with seven low-power modes, are optimized to achieve extended battery life in portable and wireless sensing applications. FRAM is a new nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption.

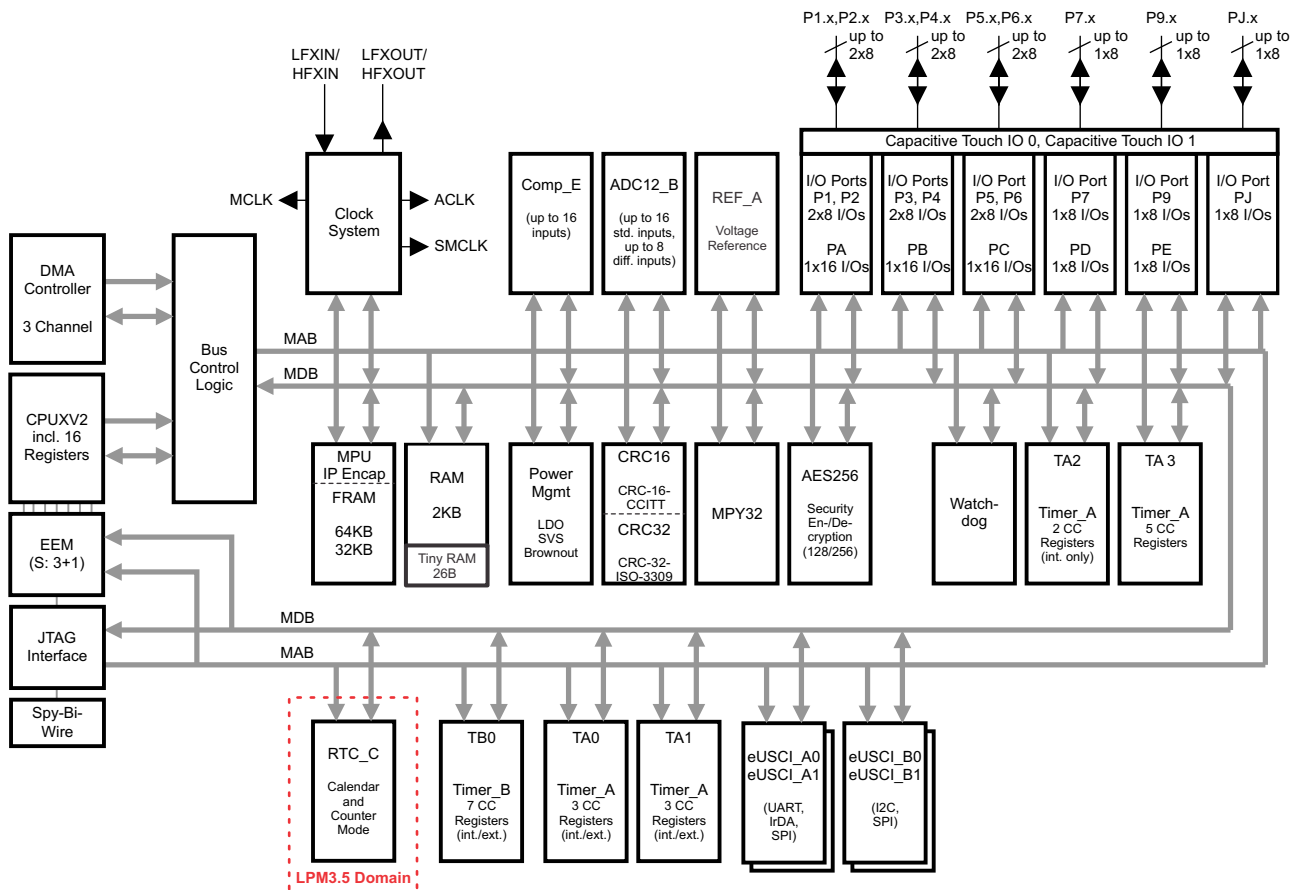
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE ⁽²⁾
MSP430FR5972IPMR	LQFP (64)	10 mm x 10 mm
MSP430FR5972IRGC	VQFN (64)	9 mm x 9 mm
MSP430FR5922IG56	TSSOP (56)	6.1 mm x 14 mm

- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 9](#), or see the TI website at www.ti.com.
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 9](#).

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.



NOTE: AES256 is not implemented in the MSP430FR587x and MSP430FR587x1 devices.

NOTE: HFXIN and HFXOUT are not implemented in the MSP430FR592x and MSP430FR592x1 devices.

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 28, 2015 to May 1, 2015

Page

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- Removed 48KB FRAM option from [Figure 1-1, Functional Block Diagram](#) [3](#)
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3 Device Comparison

Table 3-1 and Table 3-2 summarize the available family members.

Table 3-1. Device Comparison – Family Members With UART BSL

DEVICE	FRAM (KB)	SRAM (KB)	CLOCK SYSTEM	Timer_A ⁽¹⁾	Timer_B ⁽²⁾	eUSCI		AES	ADC12_B	I/O	PACKAGE TYPE
						A ⁽³⁾	B ⁽⁴⁾				
MSP430FR5972	64	2	DCO HFXT LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	yes	8 ext	51	64 PM 64 RGC
MSP430FR5872	64	2	DCO HFXT LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	no	8 ext	51	64 PM 64 RGC
MSP430FR5970	32	2	DCO HFXT LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	yes	8 ext	51	64 PM 64 RGC
MSP430FR5922	64	2	DCO LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	yes	8 ext	51 46 (DGG)	64 PM 64 RGC 56 DGG
MSP430FR5870	32	2	DCO HFXT LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	no	8 ext	51	64 PM 64 RGC

- (1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (3) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
- (4) eUSCI_B supports I²C with multiple slave addresses and SPI.
- (5) Timer_A TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
- (6) Timer_A TA2 provides only internal capture/compare inputs and only internal PWM outputs (if any).
- (7) Timer_A TA3 provides only internal capture/compare inputs and only internal PWM outputs (if any) for FR592x(1) with RGC and PM packages. For FR592x(1) with DGG package and all other devices, Timer_A TA3 provides internal, external capture/compare inputs and internal, external PWM outputs (if any).

Table 3-2. Device Comparison – Family Members With I²C BSL

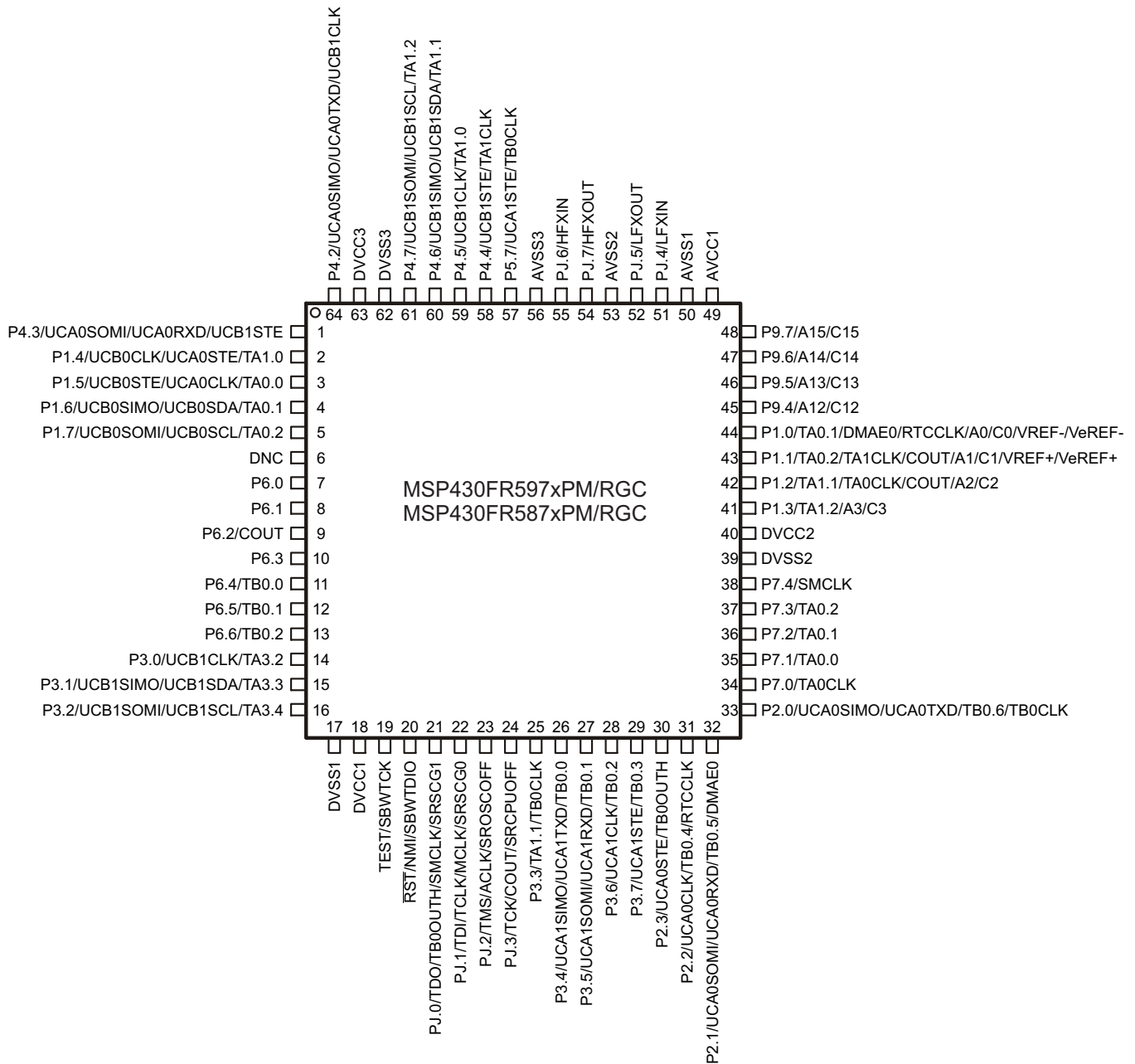
DEVICE	FRAM (KB)	SRAM (KB)	CLOCK SYSTEM	Timer_A ⁽¹⁾	Timer_B ⁽²⁾	eUSCI		AES	ADC12_B	I/O	PACKAGE TYPE
						A ⁽³⁾	B ⁽⁴⁾				
MSP430FR59721	64	2	DCO HFXT LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	yes	8 ext	51	64 PM 64 RGC
MSP430FR59221	64	2	DCO LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	yes	8 ext	51 46 (DGG)	64 PM 64 RGC 56 DGG
MSP430FR58721	64	2	DCO HFXT LFXT	3, 3 ⁽⁵⁾ 2, 5 ⁽⁶⁾⁽⁷⁾	7	2	2	no	8 ext	51	64 PM 64 RGC

- (1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
- (3) eUSCI_A supports UART with automatic baud-rate detection, IrDA encode and decode, and SPI.
- (4) eUSCI_B supports I²C with multiple slave addresses and SPI.
- (5) Timer_A TA0 and TA1 provide internal and external capture/compare inputs and internal and external PWM outputs.
- (6) Timer_A TA2 provides only internal capture/compare inputs and only internal PWM outputs (if any).
- (7) Timer_A TA3 provides only internal capture/compare inputs and only internal PWM outputs (if any) for FR592x(1) with RGC and PM packages. For FR592x(1) with DGG package and all other devices, Timer_A TA3 provides internal, external capture/compare inputs and internal, external PWM outputs (if any).

4 Terminal Configuration and Functions

4.1 Pin Diagrams

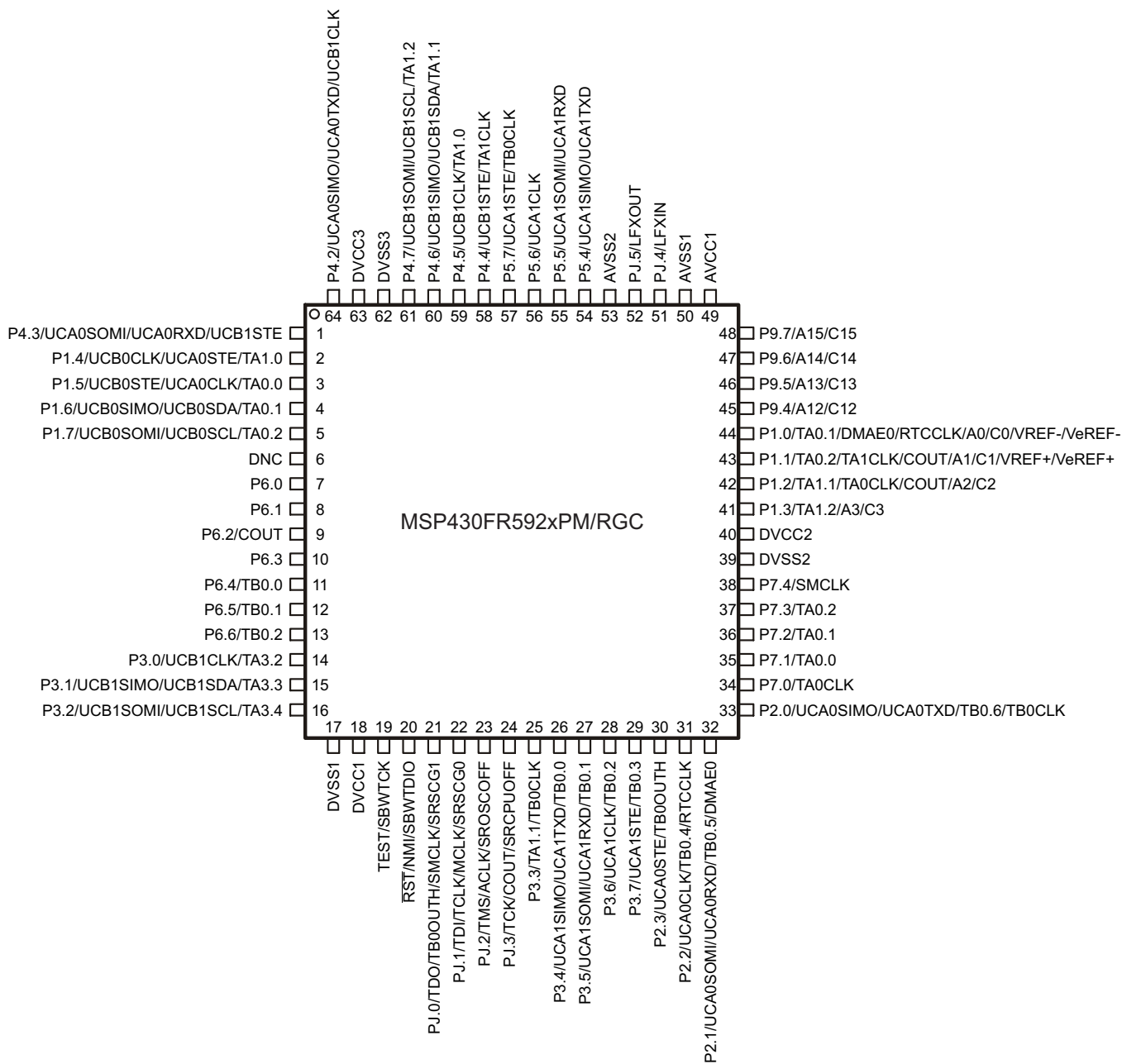
Figure 4-1 shows the pin assignments for the 64-pin PM and RGC packages of the MSP430FR597x(1) and MSP430FR587x(1).



On devices with UART BSL: P2.0: BSL_TX; P2.1: BSL_RX
On devices with I²C BSL: P1.6: BSL_DAT; P1.7: BSL_CLK

Figure 4-1. 64-Pin PM and RGC Packages (Top View) – MSP430FR597x(1), MSP430FR587x(1)

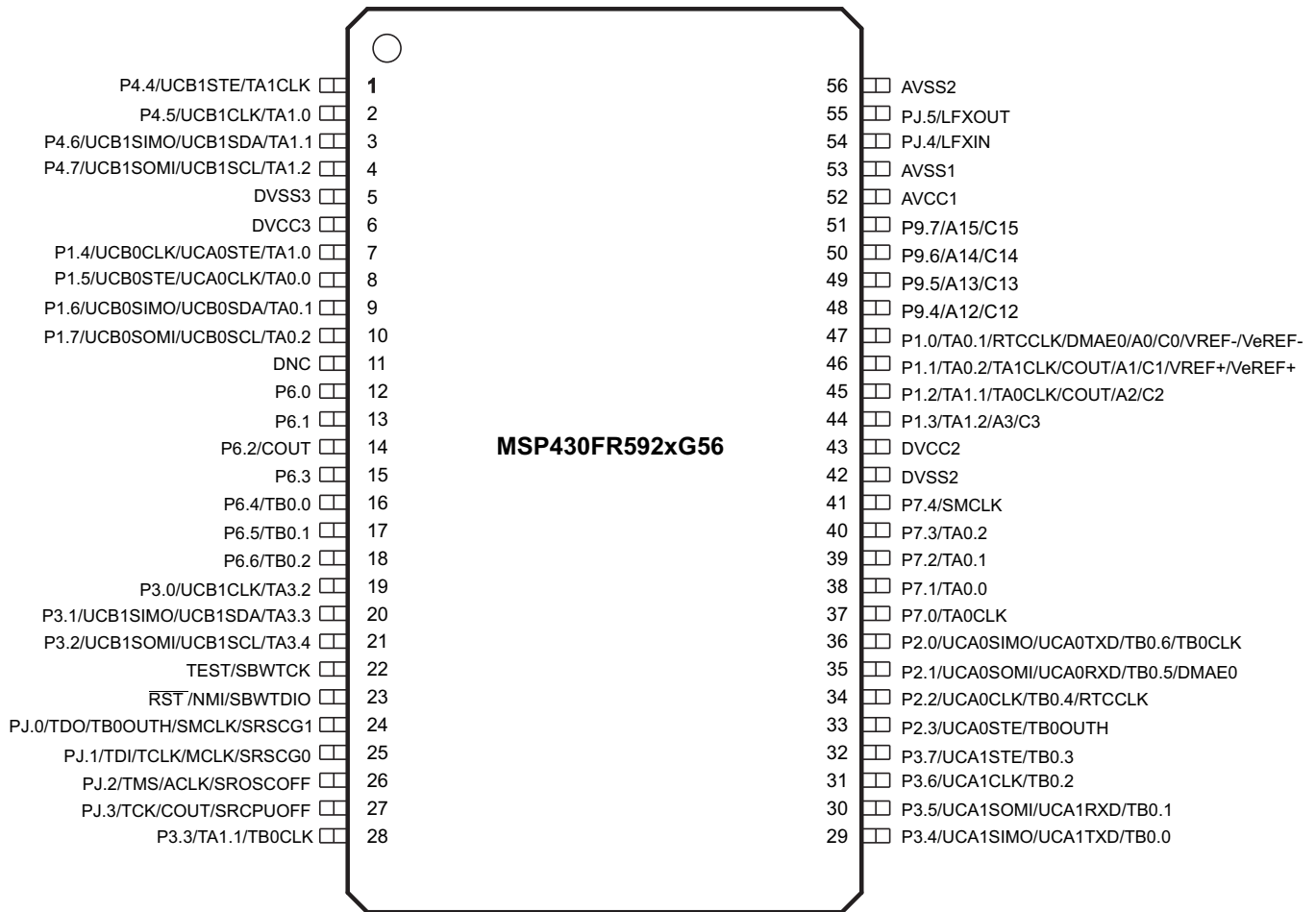
Figure 4-2 shows the pin assignments for the 64-pin PM and RGC packages of the MSP430FR592x(1).



- A. On devices with UART BSL: P2.0: BSL_TX; P2.1: BSL_RX
On devices with I²C BSL: P1.6: BSL_DAT; P1.7: BSL_CLK

Figure 4-2. 64-Pin PM and RGC Packages (Top View) – MSP430FR592x(1)

Figure 4-3 shows the pin assignments for the 56-pin DGG package of the MSP430FR592x(1).



- A. On devices with UART BSL: P2.0: BSL_TX; P2.1: BSL_RX
On devices with I²C BSL: P1.6: BSL_DAT; P1.7: BSL_CLK

Figure 4-3. 56-Pin DGG Package (Top View) – MSP430FR592x(1)

4.2 Pin Attributes

Table 4-1 lists the attributes of each pin.

Table 4-1. Pin Attributes

FR597x(1), FR587x(1)	FR592x(1)		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE	RESET STATE AFTER BOR ⁽⁵⁾	
	PM, RGC	PM, RGC						DGG
	PIN NO.	PIN NO.						PIN NO.
1	1		P4.3 (RD)	I/O	LVC MOS	DVCC	OFF	
			UCA0SOMI	I/O	LVC MOS	DVCC	-	
			UCA0RXD	I	LVC MOS	DVCC	-	
			UCB1STE	I/O	LVC MOS	DVCC	-	
2	2	7	P1.4 (RD)	I/O	LVC MOS	DVCC	OFF	
			UCB0CLK	I/O	LVC MOS	DVCC	-	
			UCA0STE	I/O	LVC MOS	DVCC	-	
			TA1.0	I/O	LVC MOS	DVCC	-	
3	3	8	P1.5 (RD)	I/O	LVC MOS	DVCC	OFF	
			UCB0STE	I/O	LVC MOS	DVCC	-	
			UCA0CLK	I/O	LVC MOS	DVCC	-	
			TA0.0	I/O	LVC MOS	DVCC	-	
4	4	9	P1.6 (RD)	I/O	LVC MOS	DVCC	OFF	
			UCB0SIMO	I/O	LVC MOS	DVCC	-	
			UCB0SDA	I/O	LVC MOS	DVCC	-	
			BSL_DAT	I	LVC MOS	DVCC	-	
			TA0.1	I/O	LVC MOS	DVCC	-	
5	5	10	P1.7 (RD)	I/O	LVC MOS	DVCC	OFF	
			UCB0SOMI	I/O	LVC MOS	DVCC	-	
			UCB0SCL	I/O	LVC MOS	DVCC	-	
			BSL_CLK	I	LVC MOS	DVCC	-	
			TA0.2	I/O	LVC MOS	DVCC	-	
6	6	11	DNC ⁽⁶⁾	-	-	-	-	
7	7	12	P6.0 (RD)	I/O	LVC MOS	DVCC	OFF	
8	8	13	P6.1 (RD)	I/O	LVC MOS	DVCC	OFF	
9	9	14	P6.2 (RD)	I/O	LVC MOS	DVCC	OFF	
			COUT	O	LVC MOS	DVCC	-	
10	10	15	P6.3 (RD)	I/O	LVC MOS	DVCC	OFF	
11	11	16	P6.4 (RD)	I/O	LVC MOS	DVCC	OFF	
			TB0.0	I/O	LVC MOS	DVCC	-	
12	12	17	P6.5 (RD)	I/O	LVC MOS	DVCC	OFF	
			TB0.1	I/O	LVC MOS	DVCC	-	

- (1) Signals names with (RD) denote the reset default pin name.
(2) To determine the pin mux encodings for each pin, refer to the *Port I/O Schematics* section.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output.
(4) Buffer Types: LVC MOS, Analog, or Power (see Table 4-3 for details)
(5) Reset States:
OFF = High-impedance input with pullup or pulldown disabled (if available)
PD = High-impedance input with pulldown enabled
PU = High-impedance input with pullup enabled
DRIVE0 = Drive output low
DRIVE1 = Drive output high
N/A = Not applicable
(6) DNC = Do not connect

Table 4-1. Pin Attributes (continued)

FR597x(1), FR587x(1)	FR592x(1)		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE	RESET STATE AFTER BOR ⁽⁵⁾
	PM, RGC	DGG					
	PIN NO.	PIN NO.					
13	13	18	P6.6 (RD)	I/O	LVC MOS	DVCC	OFF
			TB0.2	I/O	LVC MOS	DVCC	-
14	14	19	P3.0 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1CLK	I/O	LVC MOS	DVCC	-
			TA3.2	I/O	LVC MOS	DVCC	-
15	15	20	P3.1 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SIMO	I/O	LVC MOS	DVCC	-
			UCB1SDA	I/O	LVC MOS	DVCC	-
			TA3.3	I/O	LVC MOS	DVCC	-
16	16	21	P3.2 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SOMI	I/O	LVC MOS	DVCC	-
			UCB1SCL	I/O	LVC MOS	DVCC	-
			TA3.4	I/O	LVC MOS	DVCC	-
17	17		DVSS1	P	Power	-	N/A
18	18		DVCC1	P	Power	-	N/A
19	19	22	TEST	I	LVC MOS	DVCC	OFF
			SBWTCK	I	LVC MOS	DVCC	-
20	20	23	$\overline{\text{RST}}$	I	LVC MOS	DVCC	OFF
			NMI	I	LVC MOS	DVCC	-
			SBWTDIO	I/O	LVC MOS	DVCC	-
21	21	24	PJ.0 (RD)	I/O	LVC MOS	DVCC	OFF
			TDO	O	LVC MOS	DVCC	-
			TB0OUTH	I	LVC MOS	DVCC	-
			SMCLK	O	LVC MOS	DVCC	-
			SRSCG1	O	LVC MOS	DVCC	-
22	22	25	PJ.1 (RD)	I/O	LVC MOS	DVCC	OFF
			TDI	I	LVC MOS	DVCC	-
			TCLK	I	LVC MOS	DVCC	-
			MCLK	O	LVC MOS	DVCC	-
			SRSCG0	O	LVC MOS	DVCC	-
23	23	26	PJ.2 (RD)	I/O	LVC MOS	DVCC	OFF
			TMS	I	LVC MOS	DVCC	-
			ACLK	O	LVC MOS	DVCC	-
			SROSCOFF	O	LVC MOS	DVCC	-
24	24	27	PJ.3 (RD)	I/O	LVC MOS	DVCC	OFF
			TCK	I	LVC MOS	DVCC	-
			COUT	O	LVC MOS	DVCC	-
			SRCPUOFF	O	LVC MOS	DVCC	-
25	25	28	P3.3 (RD)	I/O	LVC MOS	DVCC	OFF
			TA1.1	I/O	LVC MOS	DVCC	-
			TB0CLK	I	LVC MOS	DVCC	-
26	26	29	P3.4 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1SIMO	I/O	LVC MOS	DVCC	-
			UCA1TXD	O	LVC MOS	DVCC	-
			TB0.0	I/O	LVC MOS	DVCC	-

Table 4-1. Pin Attributes (continued)

FR597x(1), FR587x(1)	FR592x(1)		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE	RESET STATE AFTER BOR ⁽⁵⁾
	PM, RGC	DGG					
	PIN NO.	PIN NO.					
27	27	30	P3.5 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1SOMI	I/O	LVC MOS	DVCC	-
			UCA1RXD	I	LVC MOS	DVCC	-
			TB0.1	I/O	LVC MOS	DVCC	-
28	28	31	P3.6 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1CLK	I/O	LVC MOS	DVCC	-
			TB0.2	I/O	LVC MOS	DVCC	-
29	29	32	P3.7 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1STE	I/O	LVC MOS	DVCC	-
			TB0.3	I/O	LVC MOS	DVCC	-
30	30	33	P2.3 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0STE	I/O	LVC MOS	DVCC	-
			TB0OUTH	I	LVC MOS	DVCC	-
31	31	34	P2.2 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0CLK	I/O	LVC MOS	DVCC	-
			TB0.4	I/O	LVC MOS	DVCC	-
			RTCCLK	O	LVC MOS	DVCC	-
32	32	35	P2.1 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0SOMI	I/O	LVC MOS	DVCC	-
			UCA0RXD	I	LVC MOS	DVCC	-
			BSL_RX	I	LVC MOS	DVCC	-
			TB0.5	I/O	LVC MOS	DVCC	-
			DMAE0	I	LVC MOS	DVCC	-
33	33	36	P2.0 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0SIMO	I/O	LVC MOS	DVCC	-
			UCA0TXD	O	LVC MOS	DVCC	-
			BSL_TX	O	LVC MOS	DVCC	-
			TB0.6	I/O	LVC MOS	DVCC	-
			TB0CLK	I	LVC MOS	DVCC	-
34	34	37	P7.0 (RD)	I/O	LVC MOS	DVCC	OFF
			TA0CLK	I	LVC MOS	DVCC	-
35	35	38	P7.1 (RD)	I/O	LVC MOS	DVCC	OFF
			TA0.0	I/O	LVC MOS	DVCC	-
36	36	39	P7.2 (RD)	I/O	LVC MOS	DVCC	OFF
			TA0.1	I/O	LVC MOS	DVCC	-
37	37	40	P7.3 (RD)	I/O	LVC MOS	DVCC	OFF
			TA0.2	I/O	LVC MOS	DVCC	-
38	38	41	P7.4 (RD)	I/O	LVC MOS	DVCC	OFF
			SMCLK	O	LVC MOS	DVCC	-
39	39	42	DVSS2	P	Power	-	N/A
40	40	43	DVCC2	P	Power	-	N/A
41	41	44	P1.3 (RD)	I/O	LVC MOS	DVCC	OFF
			TA1.2	I/O	LVC MOS	DVCC	-
			A3	I	Analog	AVCC	-
			C3	I	Analog	AVCC	-

Table 4-1. Pin Attributes (continued)

FR597x(1), FR587x(1)	FR592x(1)		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE	RESET STATE AFTER BOR ⁽⁵⁾
	PM, RGC	DGG					
	PIN NO.	PIN NO.					
42	42	45	P1.2 (RD)	I/O	LVC MOS	DVCC	OFF
			TA1.1	I/O	LVC MOS	DVCC	-
			TA0CLK	I	LVC MOS	DVCC	-
			COU T	O	LVC MOS	DVCC	-
			A2	I	Analog	AVCC	-
			C2	I	Analog	AVCC	-
43	43	46	P1.1 (RD)	I/O	LVC MOS	DVCC	OFF
			TA0.2	I/O	LVC MOS	DVCC	-
			TA1CLK	I	LVC MOS	DVCC	-
			COU T	O	LVC MOS	DVCC	-
			A1	I	Analog	AVCC	-
			C1	I	Analog	AVCC	-
			VREF+	O	Analog	AVCC	-
			VeREF+	I	Analog	-	-
44	44	47	P1.0 (RD)	I/O	LVC MOS	DVCC	OFF
			TA0.1	I/O	LVC MOS	DVCC	-
			DM AE0	I	LVC MOS	DVCC	-
			RTCCLK	O	LVC MOS	DVCC	-
			A0	I	Analog	AVCC	-
			C0	I	Analog	AVCC	-
			VREF-	O	Analog	AVCC	-
			VeREF-	I	Analog	-	-
45	45	48	P9.4 (RD)	I/O	LVC MOS	DVCC	OFF
			A12	I	Analog	AVCC	-
			C12	I	Analog	AVCC	-
46	46	49	P9.5 (RD)	I/O	LVC MOS	DVCC	OFF
			A13	I	Analog	AVCC	-
			C13	I	Analog	AVCC	-
47	47	50	P9.6 (RD)	I/O	LVC MOS	DVCC	OFF
			A14	I	Analog	AVCC	-
			C14	I	Analog	AVCC	-
48	48	51	P9.7 (RD)	I/O	LVC MOS	DVCC	OFF
			A15	I	Analog	AVCC	-
			C15	I	Analog	AVCC	-
49	49	52	AVCC1	P	Power	-	N/A
50	50	53	AVSS1	P	Power	-	N/A
51	51	54	PJ.4 (RD)	I/O	LVC MOS	DVCC	OFF
			LFXIN	I	Analog	AVCC	-
52	52	55	PJ.5 (RD)	I/O	LVC MOS	DVCC	OFF
			LFXOUT	O	Analog	AVCC	-
53	53	56	AVSS2	P	Power	-	N/A
54			PJ.7 (RD)	I/O	LVC MOS	DVCC	OFF
			HFXOUT	O	Analog	AVCC	-
55			PJ.6 (RD)	I/O	LVC MOS	DVCC	OFF
			HFXIN	I	Analog	AVCC	-

Table 4-1. Pin Attributes (continued)

FR597x(1), FR587x(1)	FR592x(1)		SIGNAL NAME ^{(1) (2)}	SIGNAL TYPE ⁽³⁾	BUFFER TYPE ⁽⁴⁾	POWER SOURCE	RESET STATE AFTER BOR ⁽⁵⁾
	PM, RGC	DGG					
	PIN NO.	PIN NO.					
56			AVSS3	P	Power	-	N/A
	54		P5.4 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1SIMO	I/O	LVC MOS	DVCC	-
			UCA1TXD	O	LVC MOS	DVCC	-
	55		P5.5 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1SOMI	I/O	LVC MOS	DVCC	-
			UCA1RXD	I	LVC MOS	DVCC	-
	56		P5.6 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1CLK	I/O	LVC MOS	DVCC	-
57	57		P5.7 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA1STE	I/O	LVC MOS	DVCC	-
			TB0CLK	I	LVC MOS	DVCC	-
58	58	1	P4.4 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1STE	I/O	LVC MOS	DVCC	-
			TA1CLK	I	LVC MOS	DVCC	-
59	59	2	P4.5 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1CLK	I/O	LVC MOS	DVCC	-
			TA1.0	I/O	LVC MOS	DVCC	-
60	60	3	P4.6 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SIMO	I/O	LVC MOS	DVCC	-
			UCB1SDA	I/O	LVC MOS	DVCC	-
			TA1.1	I/O	LVC MOS	DVCC	-
61	61	4	P4.7 (RD)	I/O	LVC MOS	DVCC	OFF
			UCB1SOMI	I/O	LVC MOS	DVCC	-
			UCB1SCL	I/O	LVC MOS	DVCC	-
			TA1.2	I/O	LVC MOS	DVCC	-
62	62	5	DVSS3	P	Power	-	N/A
63	63	6	DVCC3	P	Power	-	N/A
64	64		P4.2 (RD)	I/O	LVC MOS	DVCC	OFF
			UCA0SIMO	I/O	LVC MOS	DVCC	-
			UCA0TXD	O	LVC MOS	DVCC	-
			UCB1CLK	I/O	LVC MOS	DVCC	-

4.3 Signal Descriptions

Table 4-2 describes the signals.

Table 4-2. Signal Descriptions

FUNCTION	SIGNAL NAME	FR597x(1), FR587x(1)	FR592x(1)		SIGNAL TYPE	DESCRIPTION
		PM, RGC	PM, RGC	DGG		
		PIN NO.	PIN NO.	PIN NO.		
ADC	A0	44	44	47	I	Analog input A0
	A1	43	43	46	I	Analog input A1
	A2	42	42	45	I	Analog input A2
	A3	41	41	44	I	Analog input A3
	A12	45	45	48	I	Analog input A12
	A13	46	46	49	I	Analog input A13
	A14	47	47	50	I	Analog input A14
	A15	48	48	51	I	Analog input A15
	VREF+	43	43	46	O	Output of positive reference voltage
	VREF-	44	44	47	O	Output of negative reference voltage
	VeREF+	43	43	46	I	Input for an external positive reference voltage to the ADC
	VeREF-	44	44	47	I	Input for an external negative reference voltage to the ADC
BSL (I ² C)	BSL_CLK	5	5	10	I	BSL Clock (I ² C BSL)
	BSL_DAT	4	4	9	I	BSL Data (I ² C BSL)
BSL (UART)	BSL_RX	32	32	35	I	BSL Receive (UART BSL)
	BSL_TX	33	33	36	O	BSL Transmit (UART BSL)
Clock	ACLK	23	23	26	O	ACLK output
	HFXIN	55			I	Input terminal of crystal oscillator XT2
	HFXOUT	54			O	Output terminal for crystal oscillator XT2
	LFXIN	51	51	54	I	Input terminal for crystal oscillator XT1
	LFXOUT	52	52	55	O	Output terminal of crystal oscillator XT1
	MCLK	22	22	25	O	MCLK output
	RTCCLK	31 44	31 44	34 47	O	RTC clock output for calibration
Comparator	C0	44	44	47	I	Comparator input C0
	C1	43	43	46	I	Comparator input C1
	C2	42	42	45	I	Comparator input C2
	C3	41	41	44	I	Comparator input C3
	C12	45	45	48	I	Comparator input C12
	C13	46	46	49	I	Comparator input C13
	C14	47	47	50	I	Comparator input C14
	C15	48	48	51	I	Comparator input C15
	COUT	9 24 42 43	9 24 42 43	14 27 45 46	O	Comparator output
DMA	DMAE0	32 44	32 44	32 44	I	DMA external trigger input
DNC	DNC	6	6	22	-	Do Not Connect (DNC). It is strongly recommended to leave this pin not connected.

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	FR597x(1), FR587x(1)	FR592x(1)		SIGNAL TYPE	DESCRIPTION
		PM, RGC	PM, RGC	DGG		
		PIN NO.	PIN NO.	PIN NO.		
Debug	SBWTCK	19	19	23	I	Spy-Bi-Wire input clock
	SBWTDIO	20	20	27	I/O	Spy-Bi-Wire data input/output
	SRCPUOFF	24	24	26	O	Low-power debug: CPU status register CPUOFF
	SROSCOFF	23	23	25	O	Low-power debug: CPU status register OSCOFF
	SRSCG0	22	22	24	O	Low-power debug: CPU status register SCG0
	SRSCG1	21	21	27	O	Low-power debug: CPU status register SCG1
	TCK	24	24	25	I	Test clock
	TCLK	22	22	25	I	Test clock input
	TDI	22	22	24	I	Test data input
	TDO	21	21	22	O	Test data output port
	TEST	19	19	26	I	Test mode pin - select digital I/O on JTAG pins
	TMS	23	23	23	I	Test mode select
GPIO	P1.0	44	44	47	I/O	General-purpose digital I/O
	P1.1	43	43	46	I/O	General-purpose digital I/O
	P1.2	42	42	45	I/O	General-purpose digital I/O
	P1.3	41	41	44	I/O	General-purpose digital I/O
	P1.4	2	2	7	I/O	General-purpose digital I/O
	P1.5	3	3	8	I/O	General-purpose digital I/O
	P1.6	4	4	9	I/O	General-purpose digital I/O
	P1.7	5	5	10	I/O	General-purpose digital I/O
	P2.0	33	33	36	I/O	General-purpose digital I/O
	P2.1	32	32	35	I/O	General-purpose digital I/O
	P2.2	31	31	34	I/O	General-purpose digital I/O
	P2.3	30	30	33	I/O	General-purpose digital I/O
	P3.0	14	14	19	I/O	General-purpose digital I/O
	P3.1	15	15	20	I/O	General-purpose digital I/O
	P3.2	16	16	21	I/O	General-purpose digital I/O
	P3.3	25	25	28	I/O	General-purpose digital I/O
	P3.4	26	26	29	I/O	General-purpose digital I/O
	P3.5	27	27	30	I/O	General-purpose digital I/O
	P3.6	28	28	31	I/O	General-purpose digital I/O
	P3.7	29	29	32	I/O	General-purpose digital I/O
	P4.2	64	64		I/O	General-purpose digital I/O
	P4.3	1	1		I/O	General-purpose digital I/O
	P4.4	58	58	1	I/O	General-purpose digital I/O
	P4.5	59	59	2	I/O	General-purpose digital I/O
	P4.6	60	60	3	I/O	General-purpose digital I/O
	P4.7	61	61	4	I/O	General-purpose digital I/O
	P5.4		54		I/O	General-purpose digital I/O
	P5.5		55		I/O	General-purpose digital I/O
P5.6		56		I/O	General-purpose digital I/O	
P5.7	57	57		I/O	General-purpose digital I/O	

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	FR597x(1), FR587x(1)	FR592x(1)		SIGNAL TYPE	DESCRIPTION
		PM, RGC	PM, RGC	DGG		
		PIN NO.	PIN NO.	PIN NO.		
GPIO	P6.0	7	7	12	I/O	General-purpose digital I/O
	P6.1	8	8	13	I/O	General-purpose digital I/O
	P6.2	9	9	14	I/O	General-purpose digital I/O
	P6.3	10	10	15	I/O	General-purpose digital I/O
	P6.4	11	11	16	I/O	General-purpose digital I/O
	P6.5	12	12	17	I/O	General-purpose digital I/O
	P6.6	13	13	18	I/O	General-purpose digital I/O
	P7.0	34	34	37	I/O	General-purpose digital I/O
	P7.1	35	35	38	I/O	General-purpose digital I/O
	P7.2	36	36	39	I/O	General-purpose digital I/O
	P7.3	37	37	40	I/O	General-purpose digital I/O
	P7.4	38	38	41	I/O	General-purpose digital I/O
	P9.4	45	45	48	I/O	General-purpose digital I/O
	P9.5	46	46	49	I/O	General-purpose digital I/O
	P9.6	47	47	50	I/O	General-purpose digital I/O
	P9.7	48	48	51	I/O	General-purpose digital I/O
	PJ.0	21	21	24	I/O	General-purpose digital I/O
	PJ.1	22	22	25	I/O	General-purpose digital I/O
	PJ.2	23	23	26	I/O	General-purpose digital I/O
	PJ.3	24	24	27	I/O	General-purpose digital I/O
	PJ.4	51	51	54	I/O	General-purpose digital I/O
PJ.5	52	52	55	I/O	General-purpose digital I/O	
PJ.6	55	55		I/O	General-purpose digital I/O	
PJ.7	54	54		I/O	General-purpose digital I/O	
I ² C	UCB0SCL	5	5	10	I/O	USCI_B0: I ² C clock (I ² C mode)
	UCB0SDA	4	4	9	I/O	USCI_B0: I ² C data (I ² C mode)
	UCB1SCL	16 61	16 61	21 4	I/O	USCI_B1: I ² C clock (I ² C mode)
	UCB1SDA	15 60	15 60	20 3	I/O	USCI_B1: I ² C data (I ² C mode)
Power	AVCC1	49	49	52	P	Analog power supply
	AVSS1	50	50	53	P	Analog ground supply
	AVSS2	53	53	56	P	Analog ground supply
	AVSS3	56			P	Analog ground supply
	DVCC1	18	18		P	Digital power supply
	DVCC2	40	40	43	P	Digital power supply
	DVCC3	63	63	6	P	Digital power supply
	DVSS1	17	17		P	Digital ground supply
	DVSS2	39	39	42	P	Digital ground supply
DVSS3	62	62	5	P	Digital ground supply	

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	FR597x(1), FR587x(1)	FR592x(1)		SIGNAL TYPE	DESCRIPTION
		PM, RGC	PM, RGC	DGG		
		PIN NO.	PIN NO.	PIN NO.		
SPI	UCA0CLK	3 31	3 31	8 34	I/O	USCI_A0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)
	UCA0SIMO	33 64	33 64	36	I/O	USCI_A0: Slave in, master out (SPI mode)
	UCA0SOMI	1 32	1 32	35	I/O	USCI_A0: Slave out, master in (SPI mode)
	UCA0STE	2 30	2 30	7 33	I/O	USCI_A0: Slave transmit enable (SPI mode)
	UCA1CLK	28	28 56	31	I/O	USCI_A1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)
	UCA1SIMO	26	26 54	29	I/O	USCI_A1: Slave in, master out (SPI mode)
	UCA1SOMI	27	27 55	30	I/O	USCI_A1: Slave out, master in (SPI mode)
	UCA1STE	29 57	29 57	32	I/O	USCI_A1: Slave transmit enable (SPI mode)
	UCB0CLK	2	2	7	I/O	USCI_B0: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)
	UCB0SIMO	4	4	9	I/O	USCI_B0: Slave in, master out (SPI mode)
	UCB0SOMI	5	5	10	I/O	USCI_B0: Slave out, master in (SPI mode)
	UCB0STE	3	3	8	I/O	USCI_B0: Slave transmit enable (SPI mode)
	UCB1CLK	14 59 64	14 59 64	19 2	I/O	USCI_B1: Clock signal input (SPI slave mode), Clock signal output (SPI master mode)
	UCB1SIMO	15 60	15 60	3 20	I/O	USCI_B1: Slave in, master out (SPI mode)
	UCB1SOMI	16 61	16 61	21 4	I/O	USCI_B1: Slave out, master in (SPI mode)
	UCB1STE	1 58	1 58	1	I/O	USCI_B1: Slave transmit enable (SPI mode)
System	NMI	20	20	23	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	20	20	23	I	Reset input active low

Table 4-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	FR597x(1), FR587x(1)	FR592x(1)		SIGNAL TYPE	DESCRIPTION
		PM, RGC	PM, RGC	DGG		
		PIN NO.	PIN NO.	PIN NO.		
Timer_A	TA0.0	3 35	3 35	8 38	I/O	Timer_A TA0 CCR0 capture: CCI0A input, compare: Out0 output
	TA0.1	4 36 44	4 36 44	9 39 47	I/O	Timer_A TA0 CCR1 capture: CCI1A input, compare: Out1 output
	TA0.2	5 37 43	5 37 43	10 40 46	I/O	Timer_A TA0 CCR2 capture: CCI2A input, compare: Out2 output
	TA0CLK	34 42	34 42	37 45	I	Timer_A TA0 clock signal TA0CLK input
	TA1.0	2 59	2 59	7 2	I/O	Timer_A TA1 CCR0 capture: CCI0A input, compare: Out0 output
	TA1.1	25 42 60	25 42 60	28 45 3	I/O	Timer_A TA1 CCR1 capture: CCI1A input, compare: Out1 output
	TA1.2	41 61	41 61	44 4	I/O	Timer_A TA1 CCR2 capture: CCI2A input, compare: Out2 output
	TA1CLK	43 58	43 58	46 1	I	Timer_A TA1 clock signal TA1CLK input
	TA3.2	14	14	19	I/O	Timer_A TA3 CCR2 capture: CCI2B input, compare: Out2 output
	TA3.3	15	15	20	I/O	Timer_A TA3 CCR3 capture: CCI3B input, compare: Out3 output
TA3.4	16	16	21	I/O	Timer_A TA3 CCR4 capture: CCI4B input, compare: Out4 output	
Timer_B	TB0.0	11 26	11 26	16 29	I/O	Timer_B TB0 CCR0 capture: CCI0B input, compare: Out0 output
	TB0.1	12 27	12 27	17 30	I/O	Timer_B TB0 CCR1 capture: CCI1A input, compare: Out1 output
	TB0.2	13 28	13 28	18 31	I/O	Timer_B TB0 CCR2 capture: CCI2A input, compare: Out2 output
	TB0.3	29	29	32	I/O	Timer_B TB0 CCR3 capture: CCI3B input, compare: Out3 output
	TB0.4	31	31	34	I/O	Timer_B TB0 CCR4 capture: CCI4B input, compare: Out4 output
	TB0.5	32	32	35	I/O	Timer_B TB0 CCR5 capture: CCI5B input, compare: Out5 output
	TB0.6	33	33	36	I/O	Timer_B TB0 CCR6 capture: CCI6B input, compare: Out6 output
	TB0CLK	25 33 57	25 33 57	28 36	I	Timer_B TB0 clock signal TB0CLK input
TB0OUTH	21 30	21 30	24 33	I	Switch all PWM outputs high impedance input - Timer_B TB0	
UART	UCA0RXD	1 32	1 32	35	I	USCI_A0: Receive data (UART mode)
	UCA0TXD	33 64	33 64	36	O	USCI_A0: Transmit data (UART mode)
	UCA1RXD	27	27	30	I	USCI_A1: Receive data (UART mode)
	UCA1TXD	26	26	29	O	USCI_A1: Transmit data (UART mode)

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [Section 6.11.22](#).

Table 4-3. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (μ A)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
LVC MOS	3.0 V	Y ⁽¹⁾	Programmable	See Table 5-11	See Section 5.12.5.1	
Analog	3.0 V	N	N/A	N/A	N/A	See analog modules in Section 5 for details
Power (DVCC)	3.0 V	N	N/A	N/A	N/A	SVS enables hysteresis on DVCC
Power (AVCC)	3.0 V	N	N/A	N/A	N/A	

(1) Only for Input pins.

4.5 Connection of Unused Pins

[Table 4-4](#) lists the correct termination of all unused pins.

Table 4-4. Connection of Unused Pins⁽¹⁾

PIN	POTENTIAL	COMMENT
AVCC	DV _{CC}	
AVSS	DV _{SS}	
Px.0 to Px.7	Open	Switched to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}$ /NMI	DV _{CC} or V _{CC}	47-k Ω pullup or internal pullup selected with 10-nF (2.2 nF ⁽²⁾) pulldown
PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK	Open	The JTAG pins are shared with general-purpose I/O function (PJ.x). If these pins are not used, they should be set to port function and output direction. When used as JTAG pins, these pins should remain open.
TEST	Open	This pin always has an internal pulldown enabled.

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
- (2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V _{SS}	-0.3	4.1	V
Voltage difference between DVCC and AVCC pins ⁽²⁾		±0.3	V
Voltage applied to any pin ⁽³⁾	-0.3	V _{CC} + 0.3 (4.1 Maximum)	V
Diode current at any device pin		±2	mA
Storage temperature, T _{stg} ⁽⁴⁾	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (3) All voltages referenced to V_{SS}.
- (4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage applied at all DVCC and AVCC pins ^{(1) (2) (3)}	1.8 ⁽⁴⁾		3.6	V
V _{SS}	Supply voltage applied at all DVSS and AVSS pins		0		V
T _A	Operating free-air temperature	-40		85	°C
T _J	Operating junction temperature	-40		85	°C
C _{DVCC}	Recommended capacitor value at DVCC ⁽⁵⁾		1		µF
f _{SYSTEM}	Processor frequency (maximum MCLK frequency) ⁽⁶⁾	No FRAM wait states (NWAITSx = 0)	0	8 ⁽⁷⁾	MHz
		With FRAM wait states (NWAITSx = 1) ⁽⁸⁾	0	16 ⁽⁹⁾	
f _{ACLK}	Maximum ACLK frequency			50	kHz
f _{SMCLK}	Maximum SMCLK frequency			16 ⁽⁹⁾	MHz

- (1) TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in *Absolute Maximum Ratings*. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.
- (2) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/µs). Following the data sheet recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
- (3) Modules may have a different supply voltage range specification. Refer to the specification of the respective module in this data sheet.
- (4) The minimum supply voltage is defined by the supervisor SVS levels. Refer to the PMM SVS threshold parameters in [Table 5-2](#) for the exact values.
- (5) As decoupling capacitor for each supply pin pair (DVCC/DVSS, AVCC/AVSS, ...), a low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pairs.
- (6) Modules may have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.
- (7) DCO settings and HF crystals with a typical value less or equal the specified MAX value are permitted.
- (8) Wait states only occur on actual FRAM accesses; that is, on FRAM cache misses. RAM and peripheral accesses are always executed without wait states.
- (9) DCO settings and HF crystals with a typical value less or equal the specified MAX value are permitted. If a clock source with a higher typical value is used, the clock must be divided in the clock system.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾

PARAMETER	EXECUTION MEMORY	V_{CC}	FREQUENCY ($f_{MCLK} = f_{SMCLK}$)										UNIT			
			1 MHz 0 WAIT STATES (NWAITS _x = 0)		4 MHz 0 WAIT STATES (NWAITS _x = 0)		8 MHz 0 WAIT STATES (NWAITS _x = 0)		12 MHz 1 WAIT STATES (NWAITS _x = 1)		16 MHz 1 WAIT STATES (NWAITS _x = 1)					
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX				
$I_{AM, FRAM_UNI}$ (Unified memory) ⁽³⁾	FRAM	3.0 V	210		640			1220			1475			1845		μA
$I_{AM, FRAM(0\%)}$ ⁽⁴⁾ ⁽⁵⁾	FRAM 0% cache hit ratio	3.0 V	370		1280			2510			2080			2650		μA
$I_{AM, FRAM(50\%)}$ ⁽⁴⁾ ⁽⁵⁾	FRAM 50% cache hit ratio	3.0 V	240		745			1440			1575			1990		μA
$I_{AM, FRAM(66\%)}$ ⁽⁴⁾ ⁽⁵⁾	FRAM 66% cache hit ratio	3.0 V	200		560			1070			1300			1620		μA
$I_{AM, FRAM(75\%)}$ ⁽⁴⁾ ⁽⁵⁾	FRAM 75% cache hit ratio	3.0 V	170	255	480		890	1085	1155	1310	1420	1620				μA
$I_{AM, FRAM(100\%)}$ ⁽⁴⁾ ⁽⁵⁾	FRAM 100% cache hit ratio	3.0 V	110		235			420			640			730		μA
$I_{AM, RAM}$ ⁽⁶⁾ ⁽⁵⁾	RAM	3.0 V	130		320			585			890			1070		μA
$I_{AM, RAM\ only}$ ⁽⁷⁾ ⁽⁵⁾	RAM	3.0 V	100	180	290			555			860			1040	1300	μA

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Characterized with program executing typical data processing.

$f_{ACLK} = 32768$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, $f_{DCO} = 24$ MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO}/2$.

At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.

The following equation can be used to compute $f_{MCLK,eff}$:

$$f_{MCLK,eff} = f_{MCLK} / [\text{wait states} \times (1 - \text{cache hit ratio}) + 1]$$

For example, with 1 wait state and 75% cache hit ratio $f_{MCLK,eff} = f_{MCLK} / [1 \times (1 - 0.75) + 1] = f_{MCLK} / 1.25$.

(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.

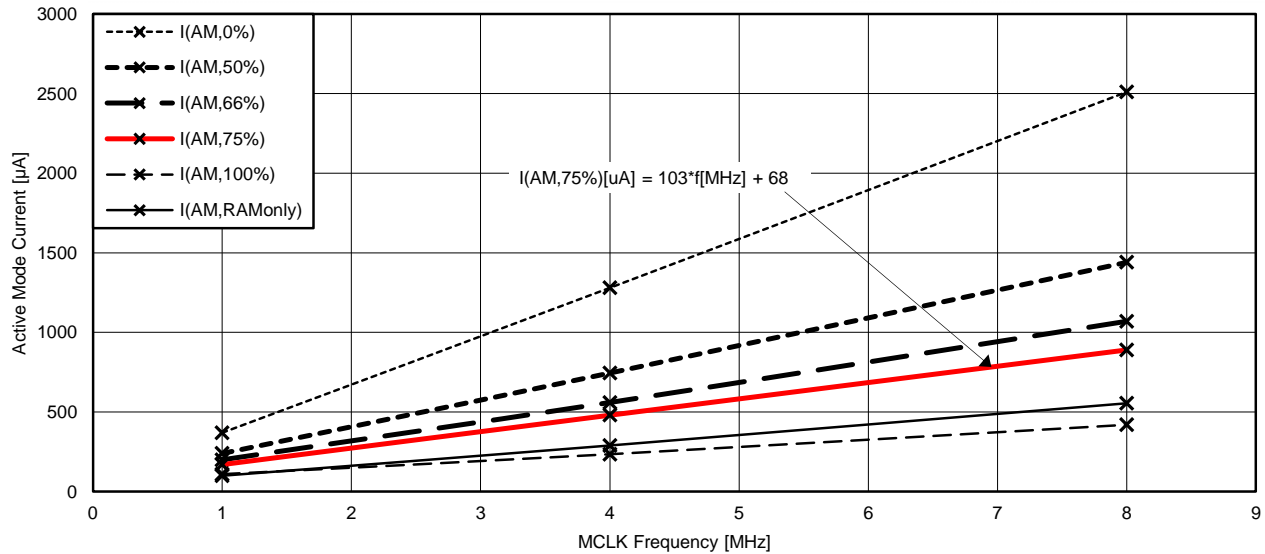
(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

(5) See [Figure 5-1](#) for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in [Section 5.4](#).

(6) Program and data reside entirely in RAM. All execution is from RAM.

(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

5.5 Typical Characteristics - Active Mode Supply Currents



I(AM, cache hit ratio): Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

I(AM, RAMonly): Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

Figure 5-1. Typical Active Mode Supply Currents, No Wait States

5.6 Low-Power Mode (LPM0, LPM1) Supply Currents Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾

PARAMETER	V _{CC}	FREQUENCY (f _{SMCLK})										UNIT
		1 MHz		4 MHz		8 MHz		12 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{LPM0}	2.2 V	75		105		165		250		230		µA
	3.0 V	80	120	115		175		260		240	275	
I _{LPM1}	2.2 V	40		65		130		215		195		µA
	3.0 V	40	65	65		130		215		195	220	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} at specified frequency - except for 12 MHz: here f_{DCO} = 24 MHz and f_{SMCLK} = f_{DCO}/2.

5.7 Low-Power Mode LPM2, LPM3, LPM4 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER	V_{CC}	-40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM2,XT12}$ Low-power mode 2, 12-pF crystal ^{(2) (3) (4)}	2.2 V	0.8		1.2		3.1		8.8		μA
	3.0 V	0.8		1.2	2.2	3.1		8.8	17	
$I_{LPM2,XT3.7}$ Low-power mode 2, 3.7-pF crystal ^{(2) (5) (4)}	2.2 V	0.7		1.1		3.0		8.7		μA
	3.0 V	0.7		1.1		3.0		8.7		
$I_{LPM2,VLO}$ Low-power mode 2, VLO, includes SVS ⁽⁶⁾	2.2 V	0.5		0.9		2.8		8.5		μA
	3.0 V	0.5		0.9	2.0	2.8		8.5	16.7	
$I_{LPM3,XT12}$ Low-power mode 3, 12-pF crystal, includes SVS ^{(2) (3) (7)}	2.2 V	0.7		0.9		1.2		2.5		μA
	3.0 V	0.7		0.9	1.2	1.2		2.5	6.4	
$I_{LPM3,XT3.7}$ Low-power mode 3, 3.7-pF crystal, excludes SVS ^{(2) (5) (8)} (refer also to Figure 5-2)	2.2 V	0.6		0.7		1.1		2.4		μA
	3.0 V	0.6		0.7		1.1		2.4		
$I_{LPM3,VLO}$ Low-power mode 3, VLO, excludes SVS ⁽⁹⁾	2.2 V	0.35		0.4		0.9		1.8		μA
	3.0 V	0.35		0.4	0.8	0.9		1.8	6.1	
$I_{LPM3,VLO, RAMoff}$ Low-power mode 3, VLO, excludes SVS, RAM powered down completely ⁽¹⁰⁾	2.2 V	0.35		0.4		0.8		1.7		μA
	3.0 V	0.35		0.4	0.7	0.8		1.7	5.2	

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) Not applicable for devices with HF crystal oscillator only.
- (3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
- (4) **Low-power mode 2, crystal oscillator** test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
- (6) **Low-power mode 2, VLO** test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout and SVS included.
CPUOFF = 1, SCG0 = 0 SCG1 = 1, OSCOFF = 0 (LPM2),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (7) **Low-power mode 3, 12-pF crystal, includes SVS** test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
- (8) **Low-power mode 3, 3.7-pF crystal, excludes SVS** test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
- (9) **Low-power mode 3, VLO, excludes SVS** test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.
- (10) **Low-power mode 3, VLO, excludes SVS, RAM powered down completely** test conditions:
Current for watchdog timer clocked by ACLK included. RTC disabled (RTCHOLD = 1). Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

Low-Power Mode LPM2, LPM3, LPM4 Supply Currents (Into V_{CC}) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

PARAMETER	V_{CC}	-40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM4,SVS}$ Low-power mode 4, includes SVS ⁽¹¹⁾	2.2 V	0.45		0.55		0.9		1.8		μA
	3.0 V	0.45		0.55	0.8	0.9		1.8	6.2	
I_{LPM4} Low-power mode 4, excludes SVS ⁽¹²⁾	2.2 V	0.25		0.4		0.7		1.6		μA
	3.0 V	0.25		0.4	0.65	0.7		1.6	4.6	
$I_{LPM4,RAMoff}$ Low-power mode 4, excludes SVS, RAM powered down completely ⁽¹³⁾	2.2 V	0.25		0.4		0.7		1.4		μA
	3.0 V	0.25		0.4	0.65	0.7		1.4	4.6	
$I_{IDLE,GroupA}$ Additional idle current if one or more modules from Group A (refer to) are activated in LPM3 or LPM4	3.0V			0.02				0.4	1.0	μA
$I_{IDLE,GroupB}$ Additional idle current if one or more modules from Group B (refer to) are activated in LPM3 or LPM4	3.0V			0.02				0.4	1.0	μA
$I_{IDLE,GroupC}$ Additional idle current if one or more modules from Group C (refer to) are activated in LPM3 or LPM4	3.0V			0.02				0.3	0.8	μA

(11) **Low-power mode 4, includes SVS** test conditions:

Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

(12) **Low-power mode 4, excludes SVS** test conditions:

Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

(13) **Low-power mode 4, excludes SVS, RAM powered down completely** test conditions:

Current for brownout included. SVS disabled (SVSHE = 0). RAM disabled (RCCTL0 = 5A55h).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

Activating additional peripherals increases the current consumption due to active supply current contribution as well as due to additional idle current. Refer to the idle currents specified for the respective peripheral groups.

5.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	V_{CC}	–40°C		25°C		60°C		85°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5,XT12}$ Low-power mode 3.5, 12-pF crystal including SVS ^{(2) (3) (4)}	2.2 V	0.45		0.5		0.6		0.75		μA
	3.0 V	0.45		0.5	0.75	0.6		0.75	1.4	
$I_{LPM3.5,XT3.7}$ Low-power mode 3.5, 3.7-pF crystal excluding SVS ^{(2) (5) (6)}	2.2 V	0.3		0.35		0.4		0.65		μA
	3.0 V	0.3		0.35		0.4		0.65		
$I_{LPM4.5,SVS}$ Low-power mode 4.5, including SVS ⁽⁷⁾	2.2 V	0.2		0.3		0.35		0.4		μA
	3.0 V	0.2		0.3	0.5	0.35		0.4	0.7	
$I_{LPM4.5}$ Low-power mode 4.5, excluding SVS ⁽⁸⁾	2.2 V	0.03		0.04		0.06		0.14		μA
	3.0 V	0.03		0.04		0.06		0.14	0.5	

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) Not applicable for devices with HF crystal oscillator only.
- (3) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF load.
- (4) **Low-power mode 3.5, 1-pF crystal including SVS** test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (5) Characterized with a Seiko SSP-T7-FL (SMD) crystal with a load capacitance of 3.7 pF. The internal and external load capacitance are chosen to closely match the required 3.7-pF load.
- (6) **Low-power mode 3.5, 3.7-pF crystal excluding SVS** test conditions:
Current for RTC clocked by XT1 included. Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (7) **Low-power mode 4.5 including SVS** test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz
- (8) **Low-power mode 4.5 excluding SVS** test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
 $f_{XT1} = 0$ Hz, $f_{ACLK} = 0$ Hz, $f_{MCLK} = f_{SMCLK} = 0$ MHz

5.9 Typical Characteristics, Low-Power Mode Supply Currents

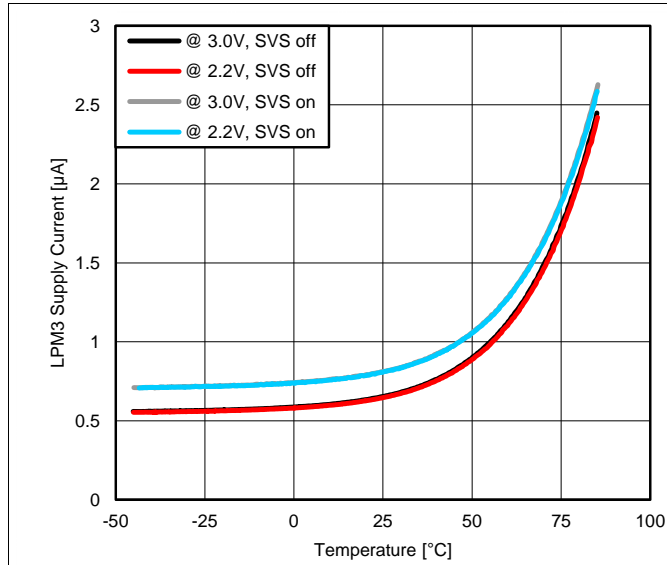


Figure 5-2. LPM3 Supply Current vs Temperature (LPM3,XT3.7)

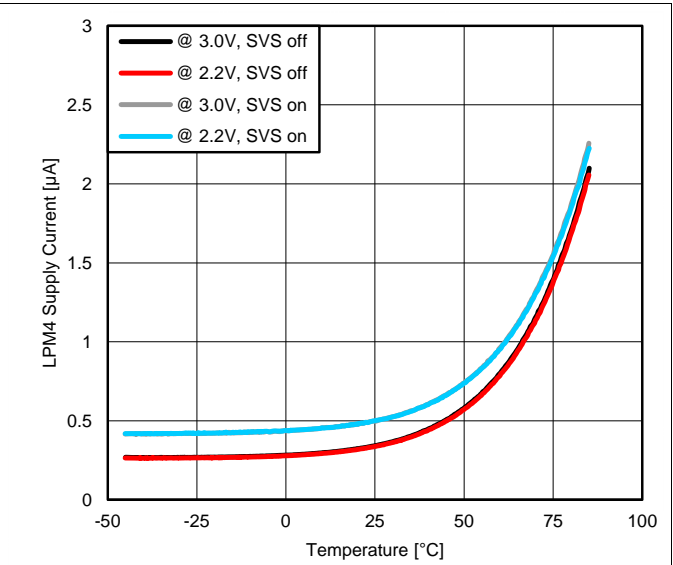


Figure 5-3. LPM4 Supply Current vs Temperature (LPM4,SVS)

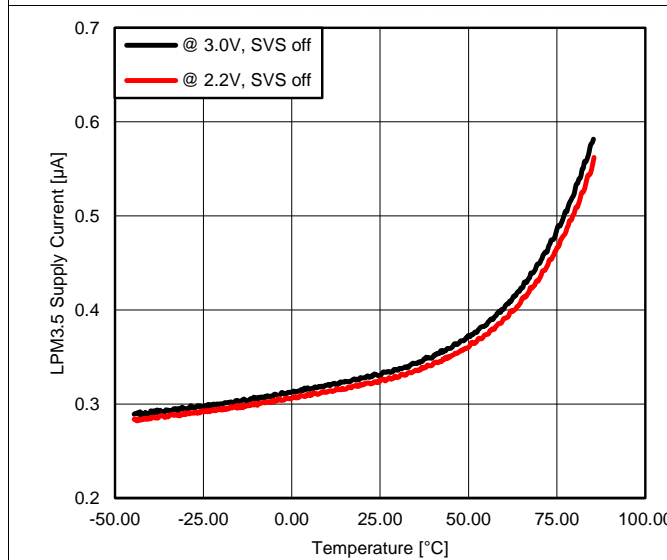


Figure 5-4. LPM3.5 Supply Current vs Temperature (LPM3.5,XT3.7)

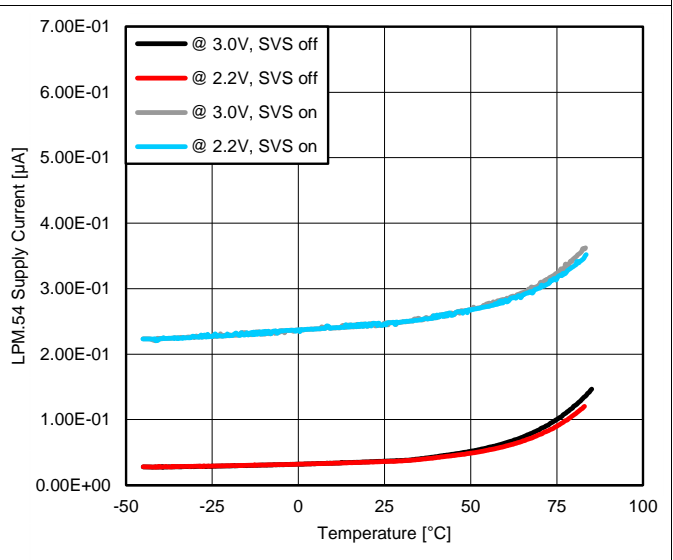


Figure 5-5. LPM4.5 Supply Current vs Temperature (LPM4.5)

5.10 Typical Characteristics, Current Consumption per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	MIN	TYP	MAX	UNIT
Timer_A		Module input clock		3		μA/MHz
Timer_B		Module input clock		5		μA/MHz
eUSCI_A	UART mode	Module input clock		5.5		μA/MHz
eUSCI_A	SPI mode	Module input clock		3.5		μA/MHz
eUSCI_B	SPI mode	Module input clock		3.5		μA/MHz
eUSCI_B	I ² C mode, 100 kbaud	Module input clock		3.5		μA/MHz
RTC_C		32 kHz		100		nA
MPY	Only from start to end of operation	MCLK		25		μA/MHz
AES	Only from start to end of operation	MCLK		21		μA/MHz
CRC16	Only from start to end of operation	MCLK		2.5		μA/MHz
CRC32	Only from start to end of operation	MCLK		2.5		μA/MHz

5.11 Thermal Characteristics⁽¹⁾

PARAMETER	PACKAGE	VALUE ⁽¹⁾	UNIT
θ_{JA} Junction-to-ambient thermal resistance, still air ⁽²⁾	TSSOP-56 (DGG)	57.7	°C/W
$\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance ⁽³⁾		15.1	°C/W
θ_{JB} Junction-to-board thermal resistance ⁽⁴⁾		26.5	°C/W
Ψ_{JB} Junction-to-board thermal characterization parameter		26.2	°C/W
Ψ_{JT} Junction-to-top thermal characterization parameter		0.5	°C/W
$\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance ⁽⁵⁾		N/A	°C/W
θ_{JA} Junction-to-ambient thermal resistance, still air ⁽²⁾	QFP-64 (PN)	59.3	°C/W
$\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance ⁽³⁾		19.5	°C/W
θ_{JB} Junction-to-board thermal resistance ⁽⁴⁾		30.8	°C/W
Ψ_{JB} Junction-to-board thermal characterization parameter		30.5	°C/W
Ψ_{JT} Junction-to-top thermal characterization parameter		1.0	°C/W
$\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance ⁽⁵⁾		N/A	°C/W
θ_{JA} Junction-to-ambient thermal resistance, still air ⁽²⁾	QFN-64 (RGC)	29.6	°C/W
$\theta_{JC(TOP)}$ Junction-to-case (top) thermal resistance ⁽³⁾		15.8	°C/W
θ_{JB} Junction-to-board thermal resistance ⁽⁴⁾		8.5	°C/W
Ψ_{JB} Junction-to-board thermal characterization parameter		8.5	°C/W
Ψ_{JT} Junction-to-top thermal characterization parameter		0.2	°C/W
$\theta_{JC(BOTTOM)}$ Junction-to-case (bottom) thermal resistance ⁽⁵⁾		1.2	°C/W

(1) N/A = not applicable

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.12 Timing and Switching Characteristics

5.12.1 Power Supply Sequencing

It is recommended to power AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

Table 5-1. Brownout and Device Reset Power Ramp Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{VCC_BOR-}	Brownout power-down level ⁽¹⁾	dV _{VCC} /d _t < 3 V/s ⁽²⁾	0.73	1.66	V
V _{VCC_BOR+}	Brownout power-up level ⁽¹⁾	dV _{VCC} /d _t < 3 V/s ⁽²⁾	0.79	1.68	V

- (1) Fast supply voltage changes can trigger a BOR reset even within the recommended supply voltage range. To avoid unwanted BOR resets, the supply voltage must change by less than 0.05 V per microsecond (±0.05 V/μs). Following the data sheet recommendation for capacitor C_{DVCC} should limit the slopes accordingly.
- (2) The brownout levels are measured with a slowly changing supply.

Table 5-2. SVS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{SVSH,LPM}	SVS _H current consumption, low power modes			170	300	nA
V _{SVSH-}	SVS _H power-down level		1.75	1.80	1.85	V
V _{SVSH+}	SVS _H power-up level		1.77	1.88	1.99	V
V _{SVSH_hys}	SVS _H hysteresis		40		120	mV
t _{PD,SVSH, AM}	SVS _H propagation delay, active mode	dV _{VCC} /dt = -10 mV/μs			10	μs

5.12.2 Reset Timing

Table 5-3. Reset Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC}	MIN	MAX	UNIT
t _(RST)	External reset pulse duration on $\overline{\text{RST}}$ ⁽¹⁾	2.2 V, 3.0 V	2		μs

- (1) Not applicable if the $\overline{\text{RST}}$ /NMI pin is configured as NMI.

5.12.3 Clock Specifications

Table 5-4. Low-Frequency Crystal Oscillator, LFXT⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
I _{VCC,LFXT}	Current consumption	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T _A = 25°C, C _{L,eff} = 3.7 pF, ESR ≈ 44 kΩ	3.0 V	180		nA	
		f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {1}, T _A = 25°C, C _{L,eff} = 6 pF, ESR ≈ 40 kΩ	3.0 V	185			
		f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {2}, T _A = 25°C, C _{L,eff} = 9 pF, ESR ≈ 40 kΩ	3.0 V	225			
		f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF, ESR ≈ 40 kΩ	3.0 V	330			
f _{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0		32768		Hz	
DC _{LFXT}	LFXT oscillator duty cycle	Measured at ACLK, f _{LFXT} = 32768 Hz		30%	70%		
f _{LFXT,SW}	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 ⁽²⁾ ⁽³⁾		10.5	32.768	50	kHz
DC _{LFXT, SW}	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%	70%		
OA _{LFXT}	Oscillation allowance for LF crystals ⁽⁴⁾	LFXTBYPASS = 0, LFXTDRIVE = {1}, f _{LFXT} = 32768 Hz, C _{L,eff} = 6 pF		210		kΩ	
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f _{LFXT} = 32768 Hz, C _{L,eff} = 12.5 pF		300			
C _{LFXIN}	Integrated load capacitance at LFXIN terminal ⁽⁵⁾ ⁽⁶⁾			2		pF	
C _{LFXOUT}	Integrated load capacitance at LFXOUT terminal ⁽⁵⁾ ⁽⁶⁾			2		pF	

- (1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins LFXIN and LFXOUT.
 - Avoid running PCB traces underneath or adjacent to the LFXIN and LFXOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator LFXIN and LFXOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by DC_{LFXT, SW}.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For LFXTDRIVE = {0}, C_{L,eff} = 3.7 pF
 - For LFXTDRIVE = {1}, C_{L,eff} = 6 pF
 - For LFXTDRIVE = {2}, 6 pF ≤ C_{L,eff} ≤ 9pF
 - For LFXTDRIVE = {3}, 9 pF ≤ C_{L,eff} ≤ 12.5 pF
- (5) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C_{L,eff} can be computed as C_{IN} × C_{OUT} / (C_{IN} + C_{OUT}), where C_{IN} and C_{OUT} is the total capacitance at the LFXIN and LFXOUT terminals, respectively.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 3.7 pF, 6 pF, 9pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. It is recommended to verify that the recommended effective load capacitance of the selected crystal is met.

Low-Frequency Crystal Oscillator, LFXT⁽¹⁾ (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{START,LFXT} Start-up time ⁽⁷⁾	f _{OSC} = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {0}, T _A = 25°C, C _{L,eff} = 3.7 pF	3.0 V		800		ms
	f _{OSC} = 32768 Hz LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF	3.0 V		1000		
f _{FAULT,LFXT} Oscillator fault frequency ^{(8) (9)}			0		3500	Hz

(7) Includes start-up counter of 1024 clock cycles.

(8) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition will set the flag.

(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-5. High-Frequency Crystal Oscillator, HFXT⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
I _{DVCC,HFXT} HFXT oscillator crystal current HF mode at typical ESR	f _{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1 ⁽²⁾ , T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}	3.0 V		75		μA	
	f _{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1 T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}			120			
	f _{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 2, HFFREQ = 2, T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}				190		
	f _{OSC} = 24 MHz HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T _A = 25°C, C _{L,eff} = 18 pF, typical ESR, C _{shunt}						250
f _{HFXT} HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 1 ^{(2) (3)}		4		8	MHz	
	HFXTBYPASS = 0, HFFREQ = 2 ⁽³⁾		8.01		16		
	HFXTBYPASS = 0, HFFREQ = 3 ⁽³⁾		16.01		24		
DC _{HFXT} HFXT oscillator duty cycle.	Measured at SMCLK, f _{HFXT} = 16 MHz		40%	50%	60%		

(1) To improve EMI on the HFXT oscillator the following guidelines should be observed.

- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins HFXIN and HFXOUT.
- Avoid running PCB traces underneath or adjacent to the HFXIN and HFXOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator HFXIN and HFXOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) HFFREQ = {0} is not supported for HFXT crystal mode of operation.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

High-Frequency Crystal Oscillator, HFXT⁽¹⁾ (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{HFXT,SW}	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1, HFFREQ = 0 ⁽⁴⁾ (3)		0.9		4	MHz
		HFXTBYPASS = 1, HFFREQ = 1 ⁽⁴⁾ (3)		4.01		8	
		HFXTBYPASS = 1, HFFREQ = 2 ⁽⁴⁾ (3)		8.01		16	
		HFXTBYPASS = 1, HFFREQ = 3 ⁽⁴⁾ (3)		16.01		24	
DC _{HFXT,SW}	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1		40%		60%	
t _{START,HFXT}	Start-up time ⁽⁵⁾	f _{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 1, T _A = 25°C, C _{L,eff} = 16 pF	3.0 V		1.6		ms
		f _{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 3, HFFREQ = 3, T _A = 25°C, C _{L,eff} = 16 pF	3.0 V		0.6		
C _{HFXTIN}	Integrated load capacitance at HFXIN terminal ⁽⁶⁾ ⁽⁷⁾				2		pF
C _{HFXTOUT}	Integrated load capacitance at HFXOUT terminal ⁽⁶⁾ ⁽⁷⁾				2		pF
f _{Fault,HFXT}	Oscillator fault frequency ⁽⁸⁾ ⁽⁹⁾			0		800	kHz

(4) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by DC_{HFXT, SW}.

(5) Includes start-up counter of 1024 clock cycles.

(6) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, C_{L,eff} can be computed as C_{IN} x C_{OUT} / (C_{IN} + C_{OUT}), where C_{IN} and C_{OUT} is the total capacitance at the HFXIN and HFXOUT terminals, respectively.

(7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. It is recommended to verify that the recommended effective load capacitance of the selected crystal is met.

(8) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX might set the flag. A static condition or stuck at fault condition will set the flag.

(9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-6. DCO

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{DCO1}	DCO frequency range 1 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 0 DCORSEL = 1, DCOFSEL = 0			1	±3.5%	MHz
f _{DCO2.7}	DCO frequency range 2.7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 1			2.667	±3.5%	MHz
f _{DCO3.5}	DCO frequency range 3.5 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 2			3.5	±3.5%	MHz
f _{DCO4}	DCO frequency range 4 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 3			4	±3.5%	MHz
f _{DCO5.3}	DCO frequency range 5.3 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 4 DCORSEL = 1, DCOFSEL = 1			5.333	±3.5%	MHz
f _{DCO7}	DCO frequency range 7 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 5 DCORSEL = 1, DCOFSEL = 2			7	±3.5%	MHz
f _{DCO8}	DCO frequency range 8 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 0, DCOFSEL = 6 DCORSEL = 1, DCOFSEL = 3			8	±3.5%	MHz
f _{DCO16}	DCO frequency range 16 MHz, trimmed	Measured at SMCLK, divide by 1, DCORSEL = 1, DCOFSEL = 4			16	±3.5% ⁽¹⁾	MHz
f _{DCO21}	DCO frequency range 21 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 5			21	±3.5% ⁽¹⁾	MHz
f _{DCO24}	DCO frequency range 24 MHz, trimmed	Measured at SMCLK, divide by 2, DCORSEL = 1, DCOFSEL = 6			24	±3.5% ⁽¹⁾	MHz
f _{DCO,DC}	Duty cycle	Measured at SMCLK, divide by 1, No external divide, all DCORSEL and DCOFSEL settings except DCORSEL = 1, DCOFSEL = 5 and DCORSEL = 1, DCOFSEL = 6		48%	50%	52%	
t _{DCO, JITTER}	DCO jitter	Based on f _{signal} = 10 kHz and DCO used for 12-bit SAR ADC sampling source. This achieves > 74-dB SNR due to jitter; that is, it is limited by ADC performance.			2	3	ns
df _{DCO} /dT	DCO temperature drift ⁽²⁾		3.0 V		0.01		%/°C

- (1) After a wakeup from LPM1, LPM2, LPM3 or LPM4 the DCO frequency f_{DCO} might exceed the specified frequency range for a few clock cycles by up to 5% before settling into the specified steady state frequency range.
(2) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))

Table 5-7. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{VLO}	Current consumption				100		nA
f _{VLO}	VLO frequency	Measured at ACLK		6	9.4	14	kHz
df _{VLO} /dT	VLO frequency temperature drift	Measured at ACLK ⁽¹⁾			0.2		%/°C
df _{VLO} /dV _{CC}	VLO frequency supply voltage drift	Measured at ACLK ⁽²⁾			0.7		%/V
f _{VLO,DC}	Duty cycle	Measured at ACLK		40%	50%	60%	

- (1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-8. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption	Enabled		25		μA
f_{MODOSC}	MODOSC frequency		4.0	4.8	5.4	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift ⁽¹⁾			0.08		$\%/^{\circ}\text{C}$
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift ⁽²⁾			1.4		$\%/V$
DC_{MODOSC}	Duty cycle	Measured at SMCLK, divide by 1	40%	50%	60%	

 (1) Calculated using the box method: $(\text{MAX}(-40^{\circ}\text{C to } 85^{\circ}\text{C}) - \text{MIN}(-40^{\circ}\text{C to } 85^{\circ}\text{C})) / \text{MIN}(-40^{\circ}\text{C to } 85^{\circ}\text{C}) / (85^{\circ}\text{C} - (-40^{\circ}\text{C}))$

 (2) Calculated using the box method: $(\text{MAX}(1.8\text{ V to } 3.6\text{ V}) - \text{MIN}(1.8\text{ V to } 3.6\text{ V})) / \text{MIN}(1.8\text{ V to } 3.6\text{ V}) / (3.6\text{ V} - 1.8\text{ V})$

5.12.4 Wake-up Characteristics

Table 5-9. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{WAKE-UP FRAM}	Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from an LPM if immediate activation is selected				6	10	µs
t _{WAKE-UP LPM0}	Wake-up time from LPM0 to active mode	MCLKREQEN = 1 ⁽¹⁾	2.2 V, 3.0 V			400 ns + 1.5/t _{DCO}	
		MCLKREQEN = 0 ⁽¹⁾⁽²⁾	2.2 V, 3.0 V			400 ns + 2.5/t _{DCO}	
t _{WAKE-UP LPM1}	Wake-up time from LPM1 to active mode ⁽¹⁾		2.2 V, 3.0 V		6		µs
t _{WAKE-UP LPM2}	Wake-up time from LPM2 to active mode ⁽¹⁾		2.2 V, 3.0 V		6		µs
t _{WAKE-UP LPM3}	Wake-up time from LPM3 to active mode ⁽¹⁾		2.2 V, 3.0 V		7	10	µs
t _{WAKE-UP LPM4}	Wake-up time from LPM4 to active mode ⁽¹⁾		2.2 V, 3.0 V		7	10	µs
t _{WAKE-UP LPM3.5}	Wake-up time from LPM3.5 to active mode ⁽³⁾		2.2 V, 3.0 V		250	350	µs
t _{WAKE-UP LPM4.5}	Wake-up time from LPM4.5 to active mode ⁽³⁾	SVSHE = 1	2.2 V, 3.0 V		250	350	µs
		SVSHE = 0	2.2 V, 3.0 V		0.4	0.8	ms
t _{WAKE-UP-RST}	Wake-up time from a $\overline{\text{RST}}$ pin triggered reset to active mode ⁽³⁾		2.2 V, 3.0 V		250	350	µs
t _{WAKE-UP-BOR}	Wake-up time from power-up to active mode ⁽³⁾		2.2 V, 3.0 V		0.5	1.0	ms

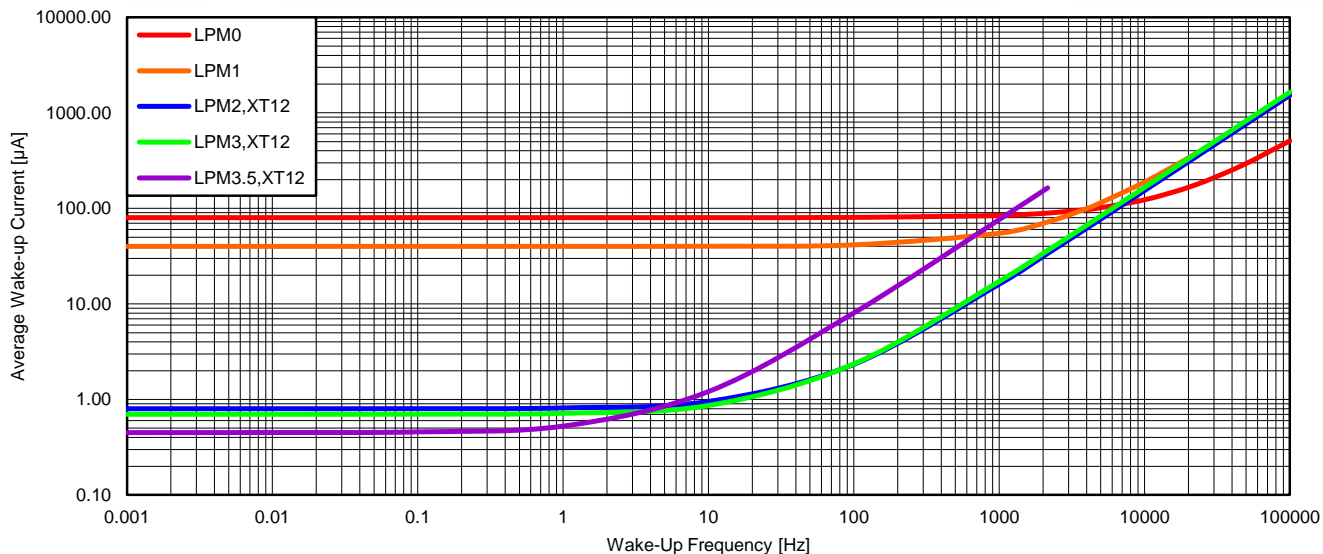
- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge with MCLKREQEN = 1. This time includes the activation of the FRAM during wakeup.
- (2) With MCLKREQEN = 0, the MCLK is gated one additional one clock cycle (wake up from LPM0, LPM1, LPM2, LPM3, and LPM4). The device wake-up time is not affected by the status of the MCLKREQEN bit.
- (3) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

Table 5-10. Typical Wake-up Charge⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q _{WAKE-UP FRAM}	Charge used for activating the FRAM in AM or during wakeup from LPM0 if previously disabled by the FRAM controller.			15.1		nAs
Q _{WAKE-UP LPM0}	Charge used to wake up from LPM0 to active mode (with FRAM active)			4.4		nAs
Q _{WAKE-UP LPM1}	Charge used to wake up from LPM1 to active mode (with FRAM active)			15.1		nAs
Q _{WAKE-UP LPM2}	Charge used to wake up from LPM2 to active mode (with FRAM active)			15.3		nAs
Q _{WAKE-UP LPM3}	Charge used to wake up from LPM3 to active mode (with FRAM active)			16.5		nAs
Q _{WAKE-UP LPM4}	Charge used to wake up from LPM4 to active mode (with FRAM active)			16.5		nAs
Q _{WAKE-UP LPM3.5}	Charge used to wake up from LPM3.5 to active mode ⁽²⁾			76		nAs
Q _{WAKE-UP LPM4.5}	Charge used to wake up from LPM4.5 to active mode ⁽²⁾	SVSHE = 1		77		nAs
		SVSHE = 0		77.5		nAs
Q _{WAKE-UP-RESET}	Charge used for reset from $\overline{\text{RST}}$ or BOR event to active mode ⁽²⁾			75		nAs

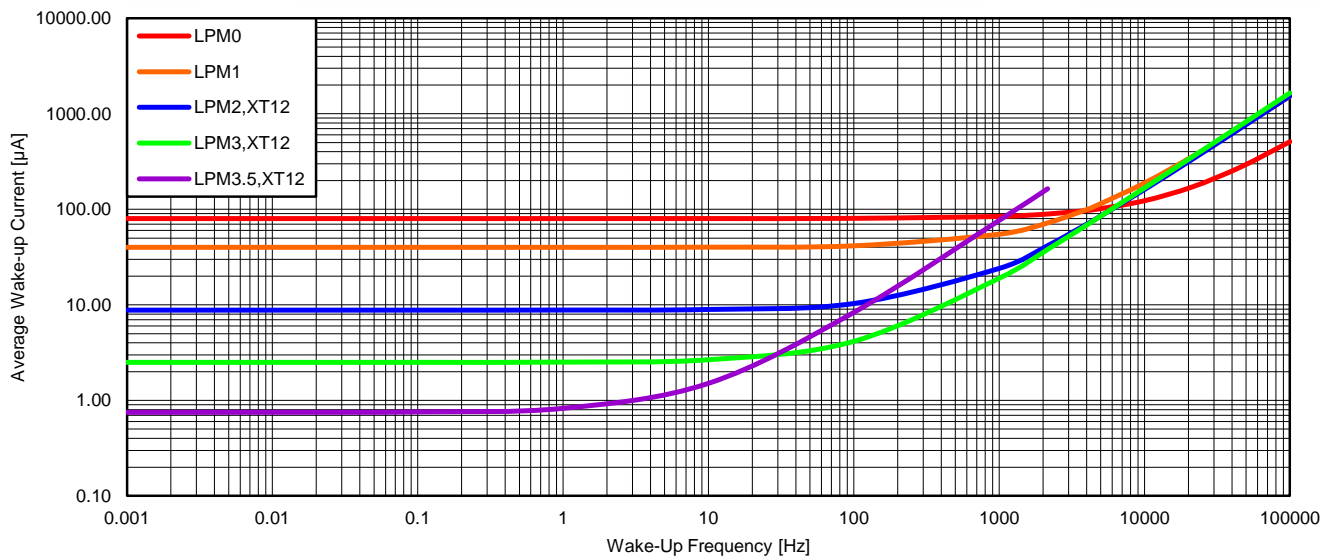
- (1) Charge used during the wake-up time from a given low-power mode to active mode. This does **not** include the energy required in active mode (for example, for an interrupt service routine).
- (2) Charge required until start of user code. This does **not** include the energy required to reconfigure the device.

5.12.4.1 Typical Characteristics, Average LPM Currents vs Wake-up Frequency



NOTE: The average wake-up current does **not** include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-6. Average LPM Currents vs Wake-up Frequency at 25°C



NOTE: The average wake-up current does **not** include the energy required in active mode; for example, for an interrupt service routine or to reconfigure the device.

Figure 5-7. Average LPM Currents vs Wake-up Frequency at 85°C

5.12.5 Digital I/Os

Table 5-11. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage		2.2 V	1.2		1.65	V
			3.0 V	1.65		2.25	
V _{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.00	V
			3.0 V	0.75		1.35	
V _{hys}	Input voltage hysteresis (V _{IT+} – V _{IT-})		2.2 V	0.44		0.98	V
			3.0 V	0.60		1.30	
R _{Pull}	Pullup or pulldown resistor	For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _{I,dig}	Input capacitance, digital only port pins	V _{IN} = V _{SS} or V _{CC}			3		pF
C _{I,ana}	Input capacitance, port pins with shared analog functions ⁽¹⁾	V _{IN} = V _{SS} or V _{CC}			5		pF
I _{Ikg(Px.y)}	High-impedance input leakage current	Refer to notes ⁽²⁾ and ⁽³⁾	2.2 V, 3.0 V	-20		+20	nA
t _(int)	External interrupt timing (external trigger pulse duration to set interrupt flag) ⁽⁴⁾	Ports with interrupt capability (see block diagram and terminal function descriptions).	2.2 V, 3.0 V	20			ns
t _(RST)	External reset pulse duration on $\overline{\text{RST}}$ ⁽⁵⁾		2.2 V, 3.0 V	2			μs

- (1) If the port pins PJ.4/LFXIN and PJ.5/LFXOUT are used as digital I/Os, they are connected by a 4-pF capacitor and a 35-MΩ resistor in series. At frequencies of approximately 1 kHz and lower, the 4-pF capacitor can add to the pin capacitance of PJ.4/LFXIN and PJ.5/LFXOUT.
- (2) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
- (3) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
- (4) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It may be set by trigger signals shorter than t_(int).
- (5) Not applicable if the $\overline{\text{RST}}$ /NMI pin is configured as NMI.

Table 5-12. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH} High-level output voltage	I _(OHmax) = -1 mA ⁽¹⁾	2.2 V	V _{CC} - 0.25		V _{CC}	V
	I _(OHmax) = -3 mA ⁽²⁾		V _{CC} - 0.60		V _{CC}	
	I _(OHmax) = -2 mA ⁽¹⁾	3.0 V	V _{CC} - 0.25		V _{CC}	
	I _(OHmax) = -6 mA ⁽²⁾		V _{CC} - 0.60		V _{CC}	
V _{OL} Low-level output voltage	I _(OLmax) = 1 mA ⁽¹⁾	2.2 V	V _{SS}		V _{SS} + 0.25	V
	I _(OLmax) = 3 mA ⁽²⁾		V _{SS}		V _{SS} + 0.60	
	I _(OLmax) = 2 mA ⁽¹⁾	3.0 V	V _{SS}		V _{SS} + 0.25	
	I _(OLmax) = 6 mA ⁽²⁾		V _{SS}		V _{SS} + 0.60	
f _{Px,y} Port output frequency (with load) ⁽³⁾	C _L = 20 pF, R _L ^{(4) (5)}	2.2 V	16			MHz
		3.0 V	16			
f _{Port_CLK} Clock output frequency ⁽³⁾	ACLK, MCLK, or SMCLK at configured output port C _L = 20 pF ⁽⁵⁾	2.2 V	16			MHz
		3.0 V	16			
t _{rise,dig} Port output rise time, digital only port pins	C _L = 20 pF	2.2 V		4	15	ns
		3.0 V		3	15	
t _{fall,dig} Port output fall time, digital only port pins	C _L = 20 pF	2.2 V		4	15	ns
		3.0 V		3	15	
t _{rise,ana} Port output rise time, port pins with shared analog functions	C _L = 20 pF	2.2 V		6	15	ns
		3.0 V		4	15	
t _{fall,ana} Port output fall time, port pins with shared analog functions	C _L = 20 pF	2.2 V		6	15	ns
		3.0 V		4	15	

- (1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.
- (3) The port can output frequencies at least up to the specified limit. It might support higher frequencies.
- (4) A resistive divider with 2 × R1 and R1 = 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.
- (5) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.12.5.1 Typical Characteristics, Digital Outputs at 3.0 V and 2.2 V

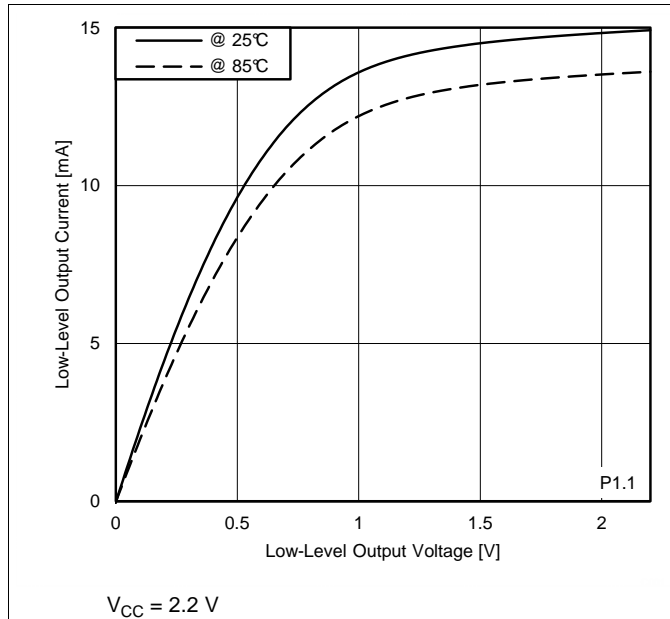


Figure 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage

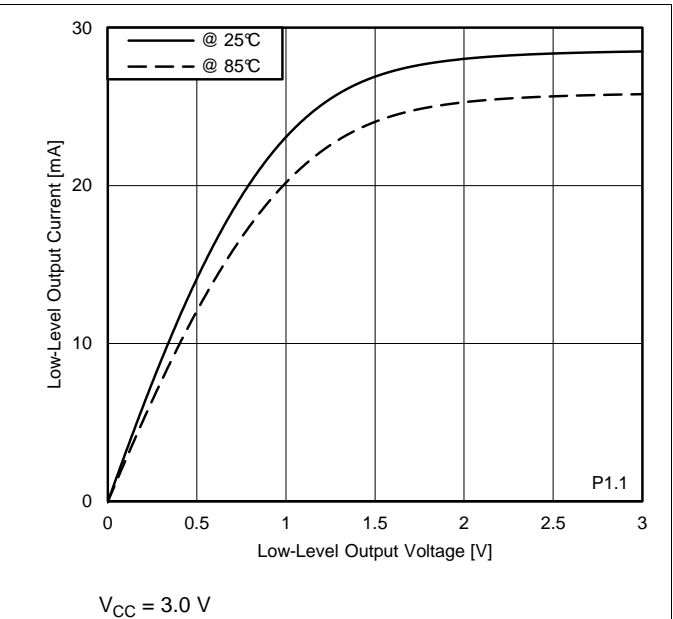


Figure 5-9. Typical Low-Level Output Current vs Low-Level Output Voltage

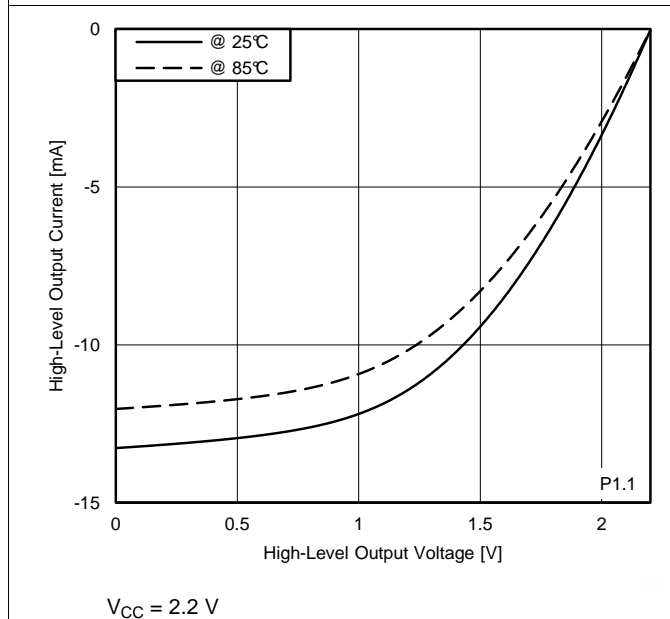


Figure 5-10. Typical High-Level Output Current vs High-Level Output Voltage

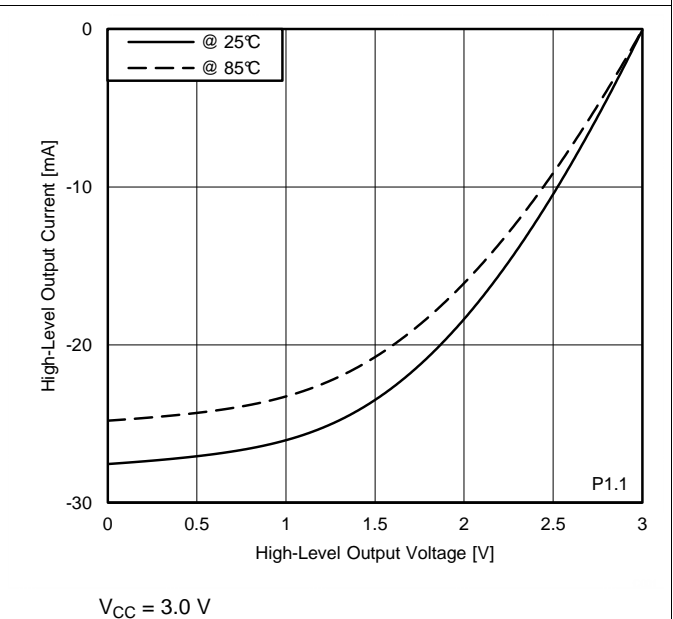


Figure 5-11. Typical High-Level Output Current vs High-Level Output Voltage

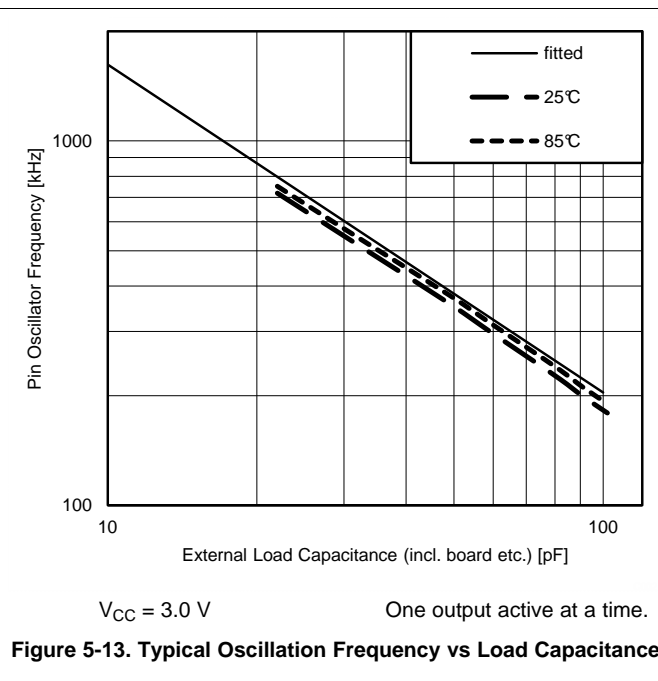
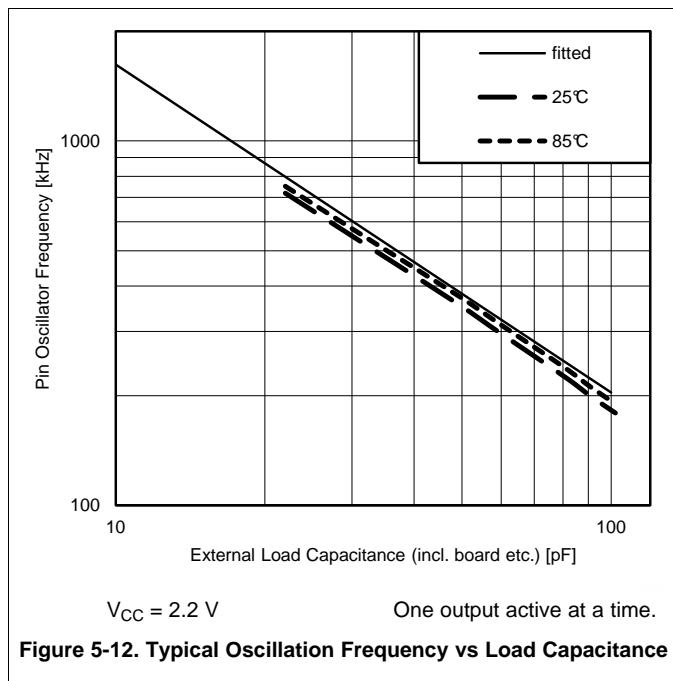
Table 5-13. Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{OPx,y}	Pin-oscillator frequency	Px,y, C _L = 10 pF ⁽¹⁾	3.0 V		1200		kHz
		Px,y, C _L = 20 pF ⁽¹⁾	3.0 V		650		kHz

(1) C_L is the external load capacitance connected from the output to V_{SS} and includes all parasitic effects such as PCB traces.

5.12.5.2 Typical Characteristics, Pin-Oscillator Frequency



5.12.6 Timer_A and Timer_B

Table 5-14. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10%	2.2 V, 3.0 V			16	MHz
t _{TA,cap}	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

Table 5-15. Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ± 10%	2.2 V, 3.0 V			16	MHz
t _{TB,cap}	Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	2.2 V, 3.0 V	20			ns

5.12.7 eUSCI

Table 5-16. eUSCI (UART Mode) Recommended Operating Conditions

PARAMETER		CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%			16	MHz
f _{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)				4	MHz

Table 5-17. eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _t	UCGLITx = 0	2.2 V, 3.0 V	5		30	ns
	UCGLITx = 1		20	90		
	UCGLITx = 2		35	160		
	UCGLITx = 3		50	220		
	UART receive deglitch time ⁽¹⁾					

- (1) Pulses on the UART receive input (UCxRX) that are shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum usable baud rate. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

Table 5-18. eUSCI (SPI Master Mode) Recommended Operating Conditions

PARAMETER	CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%		16	MHz

Table 5-19. eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10	1			UCxCLK cycles
t _{STE,LAG}	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10	1			
t _{STE,ACC}	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V		60	ns
t _{STE,DIS}	STE disable time, STE inactive to SOMI high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.2 V, 3.0 V		80	ns
t _{SU,MI}	SOMI input data setup time	2.2 V	40			ns
		3.0 V	40			
t _{HD,MI}	SOMI input data hold time	2.2 V	0			ns
		3.0 V	0			
t _{VALID,MO}	SIMO output data valid time ⁽²⁾	2.2 V			10	ns
		3.0 V			10	
t _{HD,MO}	SIMO output data hold time ⁽³⁾	2.2 V		0		ns
		3.0 V		0		

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, refer to the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-14](#) and [Figure 5-15](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in [Figure 5-14](#) and [Figure 5-15](#).

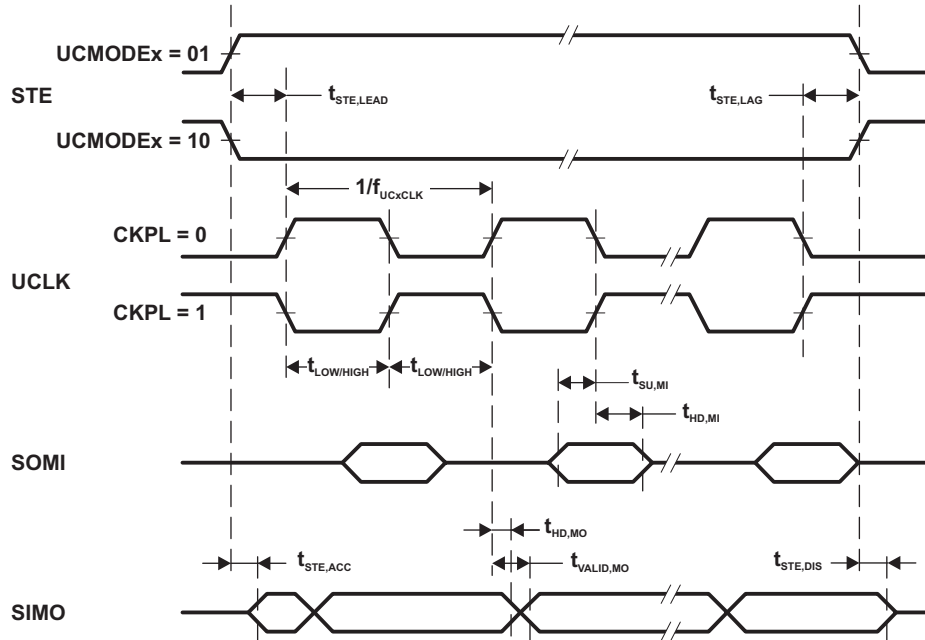


Figure 5-14. SPI Master Mode, CKPH = 0

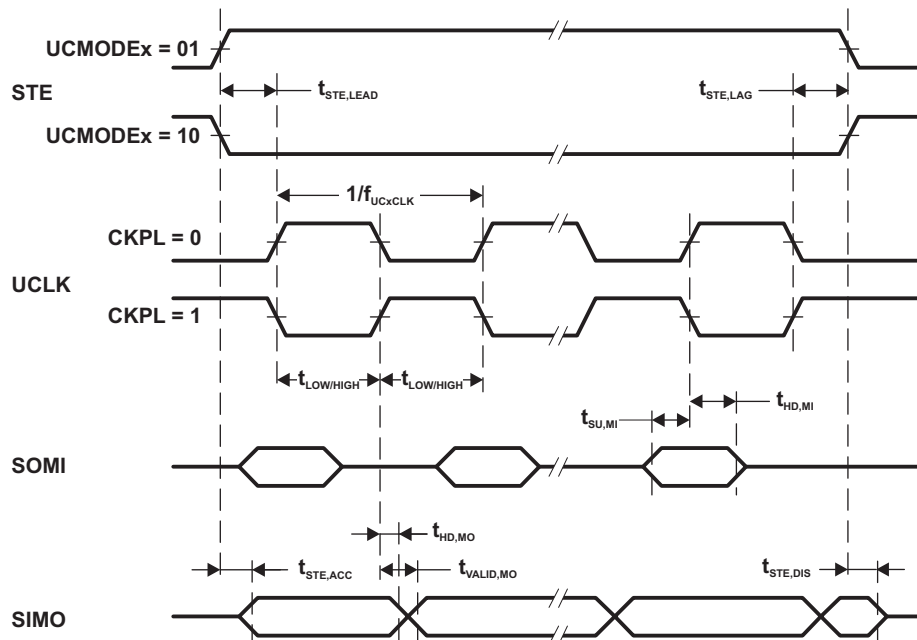


Figure 5-15. SPI Master Mode, CKPH = 1

Table 5-20. eUSCI (SPI Slave Mode)

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE active to clock		2.2 V	50			ns
			3.0 V	40			
t _{STE,LAG}	STE lag time, Last clock to STE inactive		2.2 V	2			ns
			3.0 V	3			
t _{STE,ACC}	STE access time, STE active to SOMI data out		2.2 V			50	ns
			3.0 V			40	
t _{STE,DIS}	STE disable time, STE inactive to SOMI high impedance		2.2 V			50	ns
			3.0 V			45	
t _{SU,SI}	SIMO input data setup time		2.2 V	4			ns
			3.0 V	4			
t _{HD,SI}	SIMO input data hold time		2.2 V	7			ns
			3.0 V	7			
t _{VALID,SO}	SOMI output data valid time ⁽²⁾	UCLK edge to SOMI valid, C _L = 20 pF	2.2 V			35	ns
			3.0 V			35	
t _{HD,SO}	SOMI output data hold time ⁽³⁾	C _L = 20 pF	2.2 V	0			ns
			3.0 V	0			

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-16](#) and [Figure 5-17](#).
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-16](#) and [Figure 5-17](#).

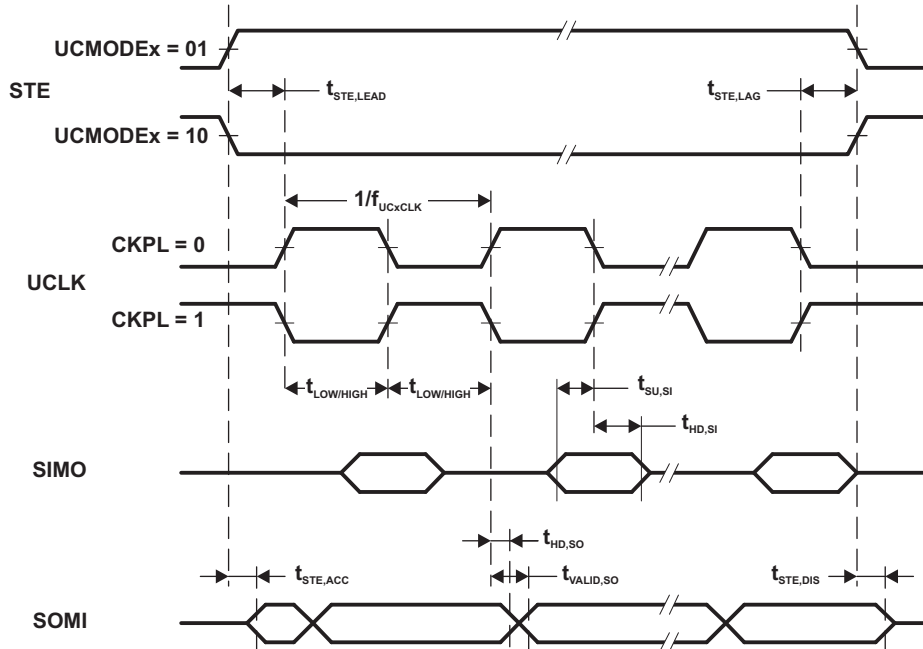


Figure 5-16. SPI Slave Mode, CKPH = 0

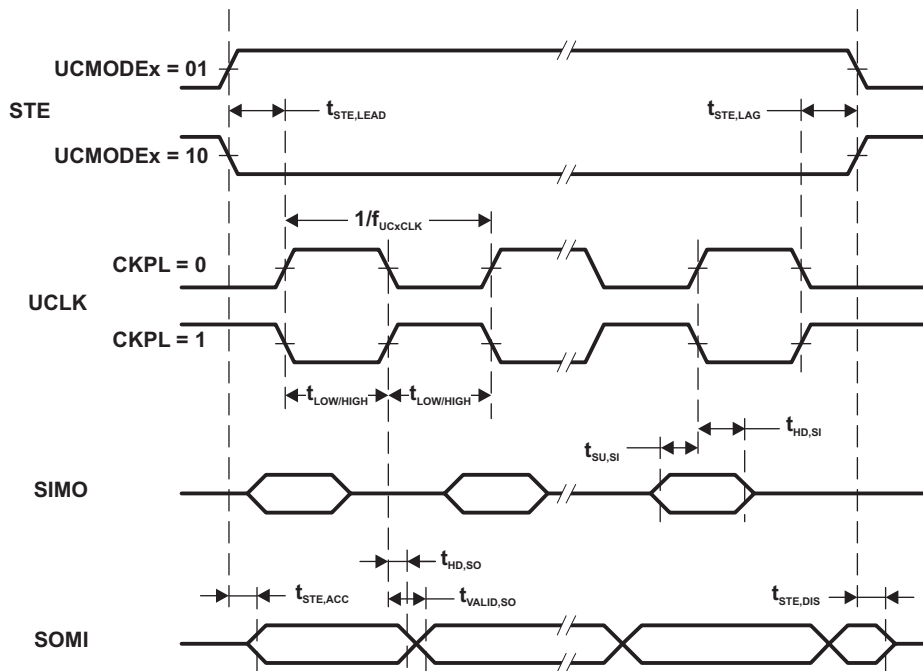


Figure 5-17. SPI Slave Mode, CKPH = 1

Table 5-21. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-18](#))

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
f _{eUSCI}	eUSCI input clock frequency				16	MHz	
f _{SCL}	SCL clock frequency	2.2 V, 3.0 V	0		400	kHz	
t _{HD,STA}	Hold time (repeated) START	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	2.2 V, 3.0 V	4.0 0.6		μs	
t _{SU,STA}	Setup time for a repeated START	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	2.2 V, 3.0 V	4.7 0.6		μs	
t _{HD,DAT}	Data hold time		2.2 V, 3.0 V	0		ns	
t _{SU,DAT}	Data setup time		2.2 V, 3.0 V	100		ns	
t _{SU,STO}	Setup time for STOP	f _{SCL} = 100 kHz f _{SCL} > 100 kHz	2.2 V, 3.0 V	4.0 0.6		μs	
t _{BUF}	Bus free time between a STOP and START condition	f _{SCL} = 100 kHz f _{SCL} > 100 kHz		4.7 1.3		us	
t _{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0 UCGLITx = 1 UCGLITx = 2 UCGLITx = 3	2.2 V, 3.0 V		50 25 12.5 6.3	250 125 62.5 31.5	ns
t _{TIMEOUT}	Clock low time-out	UCCLTOx = 1 UCCLTOx = 2 UCCLTOx = 3	2.2 V, 3.0 V		27 30 33		ms

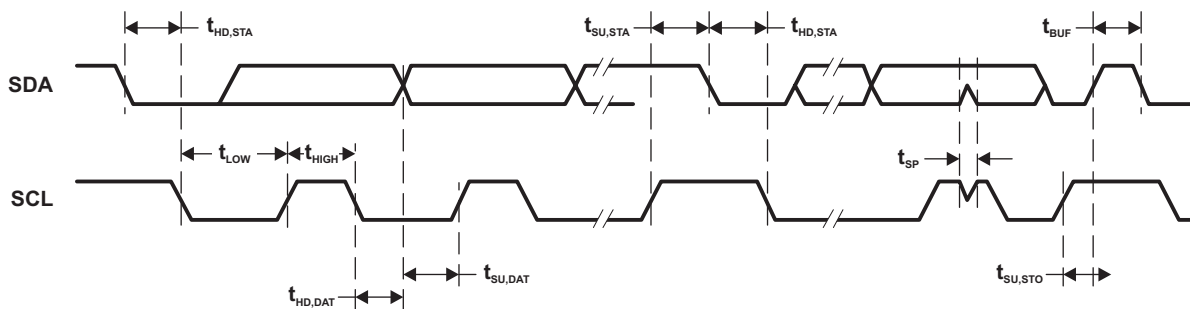


Figure 5-18. I²C Mode Timing

5.12.8 ADC12

Table 5-22. 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	NOM	MAX	UNIT
V(Ax)	Analog input voltage ⁽¹⁾	All ADC12 analog input pins Ax		0		AVCC	V
I(ADC12_B) single-ended mode	Operating supply current into AVCC plus DVCC terminal ^{(2) (3)}	f _{ADC12CLK} = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 0 REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		145	199	μA
			2.2 V		140	190	
I(ADC12_B) differential mode	Operating supply current into AVCC and DVCC terminals ^{(2) (3)}	f _{ADC12CLK} = MODCLK, ADC12ON = 1, ADC12PWRMD = 0, ADC12DIF = 1 REFON = 0, ADC12SHTx = 0, ADC12DIV = 0	3.0 V		175	245	μA
			2.2 V		170	230	
C _I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		10	15	pF
R _I	Input MUX ON resistance	0 V ≤ V(Ax) ≤ AVCC	>2V		0.5	4	kΩ
			<2V		1	10	

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.

(2) The internal reference supply current is not included in current consumption parameter I(ADC12_B).

(3) Typically about 60% of the total current into the AVCC and DVCC terminal is from AVCC.

Table 5-23. 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{ADC12CLK}	Specified performance	For specified performance of ADC12 linearity parameters with ADC12PWRMD = 0. If ADC12PWRMD = 1, the maximum is 1/4 of the value shown here.		0.45		5.4	MHz
f _{ADC12CLK}	Reduced performance	Linearity parameters have reduced performance			32.768		kHz
f _{ADC12OSC}	Internal oscillator ⁽¹⁾	ADC12DIV = 0, f _{ADC12CLK} = f _{ADC12OSC} from MODCLK		4	4.8	5.4	MHz
t _{CONVERT}	Conversion time	REFON = 0, Internal oscillator f _{ADC12CLK} = f _{ADC12OSC} from MODCLK, ADC12WINC = 0		2.6		3.5	μs
		External f _{ADC12CLK} from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			(2)		
t _{ADC12ON}	Turn on settling time of the ADC	See ⁽³⁾				100	ns
t _{ADC12OFF}	Time ADC must be off before can be turned on again	t _{ADC12OFF} must be met to make sure t _{ADC12ON} time holds		100			ns
t _{Sample}	Sampling time	R _S = 400 Ω, R _I = 4 kΩ, C _I = 15 pF, C _{pext} = 8 pF ⁽⁴⁾		1			μs

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.

(2) 14 × ADC12DIV × 1/f_{ADC12CLK}. If ADC12WINC = 1, then 15 × ADC12DIV × 1/f_{ADC12CLK}

(3) The condition is that the error in a conversion started after t_{ADC12ON} is less than ±0.5 LSB. The reference and input signals are already settled.

(4) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB: t_{sample} = ln(2ⁿ⁺²) × (R_S + R_I) × (C_I + C_{pext}), where n = ADC resolution = 12, R_S = external source resistance, C_{pext} = external parasitic capacitance.

Table 5-24. 12-Bit ADC, Linearity Parameters With External Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	Number of no missing code output-code bits		12			bits
E _I	Integral linearity error (INL) for differential input	1.2V ≤ V _{R+} - V _{R-} ≤ AV _{CC}			±1.8	LSB
E _I	Integral linearity error (INL) for single ended inputs	1.2V ≤ V _{R+} - V _{R-} ≤ AV _{CC}			±2.2	LSB
E _D	Differential linearity error (DNL)		-0.99		+1.0	LSB
E _O	Offset error ^{(2) (3)}	ADC12VRSEL = 0x2 or 0x4 without TLV calibration, TLV calibration data can be used to improve the parameter ⁽⁴⁾		±0.5	±1.5	mV
E _{G,ext}	Gain error	With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter ⁽⁴⁾ , VR+ = 2.5 V, VR- = AVSS		±0.8	±2.5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), VR+ = 2.5 V, VR- = AVSS		±1	±20	
E _{T,ext}	Total unadjusted error	With external voltage reference without internal buffer (ADC12VRSEL = 0x2 or 0x4) without TLV calibration, TLV calibration data can be used to improve the parameter ⁽⁴⁾ , VR+ = 2.5 V, VR- = AVSS		±1.4	±3.5	LSB
		With external voltage reference with internal buffer (ADC12VRSEL = 0x3), VR+ = 2.5 V, VR- = AVSS		±1.4	±21.0	

- See [Table 5-26](#) and [Table 5-32](#) electrical sections for more information on internal reference performance and refer to the application report *Designing With the MSP430FR59xx and MSP430FR58xx ADC* ([SLAA624](#)) for details on optimizing ADC performance for your application with the choice of internal versus external reference.
- Offset is measured as the input voltage (at which ADC output transitions from 0 to 1) minus 0.5 LSB.
- Offset increases as IR drop increases when VR- is AVSS.
- For details, see the device descriptor table section in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* ([SLAU367](#)).

Table 5-25. 12-Bit ADC, Dynamic Performance for Differential Inputs With External Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	VR+ = 2.5 V, VR- = AVSS	68	71		dB
ENOB	Effective number of bits ⁽²⁾	VR+ = 2.5 V, VR- = AVSS	10.7	11.2		bits

- See [Table 5-26](#) and [Table 5-32](#) electrical sections for more information on internal reference performance and refer to the application report *Designing With the MSP430FR59xx and MSP430FR58xx ADC* ([SLAA624](#)) for details on optimizing ADC performance for your application with the choice of internal versus external reference.
- ENOB = (SINAD - 1.76) / 6.02

Table 5-26. 12-Bit ADC, Dynamic Performance for Differential Inputs With Internal Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits ⁽²⁾	VR+ = 2.5V, VR- = AVSS	10.3	10.7		Bits

- See [Table 5-32](#) electrical section for more information on internal reference performance and refer to the application report *Designing With the MSP430FR59xx and MSP430FR58xx ADC* ([SLAA624](#)) for details on optimizing ADC performance for your application with the choice of internal versus external reference.
- ENOB = (SINAD - 1.76) / 6.02

Table 5-27. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With External Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	VR+ = 2.5 V, VR- = AVSS	64	68		dB
ENOB	Effective number of bits ⁽²⁾	VR+ = 2.5 V, VR- = AVSS	10.2	10.7		bits

(1) See [Table 5-28](#) and [Table 5-32](#) electrical sections for more information on internal reference performance and refer to the application report *Designing With the MSP430FR59xx and MSP430FR58xx ADC* ([SLAA624](#)) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-28. 12-Bit ADC, Dynamic Performance for Single-Ended Inputs With Internal Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits ⁽²⁾	VR+ = 2.5 V, VR- = AVSS	9.4	10.4		bits

(1) See [Table 5-32](#) electrical section for more information on internal reference performance and refer to the application report *Designing With the MSP430FR59xx and MSP430FR58xx ADC* ([SLAA624](#)) for details on optimizing ADC performance for your application with the choice of internal versus external reference.

(2) ENOB = (SINAD – 1.76) / 6.02

Table 5-29. 12-Bit ADC, Dynamic Performance With 32.768-kHz Clock

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits ⁽¹⁾	Reduced performance with f _{ADC12CLK} from ACLK LFXT 32.768 KHz, VR+ = 2.5 V, VR- = AVSS		10		bits

(1) ENOB = (SINAD – 1.76) / 6.02

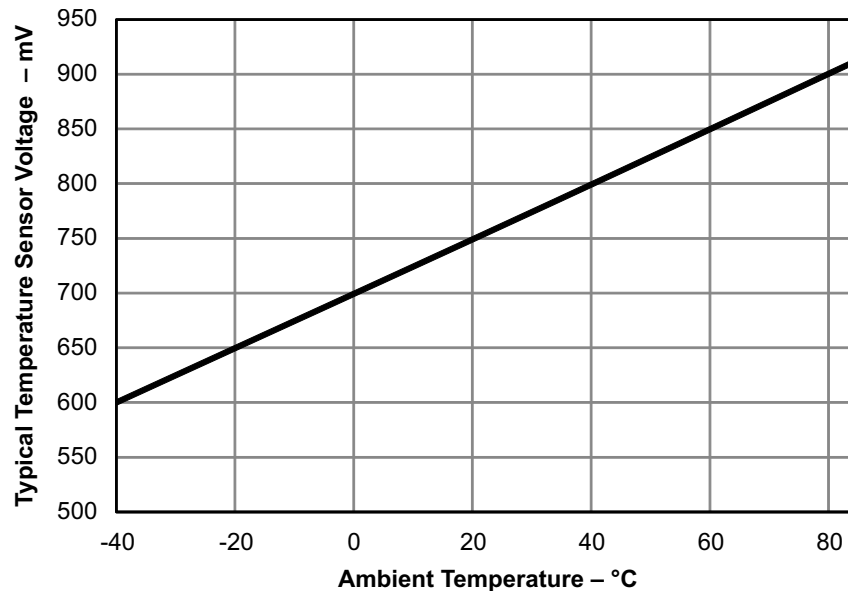


Figure 5-19. Typical Temperature Sensor Voltage

Table 5-30. 12-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1) (2)	ADC12ON = 1, ADC12TCMAP = 1, $T_A = 0^{\circ}C$			700		mV
TC_{SENSOR}	See (2)	ADC12ON = 1, ADC12TCMAP = 1			2.5		mV/ $^{\circ}C$
$t_{SENSOR(sample)}$	Sample time required if ADC12TCMAP = 1 and channel (MAX - 1) is selected ⁽³⁾	ADC12ON = 1, ADC12TCMAP = 1, Error of conversion result ≤ 1 LSB		30			μs
$V_{1/2}$	AVCC voltage divider for ADC12BATMAP = 1 on MAX input channel	ADC12ON = 1, ADC12BATMAP = 1		47.5%	50%	52.5%	
$I_{V_{1/2}}$	current for battery monitor during sample time	ADC12ON = 1, ADC12BATMAP = 1			38	72	μA
$t_{V_{1/2}(sample)}$	Sample time required if ADC12BATMAP = 1 and channel MAX is selected ⁽⁴⁾	ADC12ON = 1, ADC12BATMAP = 1		1.7			μs

- (1) The temperature sensor offset can be as much as $\pm 30^{\circ}C$. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for $30^{\circ}C \pm 3^{\circ}C$ and $85^{\circ}C \pm 3^{\circ}C$ for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} * (\text{Temperature, } ^{\circ}C) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 250 k Ω . The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
- (4) The on-time $t_{V_{1/2}(on)}$ is included in the sampling time $t_{V_{1/2}(sample)}$; no additional on time is needed.

Table 5-31. 12-Bit ADC, External Reference⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{R+}	Positive external reference voltage input V_{eREF+} or V_{eREF-} based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	1.2	AV_{CC}	V
V_{R-}	Negative external reference voltage input V_{eREF+} or V_{eREF-} based on ADC12VRSEL bit	$V_{R+} > V_{R-}$	0	1.2	V
$(V_{R+} - V_{R-})$	Differential external reference voltage input	$V_{R+} > V_{R-}$	1.2	AV_{CC}	V
I_{VeREF+} I_{VeREF-}	Static input current singled ended input mode	$1.2 V \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0 V$ $f_{ADC12CLK} = 5 MHz$, ADC12SHTx = 1h, ADC12DIF = 0, ADC12PWRMD = 0		± 10	μA
I_{VeREF+} I_{VeREF-}	Static input current differential input mode	$1.2 V \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0 V$ $f_{ADC12CLK} = 5 MHz$, ADC12SHTx = 8h, ADC12DIF = 0, ADC12PWRMD = 01		± 2.5	μA
I_{VeREF+} I_{VeREF-}	Static input current differential input mode	$1.2 V \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0 V$ $f_{ADC12CLK} = 5 MHz$, ADC12SHTx = 1h, ADC12DIF = 1, , ADC12PWRMD = 0		± 20	μA
I_{VeREF+} I_{VeREF-}	Static input current differential input mode	$1.2 V \leq V_{eREF+} \leq V_{AVCC}$, $V_{eREF-} = 0 V$ $f_{ADC12CLK} = 5 MHz$, ADC12SHTx = 8h, ADC12DIF = 1, , ADC12PWRMD = 1		± 5	μA
I_{VeREF+}	Peak input current with single ended input	$0 V \leq V_{eREF+} \leq V_{AVCC}$, ADC12DIF = 0		1.5	mA
I_{VeREF+}	Peak input current with differential input	$0 V \leq V_{eREF+} \leq V_{AVCC}$, ADC12DIF = 1		3	mA
$C_{VeREF+/-}$	Capacitance at V_{eREF+} or V_{eREF-} terminal	See (2)	10		μF

- (1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i , is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
- (2) Two decoupling capacitors, 10 μF and 470 nF, should be connected to V_{eREF} to decouple the dynamic current required for an external reference source if it is used for the ADC12_B. See also the *MSP430FR58xx*, *MSP430FR59xx*, *MSP430FR68xx*, and *MSP430FR69xx* Family User's Guide ([SLAU367](#)).

5.12.9 REF Module

Table 5-32. REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = 1	2.7 V	2.5	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1	2.2 V	2.0	±1.5%	
		REFVSEL = {0} for 1.2 V, REFON = 1	1.8 V	1.2	±1.8%	
Noise	RMS noise at VREF ⁽¹⁾	From 0.1 Hz to 10 Hz, REFVSEL = {0}		110	600	µV
V _{OS_BUF_INT}	VREF ADC BUF_INT buffer offset ⁽²⁾	T _A = 25°C, ADC ON, REFVSEL = {0}, REFON = 1, REFOUT = 0	-12		+12	mV
V _{OS_BUF_EXT}	VREF ADC BUF_EXT buffer offset ⁽³⁾	T _A = 25°C, REFVSEL = {0}, REFOUT = 1, REFON = 1 or ADC ON	-12		+12	mV
AV _{CC(min)}	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.8		V
		REFVSEL = {1} for 2.0 V		2.2		
		REFVSEL = {2} for 2.5 V		2.7		
I _{REF+}	Operating supply current into AVCC terminal ⁽⁴⁾	REFON = 1	3 V	8	15	µA
I _{REF+_ADC_BUF}	Operating supply current into AVCC terminal ⁽⁴⁾	ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0,	3 V	225	355	µA
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 0	3 V	1030	1660	
		ADC ON, REFOUT = 0, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1	3 V	120	185	
		ADC ON, REFOUT = 1, REFVSEL = {0, 1, 2}, ADC12PWRMD = 1	3 V	545	895	
		ADC OFF, REFON=1, REFOUT=1, REFVSEL = {0, 1, 2}	3 V	1085	1780	
I _{O(VREF+)}	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 2}, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1		-1000	+10	µA
ΔV _{out} /ΔI _o (VREF+)	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 2}, I _{O(VREF+)} = +10 µA or -1000 µA, AVCC = AVCC(min) for each reference level, REFON = REFOUT = 1			2500	µV/mA
C _{VREF+/-}	Capacitance at VREF+ and VREF- terminals	REFON = REFOUT = 1		0	100	pF
TC _{REF+}	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 2}, REFON = REFOUT = 1, T _A = -40°C to 85°C ⁽⁵⁾		18	50	ppm/K
PSRR _{DC}	Power supply rejection ratio (dc)	AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1		120	400	µV/V
PSRR _{AC}	Power supply rejection ratio (ac)	dAV _{CC} = 0.1 V at 1 kHz		3.0		mV/V
t _{SETTLE}	Settling time of reference voltage ⁽⁶⁾	AV _{CC} = AV _{CC(min)} - AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1		75	80	µs

- (1) Internal reference noise affects ADC performance when ADC uses internal reference. Refer to the application report *Designing With the MSP430FR59xx and MSP430FR58xx ADC* ([SLAA624](#)) for details on optimizing ADC performance for your application with the choice of internal versus external reference.
- (2) Buffer offset affects ADC gain error and thus total unadjusted error.
- (3) Buffer offset affects ADC gain error and thus total unadjusted error.
- (4) The internal reference current is supplied through terminal AVCC.
- (5) Calculated using the box method: (MAX(-40°C to 85°C) - MIN(-40°C to 85°C)) / MIN(-40°C to 85°C)/(85°C - (-40°C)).
- (6) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.12.10 Comparator

Table 5-33. Comparator_E

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{AVCC_COMP}	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3.0 V		11	20	μA
	CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)			9	17	
	CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T _A = 30°C				0.5	
	CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T _A = 85°C				1.3	
I _{AVCC_REF}	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 0	2.2 V, 3.0 V		12	15	μA
	CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0, CEREFACC = 1			5	7	
V _{REF}	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.8 V	1.17	1.2	1.23	V
	CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V	1.92	2.0	2.08	
	CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V	2.40	2.5	2.60	
	CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.8 V	1.10	1.2	1.245	
	CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V	1.90	2.0	2.08	
	CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V	2.35	2.5	2.60	
V _{IC}	Common mode input range		0		V _{CC} -1	V
V _{OFFSET}	CEPWRMD = 00		-32		32	mV
	CEPWRMD = 01		-32		32	
	CEPWRMD = 10		-30		30	
C _{IN}	CEPWRMD = 00 or CEPWRMD = 01			9		pF
	CEPWRMD = 10			9		
R _{SIN}	ON - switch closed			1	3	kΩ
	OFF - switch open		50			MΩ
t _{PD}	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			260	330	ns
	CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			350	460	
	CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV				15	μs
t _{PD,filter}	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00			700	1000	ns
	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01			1.0	1.8	μs
	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10			2.0	3.5	
	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11			4.0	7.0	
t _{EN_CMP}	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 00			0.9	1.5	μs
	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 01			0.9	1.5	
	CEON = 0 → 1, VIN+, VIN- from pins, Overdrive ≥ 20 mV, CEPWRMD = 10			15	100	

Comparator_E (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{EN_CMP_VREF} Comparator and reference ladder and reference voltage enable time	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 11, REFON = 0, Overdrive ≥ 20 mV, CEPWRMD = 00			1	2	μs
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 11, REFON = 0, Overdrive ≥ 20 mV, CEPWRMD = 01			1	2	
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 11, REFON = 0, Overdrive ≥ 20 mV, CEPWRMD = 10			10	50	
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 0, CEREF ₀ = CEREF ₁ = 0x0F, Overdrive ≥ 20 mV, CEPWRMD = 00			2	5	
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 0, CEREF ₀ = CEREF ₁ = 0x0F, Overdrive ≥ 20 mV, CEPWRMD = 01			2	5	
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 0, CEREF ₀ = CEREF ₁ = 0x0F, Overdrive ≥ 20 mV, CEPWRMD = 10			10	50	
t _{EN_CMP_RL} Comparator and reference ladder enable time	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 1, CEREF ₀ = CEREF ₁ = 0x0F, Overdrive ≥ 20 mV, CEPWRMD = 00			1	2	μs
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 1, CEREF ₀ = CEREF ₁ = 0x0F, Overdrive ≥ 20 mV, CEPWRMD = 01			1	2	
	CEON = 0 → 1, CEREF _{FLX} = 10, CERS _x = 10, REFON = 1, CEREF ₀ = CEREF ₁ = 0x0F, Overdrive ≥ 20 mV, CEPWRMD = 10			10	50	
V _{CE_REF} Reference voltage for a given tap	V _{IN} = reference into resistor ladder, n = 0 to 31		V _{IN} × (n+0.9) / 32	V _{IN} × (n+1) / 32	V _{IN} × (n+1.1) / 32	V

5.12.11 FRAM Controller

Table 5-34. FRAM Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Read and write endurance			10 ¹⁵			cycles
t _{Retention}	Data retention duration	T _J = 25°C	100			years
		T _J = 70°C	40			
		T _J = 85°C	10			
I _{WRITE}	Current to write into FRAM		I _{READ} ⁽¹⁾			nA
I _{ERASE}	Erase current		N/A ⁽²⁾			nA
t _{WRITE}	Write time		t _{READ} ⁽³⁾			ns
t _{READ}	Read time, NWAITSx=0		1/f _{SYSTEM} ⁽⁴⁾			ns
	Read time, NWAITSx=1		2/f _{SYSTEM} ⁽⁴⁾			ns

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption numbers I_{AM,FRAM}.

(2) N/A = not applicable. FRAM does not require a special erase sequence.

(3) Writing into FRAM is as fast as reading.

(4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

5.12.12 Emulation and Debug

Table 5-35. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{JTAG}	Supply current adder when JTAG active (but not clocked)	2.2 V, 3.0 V		40	100	μ A
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3.0 V	0		10	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3.0 V	0.04		15	μ s
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾	2.2 V, 3.0 V			110	μ s
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	μ s
f_{TCK}	TCK input frequency - 4-wire JTAG ⁽²⁾	2.2 V	0		16	MHz
		3.0 V	0		16	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	2.2 V, 3.0 V	20	35	50	k Ω
f_{TCLK}	TCLK/MCLK frequency during JTAG access, no FRAM access (limited by f_{SYSTEM})				16	MHz
$t_{TCLK,Low/High}$	TCLK low or high clock pulse duration, no FRAM access				25	ns
$f_{TCLK,FRAM}$	TCLK/MCLK frequency during JTAG access, including FRAM access (limited by f_{SYSTEM} with no FRAM wait states)				4	MHz
$t_{TCLK,FRAM,Low/High}$	TCLK low or high clock pulse duration, including FRAM accesses				100	ns

- (1) Tools accessing the Spy-Bi-Wire interface need to wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The Texas Instruments MSP430FR597x(1) and MSP430FR587x(1) family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with seven low-power modes is optimized to achieve extended battery life for example in portable measurement applications. The devices features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The devices are microcontroller configurations with up to five 16-bit timers, Comparator, universal serial communication interfaces (eUSCI) that supports UART, SPI, and I²C, a hardware multiplier, an AES accelerator, DMA, a real-time clock module with alarm capabilities, up to 52 I/O pins, and a high-performance 12-bit analog-to-digital converter (ADC).

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. CPUxV2 can also operate on address-word data (20-bit).

6.3 Operating Modes

The device has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Table 6-1. Operating Modes

Mode	AM		LPM0	LPM1	LPM2	LPM3	LPM4	LPM3.5	LPM4.5	
	Active	Active, FRAM Off ⁽¹⁾	CPU Off ⁽²⁾	CPU Off	Standby	Standby	Off	RTC-only	Shutdown with SVS	Shutdown without SVS
Maximum System Clock	16 MHz		16 MHz	16 MHz	50 kHz	50 kHz	0 ⁽³⁾	50 kHz	0 ⁽³⁾	
Typical Current Consumption, 25°C	103 µA/MHz	65 µA/MHz	75 µA at 1 MHz	40 µA at 1 MHz	0.9 µA	0.4 µA	0.3 µA	0.35 µA	0.2 µA	0.02 µA
Typical Wake-up time	N/A		instant.	6 µs	6 µs	7 µs	7 µs	250 µs	250 µs	1000 µs
Wake-up events	N/A		all	all	LF RTC I/O Comp	LF RTC I/O Comp	I/O Comp	RTC I/O	I/O	
CPU	on		off	off	off	off	off	reset	reset	
FRAM	on	off ⁽¹⁾	standby (or off ⁽¹⁾)	off	off	off	off	off	off	
High-frequency peripherals	available		available	available	off	off	off	reset	reset	
Low-frequency peripherals	available		available	available	available	available ⁽⁴⁾	off	RTC	reset	
Unlocked peripherals ⁽⁵⁾	available		available	available	available	available ⁽⁴⁾	available ⁽⁴⁾	reset	reset	
MCLK	on		off	off	off	off	off	off	off	
SMCLK	opt. ⁽⁶⁾		opt. ⁽⁶⁾	opt. ⁽⁶⁾	off	off	off	off	off	
ACLK	on		on	on	on	on	off	off	off	
Full retention	yes		yes	yes	yes	yes ⁽⁷⁾	yes ⁽⁷⁾	no	no	
SVS	always		always	always	opt. ⁽⁸⁾	opt. ⁽⁸⁾	opt. ⁽⁸⁾	opt. ⁽⁸⁾	on ⁽⁹⁾	off ⁽¹⁰⁾
Brownout	always		always	always	always	always	always	always	always	

- (1) FRAM disabled in FRAM controller
- (2) Disabling the FRAM via the FRAM controller decreases the LPM current consumption, but the wake-up time can increase. If the wake-up is for FRAM access (for example, to fetch an interrupt vector), wake-up time is increased. If the wake-up is for a non-FRAM operation (for example, DMA transfer to RAM), wake-up time is not increased.
- (3) All clocks disabled
- (4) See [Section 6.3.1](#), which describes the use of peripherals in LPM3 and LPM4.
- (5) "Unlocked peripherals" are peripherals that do not require a clock source to operate; for example, the comparator and REF, or the eUSCI when operated as an SPI slave.
- (6) Controlled by SMCLKOFF
- (7) Using the RAM Controller, the RAM can be completely powered down to save leakage; however, all data is lost.
- (8) Activated SVS (SVSHE = 1) results in higher current consumption. SVS not included in typical current consumption.
- (9) SVSHE = 1
- (10) SVSHE = 0

6.3.1 Peripherals in LPM3 and LPM4

Most peripherals can be activated to be operational in LPM3 if clocked by ACLK. Some modules are even operational in LPM4 because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder, certain peripherals are group together. To achieve optimal current consumption try to use modules within one group and to limit the number of groups with active modules. The grouping is shown in [Table 6-2](#). Modules not listed there are either already included in the standard LPM3 current consumption specifications or cannot be used in LPM3 or LPM4.

The idle current adder is very small at room temperature (25°C) but increases at high temperatures (85°C); refer to the I_{IDLE} current parameters in the electrical characteristics section for details.

Table 6-2. Peripheral Groups

Group A	Group B	Group C
Timer TA0	Timer TA2	Timer TA3
Timer TA1	Timer B0	eUSCI_A1
Comparator	eUSCI_A0	
ADC12_B	eUSCI_B0	
REF_A	eUSCI_B1	

6.4 Interrupt Vector Table and Signatures

The interrupt vectors, the power-up start address, and signatures are located in the address range 0FFFFh to 0FF80h. [Table 6-3](#) summarizes the content of this address range.

The power-up start address or reset vector is located at 0FFFFh to 0FFFEh. It contains the 16-bit address pointing to the start address of the application program.

The interrupt vectors start at 0FFFDh extending to lower addresses. Each vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

The vectors programmed into the address range from 0FFFFh to 0FFE0h are used as BSL password (if enabled by the corresponding signature)

The signatures are located at 0FF80h extending to higher addresses. Signatures are evaluated during device start-up. Starting from address 0FF88h extending to higher addresses a JTAG password can be programmed. The password can extend into the interrupt vector locations using the interrupt vector addresses as additional bits for the password.

Refer to the chapter "System Resets, Interrupts, and Operating Modes, System Control Module (SYS)" in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide (SLAU367)* for details.

Table 6-3. Interrupt Sources, Flags, Vectors, and Signatures

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up, Brownout, Supply Supervisor External Reset \overline{RST} Watchdog Time-out (Watchdog mode) WDT, FRCTL MPU, CS, PMM Password Violation FRAM uncorrectable bit error detection FRAM access time error MPU segment violation Software POR, BOR	SVSHIFG PMMRSTIFG WDTIFG WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW UBDIFG ACCTEIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG PMMPORIFG, PMMBORIFG (SYSRSTIV) ⁽¹⁾ ⁽²⁾	Reset	0FFFEh	highest
System NMI Vacant Memory Access JTAG Mailbox FRAM bit error detection MPU segment violation	VMAIFG JMBNIFG, JMBOUTIFG CBDIFG, UBDIFG MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG (SYSSNIV) ⁽¹⁾ ⁽³⁾	(Non)maskable	0FFFCh	
User NMI External NMI Oscillator Fault	NMIIIFG, OFIFG (SYSUNIV) ⁽¹⁾ ⁽³⁾	(Non)maskable	0FFFAh	
Comparator_E	Comparator_E interrupt flags (CEIV) ⁽¹⁾	Maskable	0FFF8h	
Timer_B TB0	TB0CCR0.CCIFG	Maskable	0FFF6h	
Timer_B TB0	TB0CCR1.CCIFG ... TB0CCR6.CCIFG, TB0CTL.TBIFG (TB0IV) ⁽¹⁾	Maskable	0FFF4h	
Watchdog Timer (Interval Timer Mode)	WDTIFG	Maskable	0FFF2h	
Reserved	Reserved	Maskable	0FFF0h	

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space

(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

Table 6-3. Interrupt Sources, Flags, Vectors, and Signatures (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
eUSCI_A0 Receive or Transmit	UCA0IFG: UCRXIFG, UCTXIFG (SPI mode) UCA0IFG: UCSTTIFG, UCTXCFIFG, UCRXIFG, UCTXIFG (UART mode) (UCA0IV) ⁽¹⁾	Maskable	0FFEEh	
eUSCI_B0 Receive or Transmit	UCB0IFG: UCRXIFG, UCTXIFG (SPI mode) UCB0IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB0IV) ⁽¹⁾	Maskable	0FFEC h	
ADC12_B	ADC12IFG0 ... ADC12IFG31 ADC12LOIFG, ADC12INIFG, ADC12HIIFG, ADC12RDYIFG, ADC12OVIFG, ADC12TOVIFG (ADC12IV) ^{(1) (4)}	Maskable	0FFEAh	
Timer_A TA0	TA0CCR0.CCIFG	Maskable	0FFE8h	
Timer_A TA0	TA0CCR1.CCIFG ... TA0CCR2.CCIFG, TA0CTL.TAIFG (TA0IV) ⁽¹⁾	Maskable	0FFE6h	
eUSCI_A1 Receive or Transmit	UCA1IFG: UCRXIFG, UCTXIFG (SPI mode) UCA1IFG: UCSTTIFG, UCTXCFIFG, UCRXIFG, UCTXIFG (UART mode) (UCA1IV) ⁽¹⁾	Maskable	0FFE4h	
eUSCI_B1 Receive or Transmit (Reserved on MSP430FR592x)	UCB1IFG: UCRXIFG, UCTXIFG (SPI mode) UCB1IFG: UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I ² C mode) (UCB1IV) ⁽¹⁾	Maskable	0FFE2h	
DMA	DMA0CTL.DMAIFG, DMA1CTL.DMAIFG, DMA2CTL.DMAIFG (DMAIV) ⁽¹⁾	Maskable	0FFE0h	
Timer_A TA1	TA1CCR0.CCIFG	Maskable	0FFDEh	
Timer_A TA1	TA1CCR1.CCIFG ... TA1CCR2.CCIFG, TA1CTL.TAIFG (TA1IV) ⁽¹⁾	Maskable	0FFDCh	
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾	Maskable	0FFDAh	
Timer_A TA2	TA2CCR0.CCIFG	Maskable	0FFD8h	
Timer_A TA2	TA2CCR1.CCIFG TA2CTL.TAIFG (TA2IV) ⁽¹⁾	Maskable	0FFD6h	
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) ⁽¹⁾	Maskable	0FFD4h	
Timer_A TA3	TA3CCR0.CCIFG	Maskable	0FFD2h	
Timer_A TA3	TA3CCR1.CCIFG TA3CTL.TAIFG (TA3IV) ⁽¹⁾	Maskable	0FFD0h	
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV) ⁽¹⁾	Maskable	0FFCEh	
I/O Port P4	P4IFG.0 to P4IFG.7 (P4IV) ⁽¹⁾	Maskable	0FFCCh	
Reserved			0FFCAh	
RTC_C	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) ⁽¹⁾	Maskable	0FFC8h	
AES	AESRDYIFG	Maskable	0FFC6h	lowest

(4) Only on devices with ADC, otherwise reserved.

Table 6-3. Interrupt Sources, Flags, Vectors, and Signatures (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved	Reserved ⁽⁵⁾		0FFC4h	
			⋮	
			0FF8Ch	
Signatures ⁽⁶⁾	IP Encapsulation Signature2 ⁽⁵⁾		0FF8Ah	
	IP Encapsulation Signature1 ^{(5) (7)}		0FF88h	
	BSL Signature2		0FF86h	
	BSL Signature1		0FF84h	
	JTAG Signature2		0FF82h	
	JTAG Signature1		0FF80h	

(5) May contain a JTAG password required to enable JTAG access to the device.

(6) Signatures are evaluated during device start-up. See the "System Resets, Interrupts, and Operating Modes, System Control Module (SYS)" chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide (SLAU367)* for details.

(7) Must not contain 0AAAAh if used as JTAG password.

6.5 Bootstrap Loader (BSL)

The BSL enables programming of the FRAM or RAM using a UART serial interface (FRxxxx devices) or an I²C interface (FRxxxx1 devices). Access to the device memory via the BSL is protected by a user-defined password. Use of the BSL requires four pins as shown in [Table 6-4](#). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide* ([SLAU265](#)).

Table 6-4. BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
BSL_TX	Devices with UART BSL (FRxxxx): Data transmit
BSL_RX	Devices with UART BSL (FRxxxx): Data receive
BSL_DAT	Devices with I ² C BSL (FRxxxx1): Data
BSL_CLK	Devices with I ² C BSL (FRxxxx1): Clock
VCC	Power supply
VSS	Ground supply

6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in [Table 6-5](#). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* ([SLAU320](#)).

Table 6-5. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in [Table 6-6](#). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)).

Table 6-6. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 FRAM

The FRAM can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Ultra-low-power ultra-fast-write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait-state generation
- Error correction coding (ECC)

NOTE

Wait States

For MCLK frequencies > 8 MHz, wait states must be configured following the flow described in the "Wait State Control" section of the "FRAM Controller (FRCTRL)" chapter in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide (SLAU367)*.

For important software design information regarding FRAM including but not limited to partitioning the memory layout according to application-specific code, constant, and data space requirements, the use of FRAM to optimize application energy consumption, and the use of the Memory Protection Unit (MPU) to maximize application robustness by protecting the program code against unintended write accesses, see the application report *MSP430™ FRAM Technology – How To and Best Practices (SLAA628)*.

6.8 RAM

The RAM is made up of one sector. The sector can be completely powered down in LPM3 and LPM4 to save leakage; however, all data is lost during shutdown.

6.9 Tiny RAM

Twenty-six bytes of Tiny RAM are provided in addition to the complete RAM (see [Table 6-35](#)). This memory is always available even in LPM3 and LPM4, while the complete RAM can be powered down in LPM3 and LPM4. Tiny RAM can be used to hold data or a very small stack when the complete RAM memory is powered down in LPM3 and LPM4. Note that Tiny RAM is not available in LPMx.5.

6.10 Memory Protection Unit (MPU) Including IP Encapsulation

The FRAM can be protected by the MPU from inadvertent CPU execution and read or write access. Features of the MPU include:

- IP encapsulation with programmable boundaries (prevents reads from "outside" like JTAG or non-IP software) in steps of 1KB.
- Main memory partitioning that can be configured in up to three segments in steps of 1KB.
- The access rights for each main and information memory segment can be individually selected.
- Access violation flags with interrupt capability for easy servicing of access violations.

6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* ([SLAU367](#)).

6.11.1 Digital I/O

There are up to nine 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wakeup input capability is available for all pins of ports P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive touch functionality is supported on all pins of ports P1, P2, P3, P4, P5, P6, P7, P9, and PJ.

NOTE

Configuration of Digital I/Os After BOR Reset

To prevent any cross-currents during start-up of the device all port pins are high-impedance with Schmitt triggers and their module functions disabled. To enable the I/O functionality after a BOR reset the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details refer to the "Digital I/O" chapter, section "Configuration After Reset" in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* ([SLAU367](#)).

6.11.2 Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch-crystal oscillator XT1 (LF), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2 (HF). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external low frequency (<50kHz) clock source.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced from a high-frequency crystal (HFXT2), the internal digitally-controlled oscillator DCO, a 32-kHz watch crystal (LFXT1), the internal low-frequency oscillator (VLO), or a digital external clock source.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to MCLK.

6.11.3 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes the supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a safe level. SVS circuitry is available on the primary and core supplies.

6.11.4 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

6.11.5 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock (RTC) with the following features implemented:

- Calendar mode with leap year correction
- General-purpose counter mode

The internal calendar compensates for months with fewer than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 modes to minimize power consumption.

6.11.6 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Table 6-7. WDT_A Clocks

WDTSELx	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	LFMODOSC

6.11.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). Also included is a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.

Table 6-8. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV , System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$ /NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	

Table 6-8. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		MPUPW MPU password violation (PUC)	22h	
		CSPW CS password violation (PUC)	24h	
		MPUSEGPIFG encapsulated IP memory segment violation (PUC)	26h	
		MPUSEGIIFG information memory segment violation (PUC)	28h	
		MPUSEG1IFG segment 1 memory violation (PUC)	2Ah	
		MPUSEG2IFG segment 2 memory violation (PUC)	2Ch	
		MPUSEG3IFG segment 3 memory violation (PUC)	2Eh	
		ACCTEIFG access time error (PUC)	30h	
		Reserved	32h to 3Eh	Lowest
		SYSSNIV , System NMI	019Ch	No interrupt pending
Reserved	02h			Highest
Uncorrectable FRAM bit error detection	04h			
Reserved	06h			
MPUSEGPIFG encapsulated IP memory segment violation	08h			
MPUSEGIIFG information memory segment violation	0Ah			
MPUSEG1IFG segment 1 memory violation	0Ch			
MPUSEG2IFG segment 2 memory violation	0Eh			
MPUSEG3IFG segment 3 memory violation	10h			
VMAIFG Vacant memory access	12h			
JMBINIFG JTAG mailbox input	14h			
JMBOUTIFG JTAG mailbox output	16h			
Correctable FRAM bit error detection	18h			
Reserved	1Ah to 1Eh			Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG NMI pin	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

6.11.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 6-9. DMA Trigger Assignments ⁽¹⁾

TRIGGER	CHANNEL 0	CHANNEL 1	CHANNEL 2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2 CCR0 CCIFG	TA2 CCR0 CCIFG	TA2 CCR0 CCIFG
6	TA3 CCR0 CCIFG	TA3 CCR0 CCIFG	TA3 CCR0 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	AES Trigger 0 ⁽²⁾	AES Trigger 0 ⁽²⁾	AES Trigger 0 ⁽²⁾
12	AES Trigger 1 ⁽²⁾	AES Trigger 1 ⁽²⁾	AES Trigger 1 ⁽²⁾
13	AES Trigger 2 ⁽²⁾	AES Trigger 2 ⁽²⁾	AES Trigger 2 ⁽²⁾
14	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
15	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
16	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
17	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
18	UCB0RXIFG (SPI) UCB0RXIFG0 (I ² C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I ² C)	UCB0RXIFG (SPI) UCB0RXIFG0 (I ² C)
19	UCB0TXIFG (SPI) UCB0TXIFG0 (I ² C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I ² C)	UCB0TXIFG (SPI) UCB0TXIFG0 (I ² C)
20	UCB0RXIFG1 (I ² C)	UCB0RXIFG1 (I ² C)	UCB0RXIFG1 (I ² C)
21	UCB0TXIFG1 (I ² C)	UCB0TXIFG1 (I ² C)	UCB0TXIFG1 (I ² C)
22	UCB0RXIFG2 (I ² C)	UCB0RXIFG2 (I ² C)	UCB0RXIFG2 (I ² C)
23	UCB0TXIFG2 (I ² C)	UCB0TXIFG2 (I ² C)	UCB0TXIFG2 (I ² C)
24	UCB1RXIFG (SPI) UCB1RXIFG0 (I ² C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I ² C)	UCB1RXIFG (SPI) UCB1RXIFG0 (I ² C)
25	UCB1TXIFG (SPI) UCB1TXIFG0 (I ² C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I ² C)	UCB1TXIFG (SPI) UCB1TXIFG0 (I ² C)
26	ADC12 end of conversion ⁽³⁾	ADC12 end of conversion ⁽³⁾	ADC12 end of conversion ⁽³⁾
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

- (1) If a reserved trigger source is selected, no trigger is generated.
- (2) Only on devices with AES. Reserved on devices without AES.
- (3) Only on devices with ADC. Reserved on devices without ADC.

6.11.9 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I²C.

Two eUSCI_A modules and two eUSCI_B module are implemented.

6.11.10 Timer_A TA0, Timer_A TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. Each can support multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. Timer_A TA0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.2 or P7.0	TA0CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.2 or P7.0	$\overline{\text{TA0CLK}}$	INCLK				
P1.5	TA0.0	CCI0A	CCR0	TA0	TA0.0	P1.5
P7.1	TA0.0	CCI0B				P7.1
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
P1.0 or P1.6 or P7.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	P1.0
	COU _T (internal)	CCI1B				P1.6
	DV _{SS}	GND				P7.2
	DV _{CC}	V _{CC}				ADC12(internal) ⁽¹⁾ ADC12SHSx = {1}
P1.1 or P1.7 or P7.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	P1.1
	ACLK (internal)	CCI2B				P1.7
	DV _{SS}	GND				P7.3
	DV _{CC}	V _{CC}				

(1) Only on devices with ADC.

Table 6-11. Timer_A TA1 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P1.1 or P4.4	TA1CLK	TACLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P1.1 or P4.4	$\overline{\text{TA1CLK}}$	INCLK				
P1.4 or P4.5	TA1.0	CCI0A	CCR0	TA0	TA1.0	P1.4
	DV _{SS}	CCI0B				P4.5
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
P1.2 or P3.3 or P4.6	TA1.1	CCI1A	CCR1	TA1	TA1.1	P1.2
	COUT (internal)	CCI1B				P4.6
	DV _{SS}	GND				P3.3
	DV _{CC}	V _{CC}				ADC12(internal) ⁽¹⁾ ADC12SHSx = {4}
P1.3 or P4.7	TA1.2	CCI2A	CCR2	TA2	TA1.2	P1.3
	ACLK (internal)	CCI2B				P4.7
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				

(1) Only on devices with ADC.

6.11.11 Timer_A TA2

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers each and with internal connections only. It can support multiple capture/compares, PWM outputs, and interval timing. It has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. Timer_A TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
from Capacitive Touch I/O 0 (internal)	INCLK			
TA3 CCR0 output (internal)	CCI0A	CCR0	TA0	TA3 CCI0A input
ACLK (internal)	CCI0B			
DV _{SS}	GND			
DV _{CC}	V _{CC}			
from Capacitive Touch I/O 0 (internal)	CCI1A	CCR1	TA1	ADC12(internal) ⁽¹⁾ ADC12SHSx = {5}
COUT (internal)	CCI1B			
DV _{SS}	GND			
DV _{CC}	V _{CC}			

(1) Only on devices with ADC.

6.11.12 Timer_A TA3

TA3 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers each and with internal connections only. It can support multiple capture/compares, PWM outputs, and interval timing. It has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. Timer_A TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
COUT (internal)	TACLK	Timer	N/A	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
from Capacitive Touch I/O 1 (internal)	INCLK			
TA2 CCR0 output (internal)	CCI0A	CCR0	TA0	TA2 CCI0A input
ACLK (internal)	CCI0B			
DV _{SS}	GND			
DV _{CC}	V _{CC}			
From Capacitive Touch I/O 1 (internal)	CCI1A	CCR1	TA1	ADC12 (internal) ⁽¹⁾ ADC12SHSx = {6}
COUT (internal)	CCI1B			
DV _{SS}	GND			
DV _{CC}	V _{CC}			
P3.0 DV _{SS} (FR592x(1) 64-pin package)	CCI2B	CCR2	TA2	P3.0 (Note: Not available for FR592x(1) 64-pin package devices)
DV _{SS}	GND			
DV _{CC}	V _{CC}			
DV _{SS}	CCI2A			
P3.1 DV _{SS} (FR592x(1) 64-pin package)	CCI3B	CCR3	TA3	P3.1 (Note: Not available for FR592x(1) 64-pin package devices)
DV _{SS}	GND			
DV _{CC}	V _{CC}			
DV _{SS}	CCI3A			
P3.2 DV _{SS} (FR592x(1) 64-pin package)	CCI4B	CCR4	TA4	P3.2 (Note: Not available for FR592x(1) 64-pin package devices)
DV _{SS}	GND			
DV _{CC}	V _{CC}			
DV _{SS}	CCI4A			

(1) Only on devices with ADC.

6.11.13 Timer_B TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers each. It can support multiple capture/compares, PWM outputs, and interval timing. It has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-14. Timer_B TB0 Signal Connections

INPUT PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PORT PIN
P2.0 or P3.3 or P5.7	TB0CLK	TBCLK	Timer	N/A	N/A	
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK				
P2.0 or P3.3 or P5.7	$\overline{\text{TB0CLK}}$	INCLK	CCR0	TB0	TB0.0	
P3.4	TB0.0	CCI0A				P3.4
P6.4	TB0.0	CCI0B				P6.4
	DV _{SS}	GND				ADC12 (internal) ⁽¹⁾ ADC12SHSx = {2}
	DV _{CC}	V _{CC}				
P3.5 or P6.5	TB0.1	CCI1A	CCR1	TB1	TB0.1	P3.5
	COUT (internal)	CCI1B				P6.5
	DV _{SS}	GND				ADC12 (internal) ⁽¹⁾ ADC12SHSx = {3}
	DV _{CC}	V _{CC}				
P3.6 or P6.6	TB0.2	CCI2A	CCR2	TB2	TB0.2	P3.6
	ACLK (internal)	CCI2B				P6.6
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	DV _{SS}	CCI3A	CCR3	TB3	TB0.3	
P3.7	TB0.3	CCI3B				P3.7
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	DV _{SS}	CCI4A	CCR4	TB4	TB0.4	
P2.2	TB0.4	CCI4B				P2.2
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	DV _{SS}	CCI5A	CCR5	TB5	TB0.5	
P2.1	TB0.5	CCI5B				P2.1
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				
	DV _{SS}	CCI6A	CCR6	TB6	TB0.6	
P2.0	TB0.6	CCI6B				P2.0
	DV _{SS}	GND				
	DV _{CC}	V _{CC}				

(1) Only on devices with ADC.

6.11.14 ADC12_B

The ADC12_B module supports fast 12-bit analog-to-digital conversions with differential and single-ended inputs. The module implements a 12-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

Table 6-15 summarizes the available external trigger sources.

Table 6-16 lists the available multiplexing between internal and external analog inputs.

Table 6-15. ADC12_B Trigger Signal Connections

ADC12SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC12SC)
001	1	Timer_A TA0 CCR1 output
010	2	Timer_B TB0 CCR0 output
011	3	Timer_B TB0 CCR1 output
100	4	Timer_A TA1 CCR1 output
101	5	Timer_A TA2 CCR1 output
110	6	Timer_A TA3 CCR1 output
111	7	Reserved (DVSS)

Table 6-16. ADC12_B External and Internal Signal Mapping

CONTROL BIT	EXTERNAL (CONTROL BIT = 0)	INTERNAL (CONTROL BIT = 1)
ADC12BATMAP	A31	Battery monitor
ADC12TCMAP	A30	Temperature sensor
ADC12CH0MAP	A29	N/A ⁽¹⁾
ADC12CH1MAP	A28	N/A ⁽¹⁾
ADC12CH2MAP	A27	N/A ⁽¹⁾
ADC12CH3MAP	A26	N/A ⁽¹⁾

(1) N/A: No internal signal available on this device.

6.11.15 Comparator_E

The primary function of the Comparator_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.11.16 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 signature is based on the CRC-CCITT standard.

6.11.17 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC32 signature is based on the ISO 3309 standard.

6.11.18 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-bit, 192-bit, or 256-bit keys according to the advanced encryption standard (AES) (FIPS PUB 197) in hardware.

6.11.19 True Random Seed

The Device Descriptor Info (TLV) (see [Section 6.12](#)) contains a 128-bit true random seed that can be used to implement a deterministic random-number generator.

6.11.20 Shared Reference (REF_A)

The REF_A module is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

6.11.21 Embedded Emulation

6.11.21.1 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.11.21.2 EnergyTrace++™ Technology

The devices implement circuitry to support EnergyTrace++ technology. The EnergyTrace++ technology allows you to observe information about the internal states of the microcontroller. These states include the CPU Program Counter (PC), the ON or OFF status of the peripherals and the system clocks (regardless of the clock source), and the low-power mode currently in use. These states can always be read by a debug tool, even when the microcontroller sleeps in LPMx.5 modes.

The activity of the following modules can be observed:

- MPY is calculating.
- WDT is counting.
- RTC is counting.
- ADC: a sequence, sample, or conversion is active.
- REF: REF_BG or REF_GEN active and BG in static mode.
- COMP is on.
- AES is encrypting or decrypting.
- eUSCI_A0 is transferring (receiving or transmitting) data.
- eUSCI_A1 is transferring (receiving or transmitting) data.
- eUSCI_B0 is transferring (receiving or transmitting) data.
- eUSCI_B1 is transferring (receiving or transmitting) data.
- TB0 is counting.
- TA0 is counting.
- TA1 is counting.
- TA2 is counting.
- TA3 is counting.

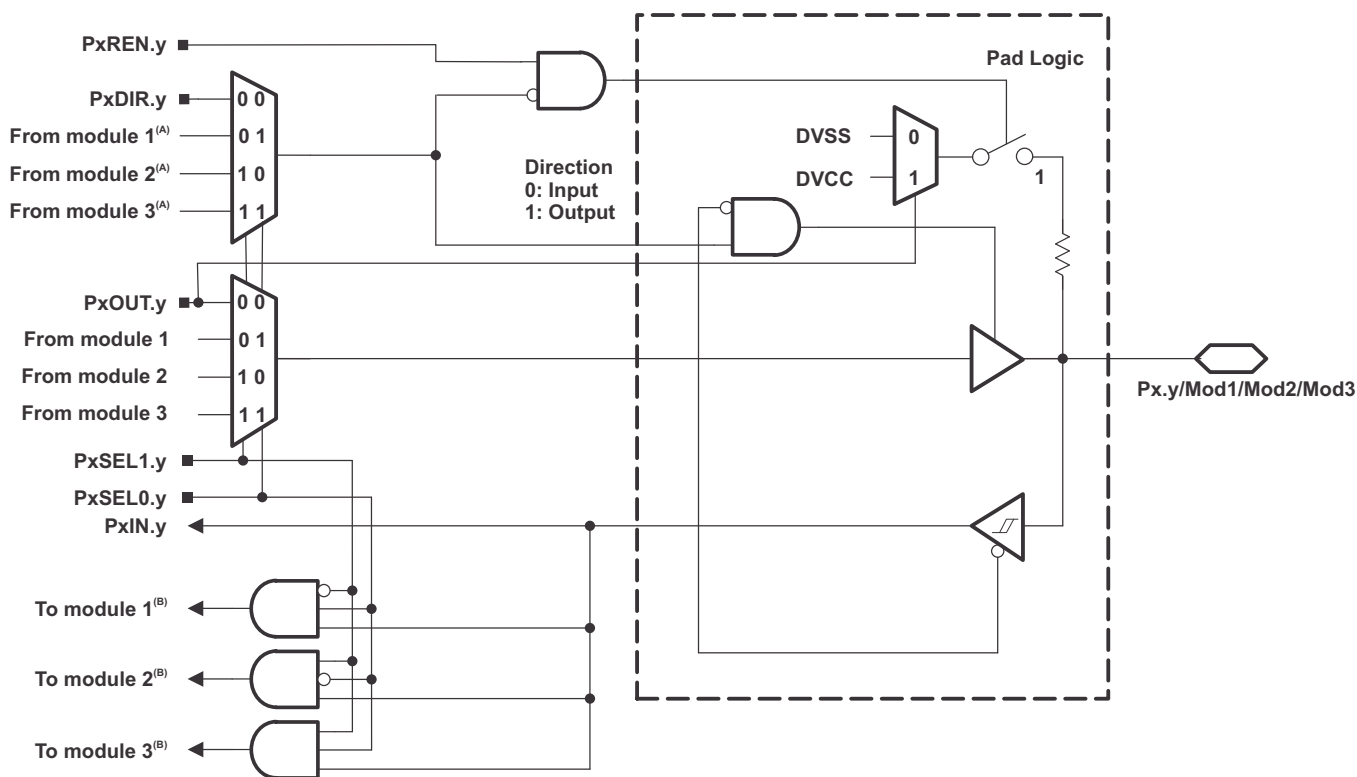
6.11.22 Input/Output Schematics

6.11.22.1 Digital I/O Functionality Port P1, P2, P3, P4, P5, P6, P7, and P9

The port pins provide the following features:

- Interrupt and wake-up from LPMx.5 capability for ports P1, P2, P3, and P4
- Capacitive touch functionality (see Section 6.11.22.2)
- Up to three digital module input and/or output functions

The features and the corresponding control logic (besides the Capacitive Touch logic) is shown in Figure 6-1. It is applicable for all port pins P1.0 through P9.7, unless a dedicated schematic is available in the following sections. The module functions provided per pin and whether the direction is controlled by the module or by the port direction register for the selected secondary function are described in the following pin function tables.



- A. The direction is either controlled by connected module or by the corresponding PxDIR.y bit. Refer to pin function tables.
- B. The inputs from several pins towards a module are ORed together. Functional representation only.

Figure 6-1. General Port Pin Schematic

6.11.22.2 Capacitive Touch Functionality Port P1, P2, P3, P4, P5, P6, P7, P9, and PJ

All port pins provide the capacitive touch functionality as shown in Figure 6-2. The capacitive touch functionality is controlled using the capacitive touch I/O control registers CAPTIO0CTL and CAPTIO1CTL as described in the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide (SLAU367)*. The capacitive touch functionality is not shown in the other pin schematics.

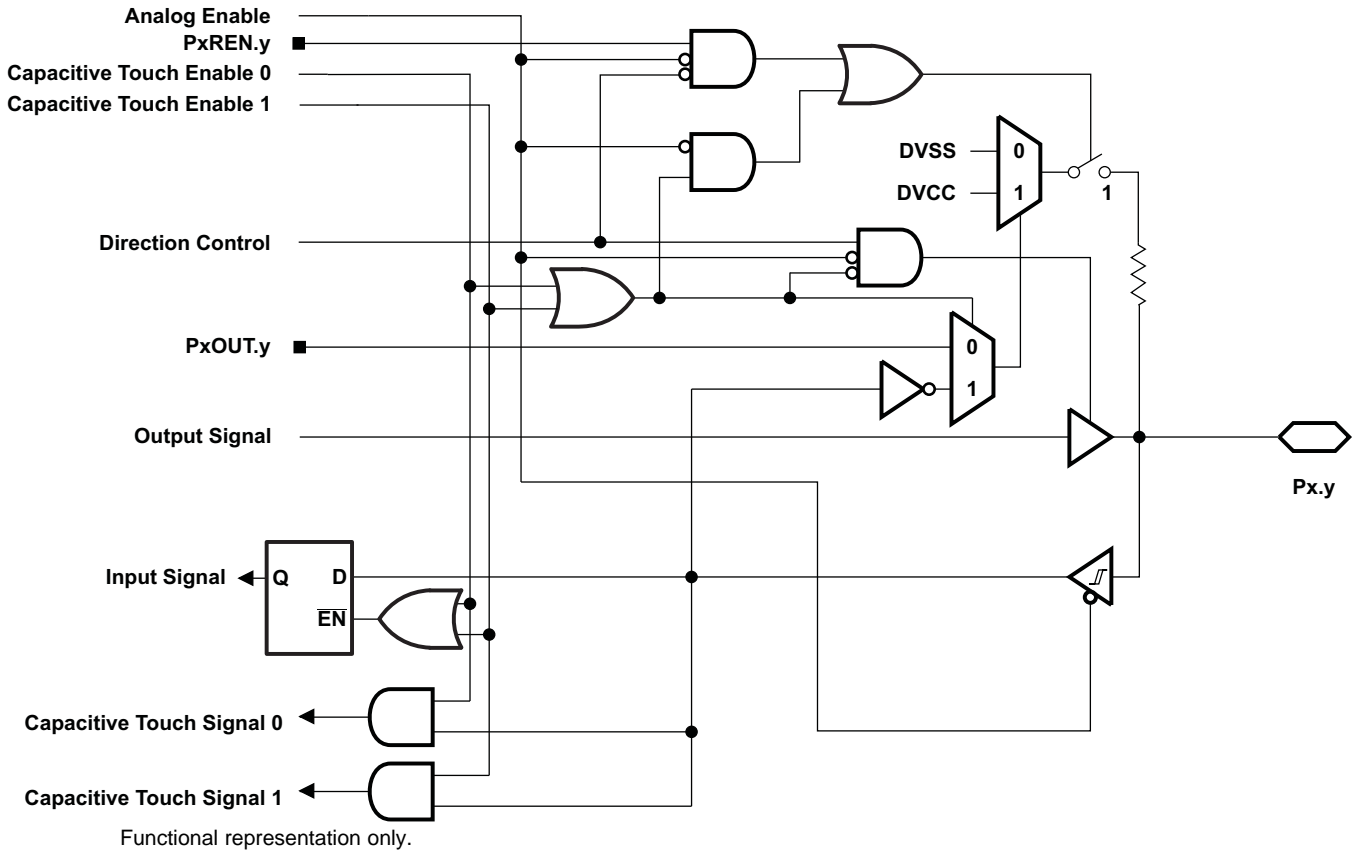


Figure 6-2. Capacitive Touch I/O Functionality

6.11.22.3 Port P1, P1.0 to P1.3, Input/Output With Schmitt Trigger

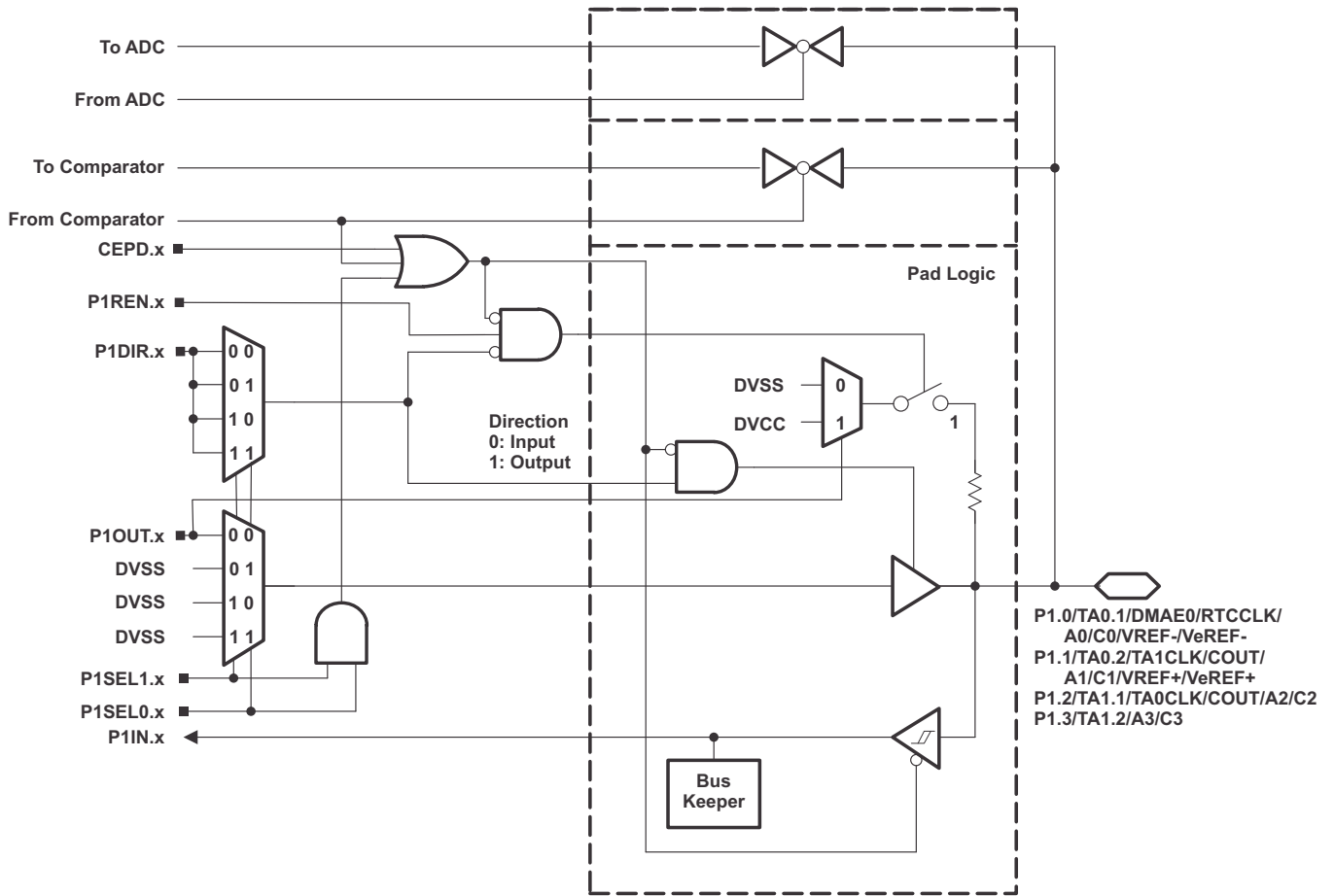


Table 6-17. Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/TA0.1/DMAE0/RTCCLK/A0/C0/ VREF-/VeREF-	0	P1.0 (I/O)	I: 0; O: 1	0	0
		TA0.CCI1A	0	0	1
		TA0.1	1		
		DMAE0	0	1	0
		RTCCLK ⁽²⁾	1		
		A0, C0, VREF-, VeREF- ^{(3) (4)}	X	1	1
P1.1/TA0.2/TA1CLK/COU/A1/C1/ VREF+/VeREF+	1	P1.1 (I/O)	I: 0; O: 1	0	0
		TA0.CCI2A	0	0	1
		TA0.2	1		
		TA1CLK	0	1	0
		COU ⁽⁵⁾	1		
		A1, C1, VREF+, VeREF+ ^{(3) (4)}	X	1	1
P1.2/TA1.1/TA0CLK/COU/A2/C2	2	P1.2 (I/O)	I: 0; O: 1	0	0
		TA1.CCI1A	0	0	1
		TA1.1	1		
		TA0CLK	0	1	0
		COU ⁽⁵⁾	1		
		A2, C2 ^{(3) (4)}	X	1	1
P1.3/TA1.2/A3/C3	3	P1.3 (I/O)	I: 0; O: 1	0	0
		TA1.CCI2A	0	0	1
		TA1.2	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A3, C3 ^{(3) (4)}	X	1	1

- (1) X = Don't care
- (2) **NOTE:** Do **not** use this pin as RTCCLK output if the DMAE0 functionality is used on any other pin. Select an alternative RTCCLK output pin.
- (3) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (4) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.
- (5) **NOTE:** Do **not** use this pin as COU output if the TA1CLK functionality is used on any other pin. Select an alternative COU output pin.

6.11.22.4 Port P1, P1.4 to P1.7, Input/Output With Schmitt Trigger

 Pin Schematic: see [Figure 6-1](#).

Table 6-18. Port P1 (P1.4 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.4/UCB0CLK/UCA0STE/TA1.0	4	P1.4 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	X ⁽²⁾	0	1
		UCA0STE	X ⁽³⁾	1	0
		TA1.CCI0A	0	1	1
		TA1.0	1		
P1.5/UCB0STE/UCA0CLK/TA0.0	5	P1.5 (I/O)	I: 0; O: 1	0	0
		UCB0STE	X ⁽²⁾	0	1
		UCA0CLK	X ⁽³⁾	1	0
		TA0.CCI0A	0	1	1
		TA0.0	1		
P1.6/UCB0SIMO/UCB0SDA/TA0.1	6	P1.6 (I/O)	I: 0; O: 1	0	0
		UCB0SIMO/UCB0SDA	X ⁽²⁾	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		TA0.CCI1A	0	1	1
		TA0.1	1		
P1.7/UCB0SOMI/UCB0SCL/TA0.2	7	P1.7 (I/O)	I: 0; O: 1	0	0
		UCB0SOMI/UCB0SCL	X ⁽²⁾	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		TA0.CCI2A	0	1	1
		TA0.2	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_B0 module.

(3) Direction controlled by eUSCI_A0 module.

6.11.22.5 Port P2, P2.0 to P2.3, Input/Output With Schmitt Trigger

Pin Schematic: see [Figure 6-1](#).

Table 6-19. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P2DIR.x	P2SEL1.x	P2SEL0.x
P2.0/UCA0SIMO/UCA0TXD/TB0.6/ TB0CLK	0	P2.0 (I/O)	I: 0; O: 1	0	0
		UCA0SIMO/UCA0TXD	X ⁽²⁾	0	1
		TB0.CCI6B	0	1	0
		TB0.6	1		
		TB0CLK	0	1	1
		Internally tied to DVSS	1		
P2.1/UCA0SOMI/UCA0RXD/TB0.5/ DMA0E	1	P2.1 (I/O)	I: 0; O: 1	0	0
		UCA0SOMI/UCA0RXD	X ⁽²⁾	0	1
		TB0.CCI5B	0	1	0
		TB0.5	1		
		DMA0E	0	1	1
		Internally tied to DVSS	1		
P2.2/UCA0CLK/TB0.4/RTCCLK	2	P2.2 (I/O)	I: 0; O: 1	0	0
		UCA0CLK	X ⁽²⁾	0	1
		TB0.CCI4B	0	1	0
		TB0.4	1		
		N/A	0	1	1
		RTCCLK	1		
P2.3/UCA0STE/TB0OUTH	3	P2.3 (I/O)	I: 0; O: 1	0	0
		UCA0STE	X ⁽²⁾	0	1
		TB0OUTH	0	1	0
		Internally tied to DVSS	1		
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_A0 module.

6.11.22.6 Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

 Pin Schematic: see [Figure 6-1](#).

Table 6-20. Port P3 (P3.0 to P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.0/UCB1CLK	0	P3.0 (I/O)	I: 0; O: 1	0	0
		UCB1CLK	X ⁽²⁾	0	1
		TA3.CCI2B (Note: not available for FR592x(1) 64-pin package devices)	0	1	0
		TA3.2 Internally tied to DVSS (for FR292x(1) 64-pin package devices)	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P3.1/UCB1SIMO/UCB1SDA	1	P3.1 (I/O)	I: 0; O: 1	0	0
		UCB1SIMO/UCB1SDA	X ⁽²⁾	0	1
		TA3.CCI3B (Note: not available for FR592x(1) 64-pin package devices)	0	1	0
		TA3.3 Internally tied to DVSS (for FR592x(1) 64-pin package devices)	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P3.2/UCB1SOMI/UCB1SCL	2	P3.2 (I/O)	I: 0; O: 1	0	0
		UCB1SOMI/UCB1SCL	X ⁽²⁾	0	1
		TA3.CCI4B (Note: not available for FR592x(1) 64-pin package devices)	0	1	0
		TA3.4 Internally tied to DVSS (for FR592x(1) 64-pin package devices)	1		
			0	1	1
			1		
P3.3/TA1.1/TB0CLK	3	P3.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		TA1.CCI1A	0	1	0
		TA1.1	1		
		TB0CLK	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_B1 module.

Table 6-21. Port P3 (P3.4 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P3DIR.x	P3SEL1.x	P3SEL0.x
P3.4/UCA1SIMO/UCA1TXD/TB0.0	4	P3.4 (I/O)	I: 0; O: 1	0	0
		UCA1SIMO/UCA1TXD	X ⁽²⁾	0	1
		TB0CCI0A	0	1	0
		TB0.0	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P3.5/UCA1SOMI/UCA1RXD/TB0.1	5	P3.5 (I/O)	I: 0; O: 1	0	0
		UCA1SOMI/UCA1RXD	X ⁽²⁾	0	1
		TB0CCI1A	0	1	0
		TB0.1	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P3.6/UCA1CLK/TB0.2	6	P3.6 (I/O)	I: 0; O: 1	0	0
		UCA1CLK	X ⁽²⁾	0	1
		TB0CCI2A	0	1	0
		TB0.2	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P3.7/UCA1STE/TB0.3	7	P3.7 (I/O)	I: 0; O: 1	0	0
		UCA1STE	X ⁽²⁾	0	1
		TB0CCI3B	0	1	0
		TB0.3	1		
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_A1 module.

6.11.22.7 Port P4, P4.2 to P4.7, Input/Output With Schmitt Trigger

 Pin Schematic: see [Figure 6-1](#).

Table 6-22. Port P4 (P4.2 to P4.3) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.2/UCA0SIMO/UCA0TXD/UCB1CLK	2	P4.2 (I/O)	I: 0; O: 1	0	0
		UCA0SIMO/UCA0TXD	X ⁽²⁾	0	1
		UCB1CLK	X ⁽³⁾	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		
P4.3/UCA0SOMI/UCA0RXD/UCB1STE	3	P4.3 (I/O)	I: 0; O: 1	0	0
		UCA0SOMI/UCA0RXD	X ⁽²⁾	0	1
		UCB1STE	X ⁽³⁾	1	0
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_A0 module.

(3) Direction controlled by eUSCI_B1 module.

Table 6-23. Port P4 (P4.4 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.4/UCB1STE/TA1CLK	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCB1STE	X ⁽²⁾	1	0
		TA1CLK	0	1	1
		Internally tied to DVSS	1		
P4.5/UCB1CLK/TA1.0	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCB1CLK	X ⁽²⁾	1	0
		TA1CCI0A	0	1	1
		TA1.0	1		
P4.6/UCB1SIMO/UCB1SDA/TA1.1	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCB1SIMO/UCB1SDA	X ⁽²⁾	1	0
		TA1CCI1A	0	1	1
		TA1.1	1		
P4.7/UCB1SOMI/UCB1SCL/TA1.2	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		UCB1SOMI/UCB1SCL	X ⁽²⁾	1	0
		TA1CCI2A	0	1	1
		TA1.2	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_B1 module.

6.11.22.8 Port P5, P5.4 to P5.7, Input/Output With Schmitt Trigger

 Pin Schematic: see [Figure 6-1](#).

Table 6-24. Port P5 (P5.4 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.4/UCA1SIMO/UCA1TXD	4	P5.4 (I/O)	I: 0; O: 1	0	0
		UCA1SIMO/UCA1TXD	X ⁽²⁾	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P5.5/UCA1SOMI/UCA1RXD	5	P5.5 (I/O)	I: 0; O: 1	0	0
		UCA1SOMI/UCA1RXD	X ⁽²⁾	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P5.6/UCA1CLK	6	P5.6 (I/O)	I: 0; O: 1	0	0
		UCA1CLK	X ⁽²⁾	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
P5.7/UCA1STE/TB0CLK	7	P5.7 (I/O)	I: 0; O: 1	0	0
		UCA1STE	X ⁽²⁾	0	1
		N/A	0	1	0
		Internally tied to DVSS	1		
		TB0CLK	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care

(2) Direction controlled by eUSCI_A1 module.

6.11.22.9 Port P6, P6.0 to P6.6, Input/Output With Schmitt Trigger

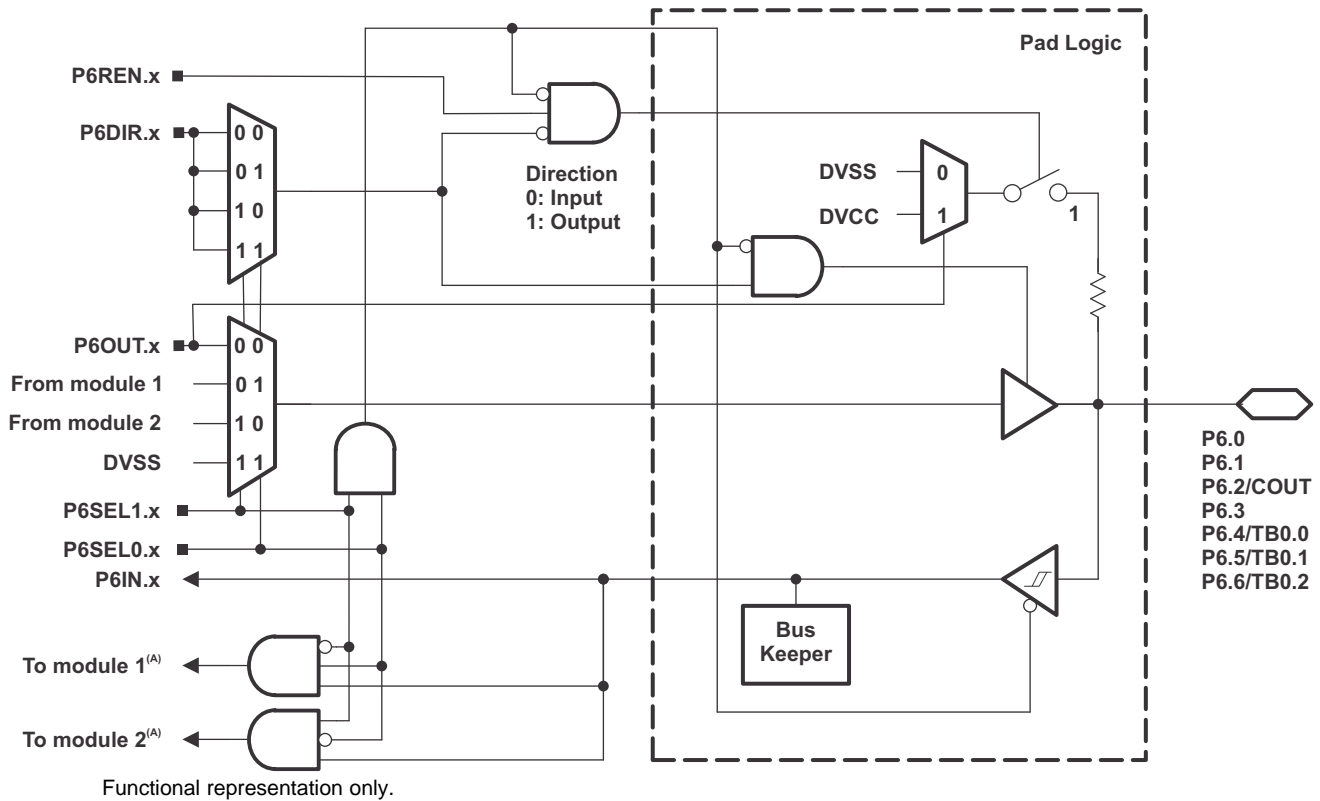


Table 6-25. Port P6 (P6.0 to P6.2) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.0	0	P6.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1
P6.1	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1
P6.2/COUT	2	P6.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		COUT	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1

(1) X = Don't care

Table 6-26. Port P6 (P6.3 to P6.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.3	3	P6.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1
P6.4/TB0.0	4	P6.4 (I/O)	I: 0; O: 1	0	0
		TB0CCI0B	0	0	1
		TB0.0	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1
P6.5/TB0.1	5	P6.5 (I/O)	I: 0; O: 1	0	0
		TB0CCI1A	0	0	1
		TB0.1	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1
P6.6/TB0.2	6	P6.6 (I/O)	I: 0; O: 1	0	0
		TB0CCI2A	0	0	1
		TB0.2	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	X	1	1

(1) X = Don't care

6.11.22.10 Port P7, P7.0 to P7.4, Input/Output With Schmitt Trigger

 Pin Schematic: see [Figure 6-1](#).

Table 6-27. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P7DIR.x	P7SEL1.x	P7SEL0.x
P7.0/TA0CLK	0	P7.0 (I/O)	I: 0; O: 1	0	0
		TA0CLK	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0		
		Internally tied to DVSS	1	1	1
P7.1/TA0.0	1	P7.1 (I/O)	I: 0; O: 1	0	0
		TA0CCI0B	0	0	1
		TA0.0	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0		
		ACLK	1	1	1
P7.2/TA0.1	2	P7.2 (I/O)	I: 0; O: 1	0	0
		TA0CCI1A	0	0	1
		TA0.1	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0		
		N/A	1	1	1
P7.3/TA0.2	3	P7.3 (I/O)	I: 0; O: 1	0	0
		TA0CCI2A	0	0	1
		TA0.2	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0		
		Internally tied to DVSS	1	1	1

(1) X = Don't care

Table 6-28. Port P7 (P7.4) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P7DIR.x	P7SEL1.x	P7SEL0.x
P7.4/SMCLK	4	P7.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		N/A	0		
		SMCLK	1	1	1

(1) X = Don't care

6.11.22.11 Port P9, P9.4 to P9.7, Input/Output With Schmitt Trigger

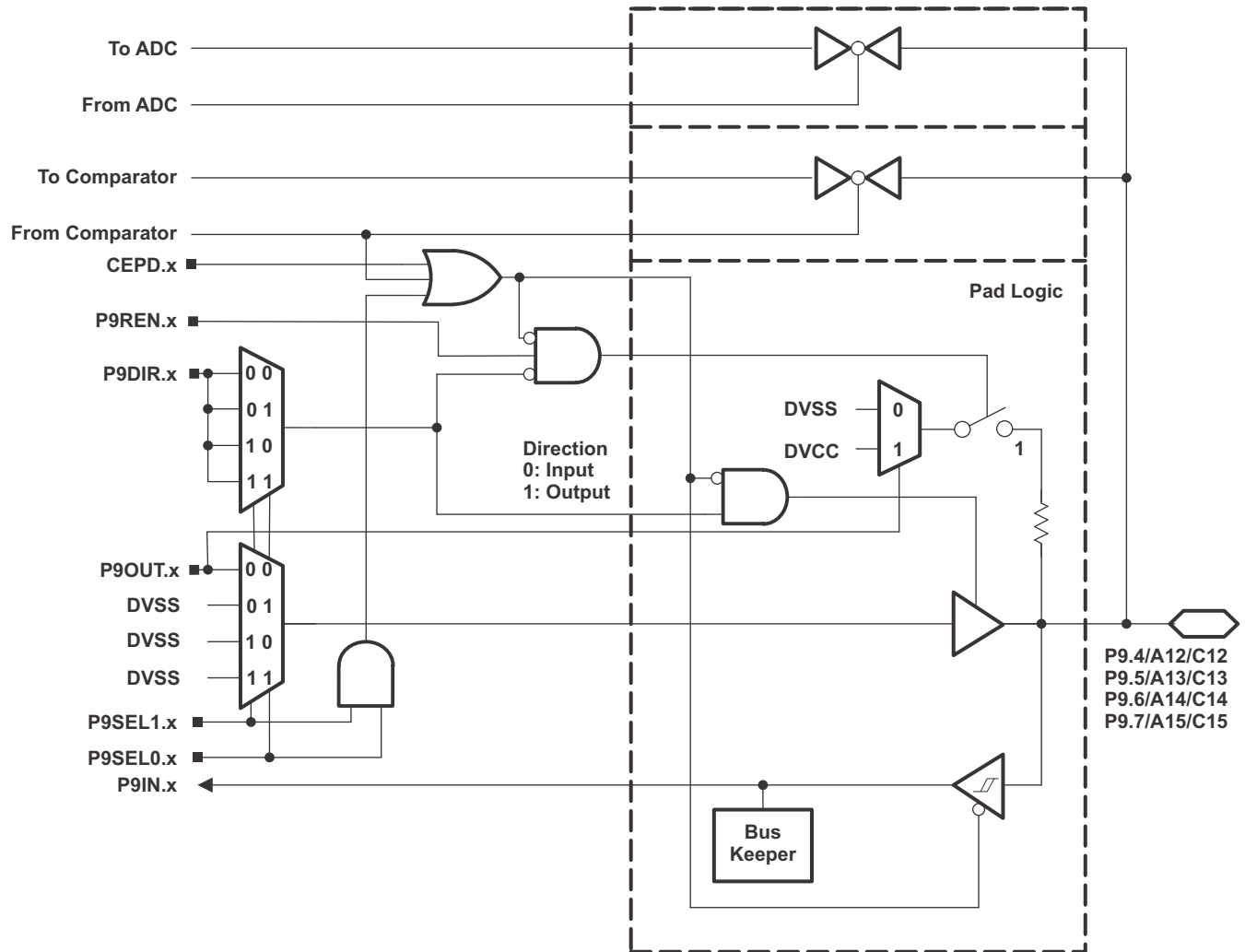


Table 6-29. Port P9 (P9.4 to P9.7) Pin Functions

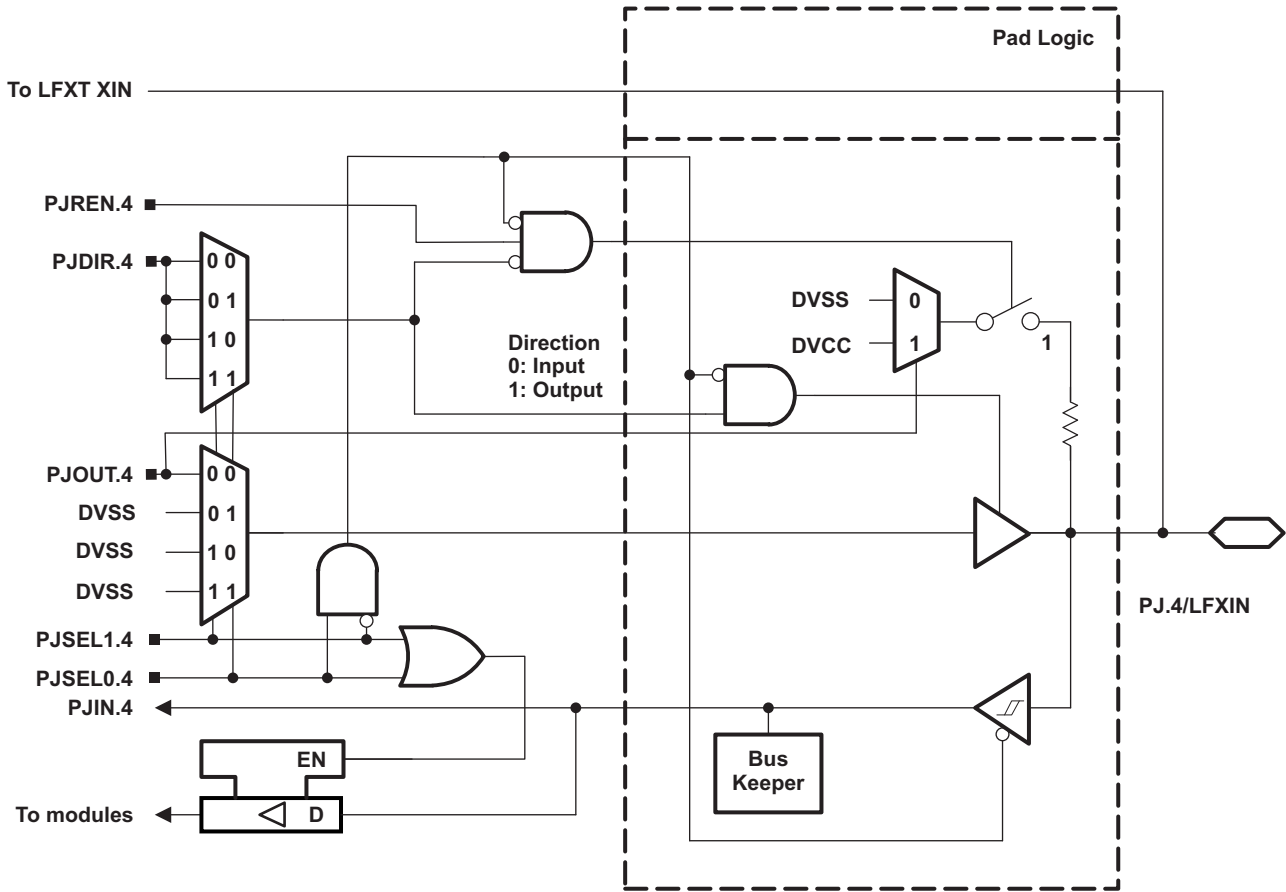
PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.4/A12/C12	4	P9.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A12/C12 ^{(2) (3)}	X		
P9.5/A13/C13	5	P9.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A13/C13 ^{(2) (3)}	X		
P9.6/A14/C14	6	P9.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A14/C14 ^{(2) (3)}	X		
P9.7/A15/C15	7	P9.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		Internally tied to DVSS	1		
		N/A	0	1	0
		Internally tied to DVSS	1		
		A15/C15 ^{(2) (3)}	X		

(1) X = Don't care

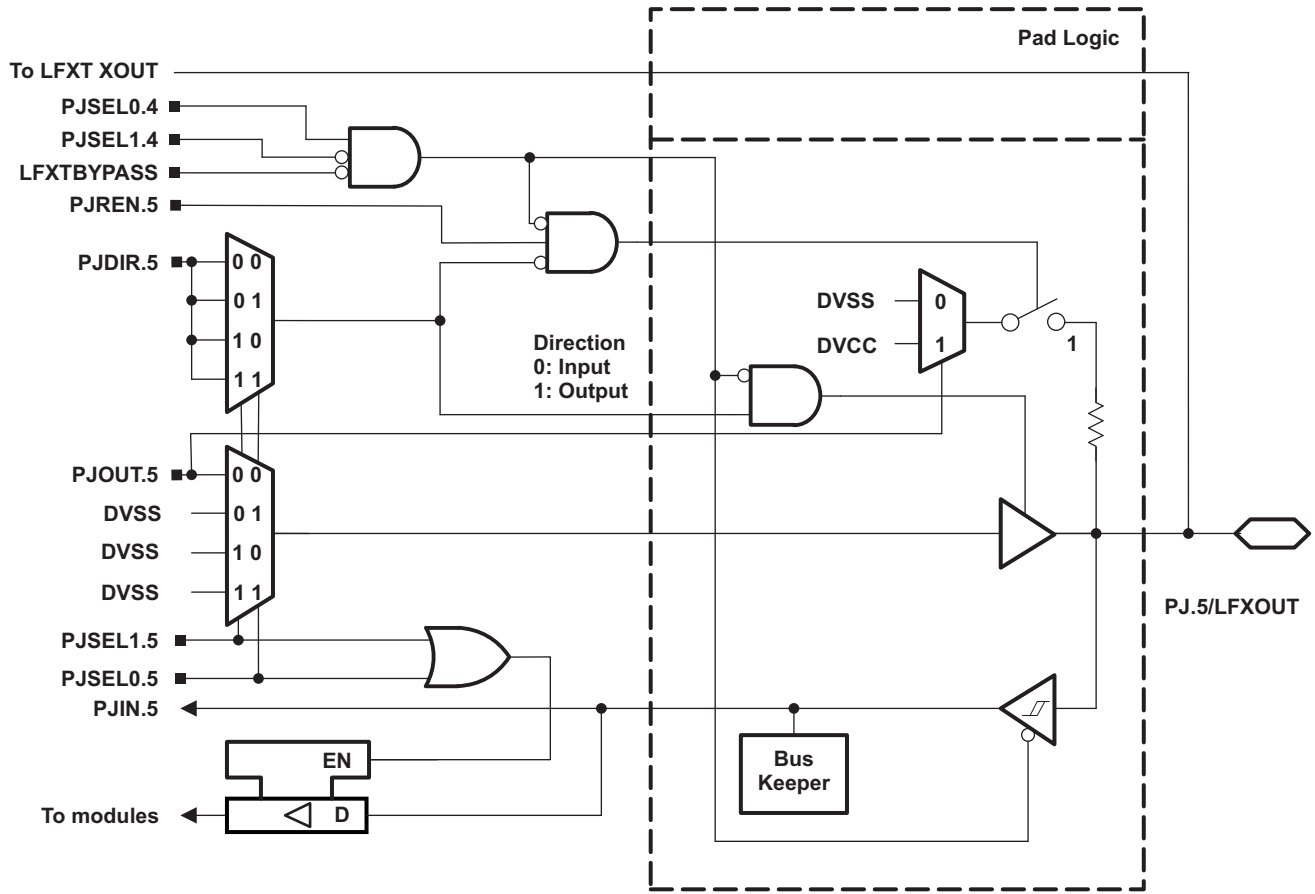
(2) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(3) Setting the CEPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the Cx input pin to the comparator multiplexer with the input select bits in the comparator module automatically disables output driver and input buffer for that pin, regardless of the state of the associated CEPD.x bit.

6.11.22.12 Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger



Functional representation only.



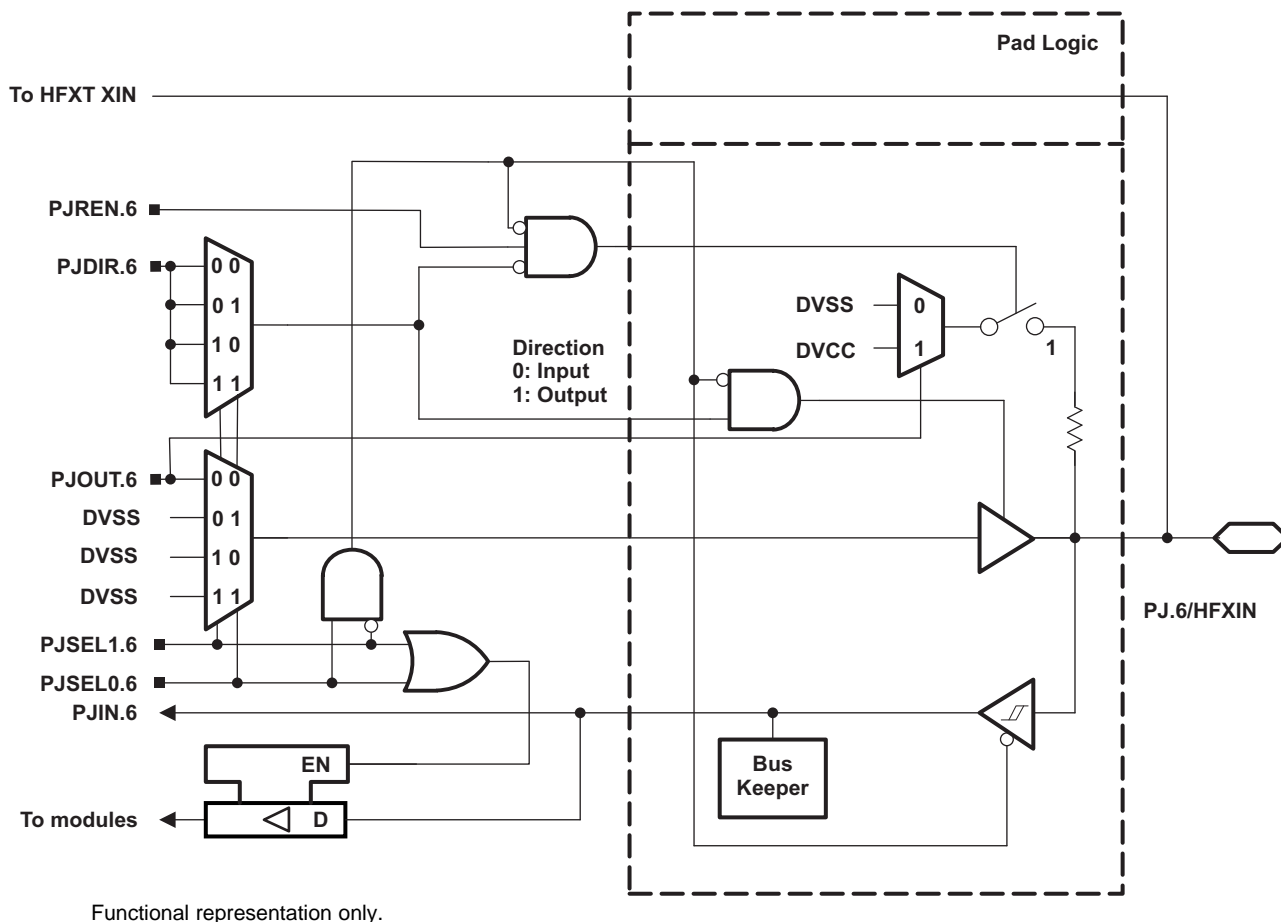
Functional representation only.

Table 6-30. Port PJ (PJ.4 and PJ.5) Pin Functions

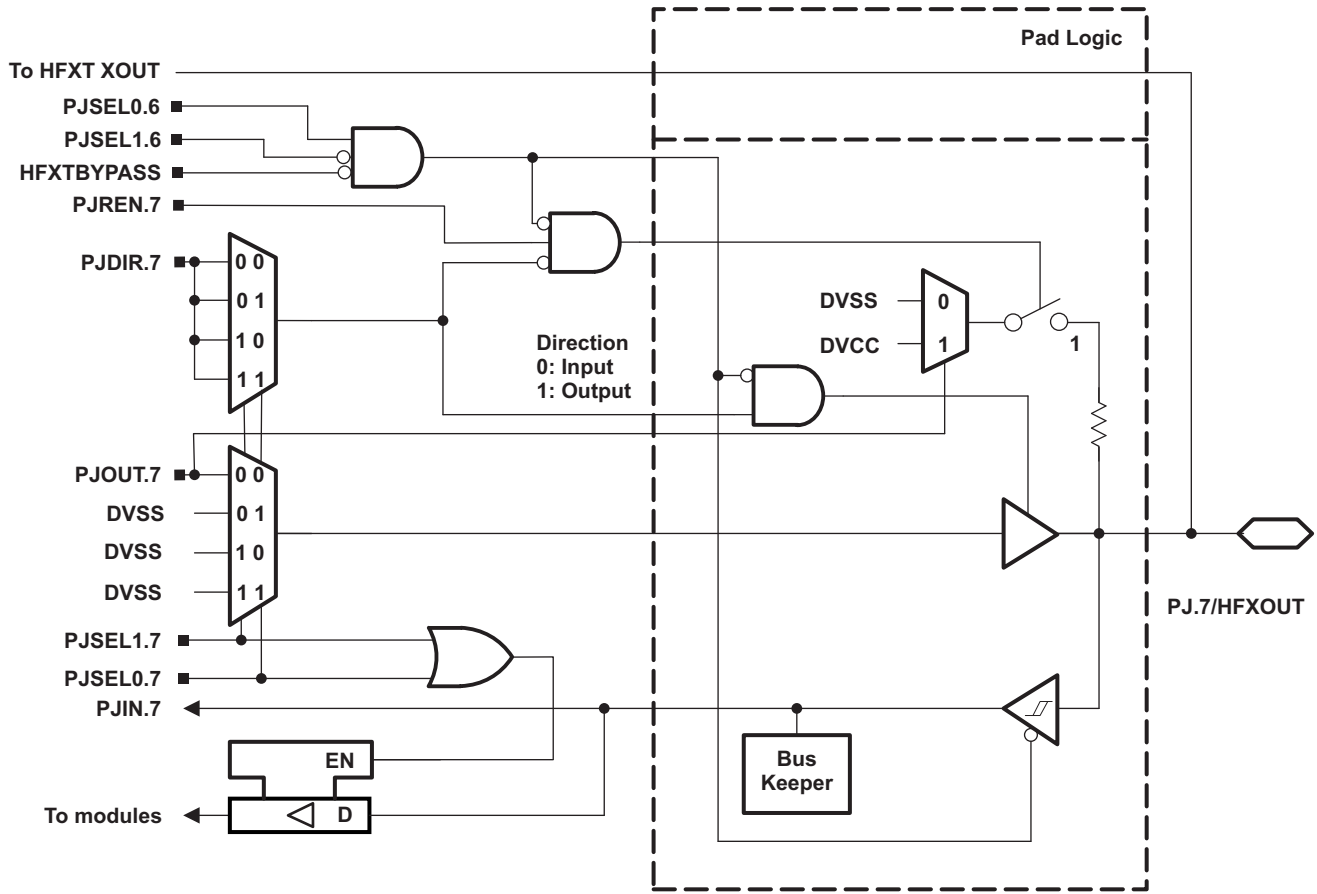
PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾					
			PJDIR.x	PJSEL1.5	PJSEL0.5	PJSEL1.4	PJSEL0.4	LFXTBYPASS
PJ.4/LFXIN	4	PJ.4 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		LFXIN crystal mode ⁽²⁾	X	X	X	0	1	0
		LFXIN bypass mode ⁽²⁾	X	X	X	0	1	1
PJ.5/LFXOUT	5	PJ.5 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 ⁽³⁾
		N/A	0	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
						1	X	
						X	X	1 ⁽³⁾
		Internally tied to DVSS	1	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
						1	X	
						X	X	1 ⁽³⁾
		LFXOUT crystal mode ⁽²⁾	X	X	X	0	1	0

- (1) X = Don't care
- (2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are do not care. When LFXTBYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
- (3) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.
- (4) With PJSEL0.5 = 1 or PJSEL1.5 = 1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

6.11.22.13 Port PJ, PJ.6 and PJ.7 Input/Output With Schmitt Trigger



Functional representation only.



Functional representation only.

Table 6-31. Port PJ (PJ.6 and PJ.7) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾					
			PJDIR.x	PJSEL1.7	PJSEL0.7	PJSEL1.6	PJSEL0.6	HFXTBYPASS
PJ.6/HFXIN	6	PJ.6 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		Internally tied to DVSS	1					
		HFXIN crystal mode ⁽²⁾	X	X	X	0	1	0
		HFXIN bypass mode ⁽²⁾	X	X	X	0	1	1
PJ.7/HFXOUT	7	PJ.7 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	
		N/A	0	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
						1	X	
						X	X	
		Internally tied to DVSS	1	see ⁽⁴⁾	see ⁽⁴⁾	0	0	0
						1	X	
X	X					1 ⁽³⁾		
HFXOUT crystal mode ⁽²⁾	X	X	X	0	1	0		

(1) X = Don't care

(2) Setting PJSEL1.6 = 0 and PJSEL0.6 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.6 and PJ.7 are configured for crystal operation and PJSEL1.6 and PJSEL0.7 are do not care. When HFXTBYPASS = 1, PJ.6 is configured for bypass operation and PJ.7 is configured as general-purpose I/O.

(3) When PJ.6 is configured in bypass mode, PJ.7 is configured as general-purpose I/O.

(4) With PJSEL0.7 = 1 or PJSEL1.7 = 1 the general-purpose I/O functionality is disabled. No input function is available. Configured as output, the pin is actively pulled to zero.

6.11.22.14 Port J, J.0 to J.3 JTAG pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger

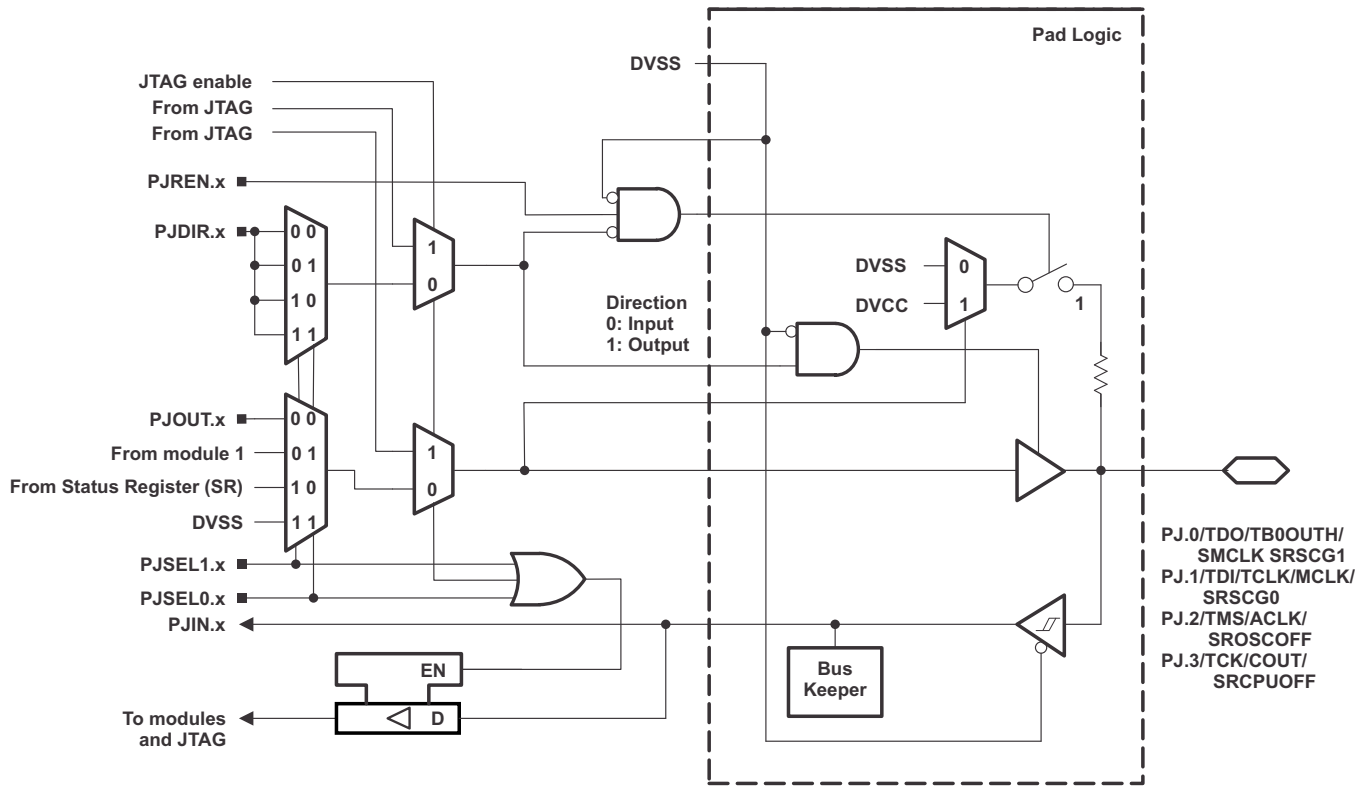


Table 6-32. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			PJDIR.x	PJSEL1.x	PJSEL0.x
PJ.0/TDO/TB0OUTH/ SMCLK/SRSCG1	0	PJ.0 (I/O) ⁽²⁾	I: 0; O: 1	0	0
		TDO ⁽³⁾	X	X	X
		TB0OUTH	0	0	1
		SMCLK ⁽⁴⁾	1		
		N/A	0	1	0
		CPU Status Register Bit SCG1	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
PJ.1/TDI/TCLK/MCLK/ SRSCG0	1	PJ.1 (I/O) ⁽²⁾	I: 0; O: 1	0	0
		TDI/TCLK ^{(3) (5)}	X	X	X
		N/A	0	0	1
		MCLK	1		
		N/A	0	1	0
		CPU Status Register Bit SCG0	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
PJ.2/TMS/ACLK/ SROSCOFF	2	PJ.2 (I/O) ⁽²⁾	I: 0; O: 1	0	0
		TMS ^{(3) (5)}	X	X	X
		N/A	0	0	1
		ACLK	1		
		N/A	0	1	0
		CPU Status Register Bit OSCOFF	1		
		N/A	0	1	1
		Internally tied to DVSS	1		
PJ.3/TCK/COUT/ SRCPUOFF	3	PJ.3 (I/O) ⁽²⁾	I: 0; O: 1	0	0
		TCK ^{(3) (5)}	X	X	X
		N/A	0	0	1
		COUT	1		
		N/A	0	1	0
		CPU Status Register Bit CPUOFF	1		
		N/A	0	1	1
		Internally tied to DVSS	1		

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made via the SYS module or by the SpyBiWire four wire entry sequence. Neither PJSEL1.x and PJSEL0.x nor CEPD.x bits have an effect in these cases.

(4) **NOTE:** Do **not** use this pin as SMCLK output if the TB0OUTH functionality is used on any other pin. Select an alternative SMCLK output pin.

(5) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

6.12 Device Descriptors (TLV)

Table 6-34 list the contents of the device descriptor tag-length-value (TLV) structure. Table 6-33 summarizes the Device IDs.

Table 6-33. Device ID

DEVICE	PACKAGE	DEVICE ID	
		At 01A05h	At 01A04h
MSP430FR5970	PM and RGC	82h	5Bh
MSP430FR5972(1)	PM and RGC	82h	5Dh
MSP430FR5922(1)	PM and RGC	82h	61h
	DGG	82h	62h
MSP430FR5870	PM and RGC	82h	5Eh
MSP430FR5872(1)	PM and RGC	82h	60h

Table 6-34. Device Descriptor Table ⁽¹⁾

	DESCRIPTION	MSP430FRxxxx (UART BSL)		MSP430FRxxxx1 (I ² C BSL)	
		ADDRESS	VALUE	ADDRESS	VALUE
Info Block	Info length	01A00h	06h	01A00h	06h
	CRC length	01A01h	06h	01A01h	06h
	CRC value	01A02h	per unit	01A02h	per unit
		01A03h	per unit	01A03h	per unit
	Device ID	01A04h	see Table 6-33	01A04h	see Table 6-33
	Device ID	01A05h		01A05h	
	Hardware revision	01A06h	per unit	01A06h	per unit
	Firmware revision	01A07h	per unit	01A07h	per unit
Die Record	Die Record Tag	01A08h	08h	01A08h	08h
	Die Record length	01A09h	0Ah	01A09h	0Ah
	Lot/Wafer ID	01A0Ah	per unit	01A0Ah	per unit
		01A0Bh	per unit	01A0Bh	per unit
		01A0Ch	per unit	01A0Ch	per unit
		01A0Dh	per unit	01A0Dh	per unit
	Die X position	01A0Eh	per unit	01A0Eh	per unit
		01A0Fh	per unit	01A0Fh	per unit
	Die Y position	01A10h	per unit	01A10h	per unit
		01A11h	per unit	01A11h	per unit
	Test results	01A12h	per unit	01A12h	per unit
		01A13h	per unit	01A13h	per unit
ADC12B Calibration	ADC12B Calibration Tag	01A14h	11h	01A14h	11h
	ADC12B Calibration length	01A15h	10h	01A15h	10h
	ADC Gain Factor ⁽²⁾	01A16h	per unit	01A16h	per unit
		01A17h	per unit	01A17h	per unit
	ADC Offset ⁽³⁾	01A18h	per unit	01A18h	per unit
		01A19h	per unit	01A19h	per unit

(1) NA = Not applicable

per unit = content can differ from device to device

(2) ADC Gain: The gain correction factor is measured using the internal voltage reference with REFOUT = 0. Other settings (for example, with REFOUT = 1) can result in different correction factors.

(3) ADC Offset: The offset correction factor is measured using the internal 2.5-V reference.

Table 6-34. Device Descriptor Table ⁽¹⁾ (continued)

	DESCRIPTION	MSP430FRxxxx (UART BSL)		MSP430FRxxxx1 (I ² C BSL)		
		ADDRESS	VALUE	ADDRESS	VALUE	
	ADC 1.2-V Reference Temp. Sensor 30°C	01A1Ah	per unit	01A1Ah	per unit	
		01A1Bh	per unit	01A1Bh	per unit	
	ADC 1.2-V Reference Temp. Sensor 85°C	01A1Ch	per unit	01A1Ch	per unit	
		01A1Dh	per unit	01A1Dh	per unit	
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	per unit	01A1Eh	per unit	
		01A1Fh	per unit	01A1Fh	per unit	
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	per unit	01A20h	per unit	
		01A21h	per unit	01A21h	per unit	
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	per unit	01A22h	per unit	
		01A23h	per unit	01A23h	per unit	
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	per unit	01A24h	per unit	
		01A25h	per unit	01A25h	per unit	
	REF Calibration	REF Calibration Tag	01A26h	12h	01A26h	12h
		REF Calibration length	01A27h	06h	01A27h	06h
REF 1.2-V Reference		01A28h	per unit	01A28h	per unit	
		01A29h	per unit	01A29h	per unit	
REF 2.0-V Reference		01A2Ah	per unit	01A2Ah	per unit	
		01A2Bh	per unit	01A2Bh	per unit	
REF 2.5-V Reference		01A2Ch	per unit	01A2Ch	per unit	
	01A2Dh	per unit	01A2Dh	per unit		
Random Number	128-bit Random Number Tag	01A2Eh	15h	01A2Eh	15h	
	Random Number Length	01A2Fh	10h	01A2Fh	10h	
	128-bit Random Number ⁽⁴⁾	01A30h	per unit	01A30h	per unit	
		01A31h	per unit	01A31h	per unit	
		01A32h	per unit	01A32h	per unit	
		01A33h	per unit	01A33h	per unit	
		01A34h	per unit	01A34h	per unit	
		01A35h	per unit	01A35h	per unit	
		01A36h	per unit	01A36h	per unit	
		01A37h	per unit	01A37h	per unit	
		01A38h	per unit	01A38h	per unit	
		01A39h	per unit	01A39h	per unit	
		01A3Ah	per unit	01A3Ah	per unit	
		01A3Bh	per unit	01A3Bh	per unit	
		01A3Ch	per unit	01A3Ch	per unit	
		01A3Dh	per unit	01A3Dh	per unit	
		01A3Eh	per unit	01A3Eh	per unit	
01A3Fh	per unit	01A3Fh	per unit			
BSL Configuration	BSL Tag	01A40h	1Ch	01A40h	1Ch	
	BSL length	01A41h	02h	01A41h	02h	
	BSL Interface	01A42h	00h	01A42h	01h	
	BSL Interface Configuration	01A43h	00h	01A43h	48h	

(4) 128-bit Random Number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

6.13 Memory

Table 6-35 shows the memory map for all devices.

Table 6-35. Memory Organization⁽¹⁾

		MSP430FR5972(1) MSP430FR5922(1) MSP430FR5872(1)	MSP430FR5970 MSP430FR5870
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Total Size	63KB 00FFFFh–00FF80h 013FFFh–004400h	32KB 00FFFFh–00FF80h 00FF7Fh–008000h
RAM	Sect 1	2KB 0023FFh–001C00h	2KB 0023FFh–001C00h
Device Descriptor Info (TLV) (FRAM)		256 B 001AFFh–001A00h	256 B 001AFFh–001A00h
Information memory (FRAM)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootstrap loader (BSL) memory (ROM)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4KB 000FFFh–000020h	4KB 000FFFh–000020h
Tiny RAM	Size	26 B 000001Fh–000006h	26 B 000001Fh–000006h
Reserved (Read Only) ⁽²⁾	Size	6 B 000005h–000000h	6 B 000005h–000000h

(1) All address space not listed is considered vacant memory.

(2) Read as: D032h at 00h (Opcode: BIS.W LPM4, SR), 00F0h at 02h (Opcode: BIS.W LPM4, SR), 3FFFh at 04h (Opcode: JMP\$)

6.13.1 Peripheral File Map

Table 6-36. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-37)	0100h	000h-01Fh
PMM (see Table 6-38)	0120h	000h-01Fh
FRAM Control (see Table 6-39)	0140h	000h-00Fh
CRC16 (see Table 6-40)	0150h	000h-007h
RAM Controller (see Table 6-41)	0158h	000h-001h
Watchdog (see Table 6-42)	015Ch	000h-001h
CS (see Table 6-43)	0160h	000h-00Fh
SYS (see Table 6-44)	0180h	000h-01Fh
Shared Reference (see Table 6-45)	01B0h	000h-001h
Port P1, P2 (see Table 6-46)	0200h	000h-01Fh
Port P3, P4 (see Table 6-47)	0220h	000h-01Fh
Port P5, P6 (see Table 6-48)	0240h	000h-01Fh
Port P7 (see Table 6-49)	0260h	000h-01Fh
Port P9 (see Table 6-50)	0280h	000h-01Fh
Port PJ (see Table 6-51)	0320h	000h-01Fh
Timer_A TA0 (see Table 6-52)	0340h	000h-02Fh
Timer_A TA1 (see Table 6-53)	0380h	000h-02Fh
Timer_B TB0 (see Table 6-54)	03C0h	000h-02Fh
Timer_A TA2 (see Table 6-55)	0400h	000h-02Fh
Capacitive Touch I/O 0 (see Table 6-56)	0430h	000h-00Fh
Timer_A TA3 (see Table 6-57)	0440h	000h-02Fh
Capacitive Touch I/O 1 (see Table 6-58)	0470h	000h-00Fh
Real-Time Clock (RTC_C) (see Table 6-59)	04A0h	000h-01Fh
32-bit Hardware Multiplier (see Table 6-60)	04C0h	000h-02Fh
DMA General Control (see Table 6-61)	0500h	000h-00Fh
DMA Channel 0 (see Table 6-61)	0510h	000h-00Fh
DMA Channel 1 (see Table 6-61)	0520h	000h-00Fh
DMA Channel 2 (see Table 6-61)	0530h	000h-00Fh
MPU Control (see Table 6-62)	05A0h	000h-00Fh
eUSCI_A0 (see Table 6-63)	05C0h	000h-01Fh
eUSCI_A1 (see Table 6-64)	05E0h	000h-01Fh
eUSCI_B0 (see Table 6-65)	0640h	000h-02Fh
eUSCI_B1 (see Table 6-66)	0680h	000h-02Fh
ADC12_B (see Table 6-67)	0800h	000h-09Fh
Comparator_E (see Table 6-68)	08C0h	000h-00Fh
CRC32 (see Table 6-69)	0980h	000h-02Fh
AES (see Table 6-70)	09C0h	000h-00Fh

Table 6-37. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-38. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM interrupt flags	PMMIFG	0Ah
PM5 Control 0	PM5CTL0	10h

Table 6-39. FRAM Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

Table 6-40. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRCDI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-41. RAM Controller Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM controller control register 0	RCCTL0	00h

Table 6-42. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-43. CS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch

Table 6-44. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
JTAG mailbox control	SYSJMBC	06h

Table 6-44. SYS Registers (Base Address: 0180h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-45. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 6-46. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-47. Port P3, P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 selection 0	P3SEL0	0Ah
Port P3 selection 1	P3SEL1	0Ch
Port P3 interrupt vector word	P3IV	0Eh

Table 6-47. Port P3, P4 Registers (Base Address: 0220h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 complement selection	P3SELC	16h
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 selection 0	P4SEL0	0Bh
Port P4 selection 1	P4SEL1	0Dh
Port P4 complement selection	P4SELC	17h
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

Table 6-48. Port P5, P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 selection 0	P5SEL0	0Ah
Port P5 selection 1	P5SEL1	0Ch
Reserved		0Eh
Port P5 complement selection	P5SELC	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 selection 0	P6SEL0	0Bh
Port P6 selection 1	P6SEL1	0Dh
Port P6 complement selection	P6SELC	17h
Reserved		1Eh
Reserved		19h
Reserved		1Bh
Reserved		1Dh

Table 6-49. Port P7 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pullup/pulldown enable	P7REN	06h

Table 6-49. Port P7 Registers (Base Address: 0260h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 selection 0	P7SEL0	0Ah
Port P7 selection 1	P7SEL1	0Ch
Reserved		0Eh
Port P7 complement selection	P7SELC	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch

Table 6-50. Port P9 Registers (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 pullup/pulldown enable	P9REN	06h
Port P9 selection 0	P9SEL0	0Ah
Port P9 selection 1	P9SEL1	0Ch
Reserved		0Eh
Port P9 complement selection	P9SELC	16h
Reserved		18h
Reserved		1Ah
Reserved		1Ch

Table 6-51. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ selection 0	PJSEL0	0Ah
Port PJ selection 1	PJSEL1	0Ch
Port PJ complement selection	PJSELC	16h

Table 6-52. Timer_A TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TAOCTL	00h
Capture/compare control 0	TAOCTL0	02h
Capture/compare control 1	TAOCTL1	04h
Capture/compare control 2	TAOCTL2	06h
TA0 counter register	TAOR	10h
Capture/compare register 0	TAOCCR0	12h
Capture/compare register 1	TAOCCR1	14h
Capture/compare register 2	TAOCCR2	16h
TA0 expansion register 0	TAOEX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-53. Timer_A TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-54. Timer_B TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-55. Timer_A TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
TA2 register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 6-56. Capacitive Touch I/O 0 Registers (Base Address: 0430h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 0 control	CAPTIO0CTL	0Eh

Table 6-57. Timer_A TA3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h
Capture/compare control 1	TA3CCTL1	04h
Capture/compare control 2	TA3CCTL2	06h
Capture/compare control 3	TA3CCTL3	08h
Capture/compare control 4	TA3CCTL4	0Ah
TA3 register	TA3R	10h
Capture/compare register 0	TA3CCR0	12h
Capture/compare register 1	TA3CCR1	14h
Capture/compare register 2	TA3CCR2	16h
Capture/compare register 3	TA3CCR3	18h
Capture/compare register 4	TA3CCR4	1Ah
TA3 expansion register 0	TA3EX0	20h
TA3 interrupt vector	TA3IV	2Eh

Table 6-58. Capacitive Touch I/O 1 Registers (Base Address: 0470h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 1 control	CAPTIO1CTL	0Eh

Table 6-59. RTC_C Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC password	RTCPWD	01h
RTC control 1	RTCCTL1	02h
RTC control 3	RTCCTL3	03h
RTC offset calibration	RTCOCAL	04h
RTC temperature compensation	RTTCMP	06h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year	RTCYEAR	16h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion register	BIN2BCD	1Ch
BCD-to-Binary conversion register	BCD2BIN	1Eh

Table 6-60. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 6-61. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h

Table 6-61. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 6-62. MPU Control Registers (Base Address: 05A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
MPU control 0	MPUCTL0	00h
MPU control 1	MPUCTL1	02h
MPU Segmentation Border 2	MPUSEGB2	04h
MPU Segmentation Border 1	MPUSEGB1	06h
MPU access management	MPUSAM	08h
MPU IP control 0	MPUIPC0	0Ah
MPU IP Encapsulation Segment Border 2	MPUIPSEGB2	0Ch
MPU IP Encapsulation Segment Border 1	MPUIPSEGB1	0Eh

Table 6-63. eUSCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A baud rate 0	UCA0BR0	06h
eUSCI_A baud rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status word	UCA0STATW	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	UCA0IRTCTL	12h
eUSCI_A IrDA receive control	UCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 6-64. eUSCI_A1 Registers (Base Address:05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI_A control word 1	UCA1CTLW1	02h
eUSCI_A baud rate 0	UCA1BR0	06h
eUSCI_A baud rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status word	UCA1STATW	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	UCA1IRTCTL	12h

Table 6-64. eUSCI_A1 Registers (Base Address:05E0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A IrDA receive control	UCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

Table 6-65. eUSCI_B0 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B received address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI_B I2C slave address	UCB0I2CSA	20h
eUSCI_B interrupt enable	UCB0IE	2Ah
eUSCI_B interrupt flags	UCB0IFG	2Ch
eUSCI_B interrupt vector word	UCB0IV	2Eh

Table 6-66. eUSCI_B1 Registers (Base Address: 0680h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB1CTLW0	00h
eUSCI_B control word 1	UCB1CTLW1	02h
eUSCI_B bit rate 0	UCB1BR0	06h
eUSCI_B bit rate 1	UCB1BR1	07h
eUSCI_B status word	UCB1STATW	08h
eUSCI_B byte counter threshold	UCB1TBCNT	0Ah
eUSCI_B receive buffer	UCB1RXBUF	0Ch
eUSCI_B transmit buffer	UCB1TXBUF	0Eh
eUSCI_B I2C own address 0	UCB1I2COA0	14h
eUSCI_B I2C own address 1	UCB1I2COA1	16h
eUSCI_B I2C own address 2	UCB1I2COA2	18h
eUSCI_B I2C own address 3	UCB1I2COA3	1Ah
eUSCI_B received address	UCB1ADDRX	1Ch
eUSCI_B address mask	UCB1ADDMASK	1Eh
eUSCI_B I2C slave address	UCB1I2CSA	20h
eUSCI_B interrupt enable	UCB1IE	2Ah
eUSCI_B interrupt flags	UCB1IFG	2Ch
eUSCI_B interrupt vector word	UCB1IV	2Eh

Table 6-67. ADC12_B Registers (Base Address: 0800h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B Control 0	ADC12CTL0	00h
ADC12_B Control 1	ADC12CTL1	02h
ADC12_B Control 2	ADC12CTL2	04h
ADC12_B Control 3	ADC12CTL3	06h
ADC12_B Window Comparator Low Threshold Register	ADC12LO	08h
ADC12_B Window Comparator High Threshold Register	ADC12HI	0Ah
ADC12_B Interrupt Flag Register 0	ADC12IFGR0	0Ch
ADC12_B Interrupt Flag Register 1	ADC12IFGR1	0Eh
ADC12_B Interrupt Flag Register 2	ADC12IFGR2	10h
ADC12_B Interrupt Enable Register 0	ADC12IER0	12h
ADC12_B Interrupt Enable Register 1	ADC12IER1	14h
ADC12_B Interrupt Enable Register 2	ADC12IER2	16h
ADC12_B Interrupt Vector	ADC12IV	18h
ADC12_B Memory Control 0	ADC12MCTL0	20h
ADC12_B Memory Control 1	ADC12MCTL1	22h
ADC12_B Memory Control 2	ADC12MCTL2	24h
ADC12_B Memory Control 3	ADC12MCTL3	26h
ADC12_B Memory Control 4	ADC12MCTL4	28h
ADC12_B Memory Control 5	ADC12MCTL5	2Ah
ADC12_B Memory Control 6	ADC12MCTL6	2Ch
ADC12_B Memory Control 7	ADC12MCTL7	2Eh
ADC12_B Memory Control 8	ADC12MCTL8	30h
ADC12_B Memory Control 9	ADC12MCTL9	32h
ADC12_B Memory Control 10	ADC12MCTL10	34h
ADC12_B Memory Control 11	ADC12MCTL11	36h
ADC12_B Memory Control 12	ADC12MCTL12	38h
ADC12_B Memory Control 13	ADC12MCTL13	3Ah
ADC12_B Memory Control 14	ADC12MCTL14	3Ch
ADC12_B Memory Control 15	ADC12MCTL15	3Eh
ADC12_B Memory Control 16	ADC12MCTL16	40h
ADC12_B Memory Control 17	ADC12MCTL17	42h
ADC12_B Memory Control 18	ADC12MCTL18	44h
ADC12_B Memory Control 19	ADC12MCTL19	46h
ADC12_B Memory Control 20	ADC12MCTL20	48h
ADC12_B Memory Control 21	ADC12MCTL21	4Ah
ADC12_B Memory Control 22	ADC12MCTL22	4Ch
ADC12_B Memory Control 23	ADC12MCTL23	4Eh
ADC12_B Memory Control 24	ADC12MCTL24	50h
ADC12_B Memory Control 25	ADC12MCTL25	52h
ADC12_B Memory Control 26	ADC12MCTL26	54h
ADC12_B Memory Control 27	ADC12MCTL27	56h
ADC12_B Memory Control 28	ADC12MCTL28	58h
ADC12_B Memory Control 29	ADC12MCTL29	5Ah
ADC12_B Memory Control 30	ADC12MCTL30	5Ch
ADC12_B Memory Control 31	ADC12MCTL31	5Eh
ADC12_B Memory 0	ADC12MEM0	60h
ADC12_B Memory 1	ADC12MEM1	62h

Table 6-67. ADC12_B Registers (Base Address: 0800h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC12_B Memory 2	ADC12MEM2	64h
ADC12_B Memory 3	ADC12MEM3	66h
ADC12_B Memory 4	ADC12MEM4	68h
ADC12_B Memory 5	ADC12MEM5	6Ah
ADC12_B Memory 6	ADC12MEM6	6Ch
ADC12_B Memory 7	ADC12MEM7	6Eh
ADC12_B Memory 8	ADC12MEM8	70h
ADC12_B Memory 9	ADC12MEM9	72h
ADC12_B Memory 10	ADC12MEM10	74h
ADC12_B Memory 11	ADC12MEM11	76h
ADC12_B Memory 12	ADC12MEM12	78h
ADC12_B Memory 13	ADC12MEM13	7Ah
ADC12_B Memory 14	ADC12MEM14	7Ch
ADC12_B Memory 15	ADC12MEM15	7Eh
ADC12_B Memory 16	ADC12MEM16	80h
ADC12_B Memory 17	ADC12MEM17	82h
ADC12_B Memory 18	ADC12MEM18	84h
ADC12_B Memory 19	ADC12MEM19	86h
ADC12_B Memory 20	ADC12MEM20	88h
ADC12_B Memory 21	ADC12MEM21	8Ah
ADC12_B Memory 22	ADC12MEM22	8Ch
ADC12_B Memory 23	ADC12MEM23	8Eh
ADC12_B Memory 24	ADC12MEM24	90h
ADC12_B Memory 25	ADC12MEM25	92h
ADC12_B Memory 26	ADC12MEM26	94h
ADC12_B Memory 27	ADC12MEM27	96h
ADC12_B Memory 28	ADC12MEM28	98h
ADC12_B Memory 29	ADC12MEM29	9Ah
ADC12_B Memory 30	ADC12MEM30	9Ch
ADC12_B Memory 31	ADC12MEM31	9Eh

Table 6-68. Comparator_E Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator control register 0	CECTL0	00h
Comparator control register 1	CECTL1	02h
Comparator control register 2	CECTL2	04h
Comparator control register 3	CECTL3	06h
Comparator interrupt register	CEINT	0Ch
Comparator interrupt vector word	CEIV	0Eh

Table 6-69. CRC32 Registers (Base Address: 0980h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC32 data input	CRC32DIW0	00h
Reserved		02h
Reserved		04h
CRC32 data input reverse	CRC32DIRBW0	06h
CRC32 initialization and result word 0	CRC32INIRESW0	08h

Table 6-69. CRC32 Registers (Base Address: 0980h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC32 initialization and result word 1	CRC32INIRESW1	0Ah
CRC32 result reverse word 1	CRC32RESRW1	0Ch
CRC32 result reverse word 0	CRC32RESRW1	0Eh
CRC16 data input	CRC16DIW0	10h
Reserved		12h
Reserved		14h
CRC16 data input reverse	CRC16DIRBW0	16h
CRC16 initialization and result word 0	CRC16INIRESW0	18h
Reserved		1Ah
Reserved		1Ch
CRC16 result reverse word 0	CRC16RESRW1	1Eh
Reserved		20h
Reserved		22h
Reserved		24h
Reserved		26h
Reserved		28h
Reserved		2Ah
Reserved		2Ch
Reserved		2Eh

Table 6-70. AES Accelerator Registers (Base Address: 09C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
AES accelerator control register 0	AESACTL0	00h
Reserved		02h
AES accelerator status register	AESASTAT	04h
AES accelerator key register	AESAKEY	06h
AES accelerator data in register	AESADIN	008h
AES accelerator data out register	AESADOUT	00Ah
AES accelerator XORed data in register	AESAXDIN	00Ch
AES accelerator XORed data in register (no trigger)	AESAXIN	00Eh

6.14 Identification

6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 8.2](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [Section 6.12](#).

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [Section 8.2](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [Section 6.12](#).

6.14.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming Via the JTAG Interface User's Guide* ([SLAU320](#)).

7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

It is recommended to connect a combination of a 1- μ F plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommended for better noise isolation from digital to analog circuits on the board and are especially recommended to achieve high analog accuracy.

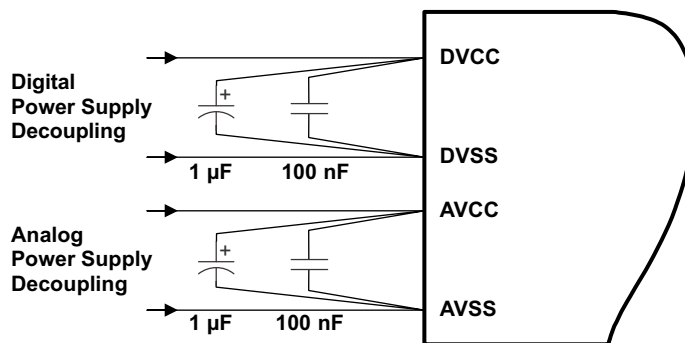


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

Depending on the device variant (see [Section 3](#)), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated according to [Section 4.5](#).

[Figure 7-2](#) shows a typical connection diagram.

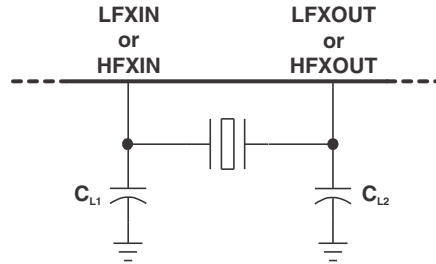


Figure 7-2. Typical Crystal Connection

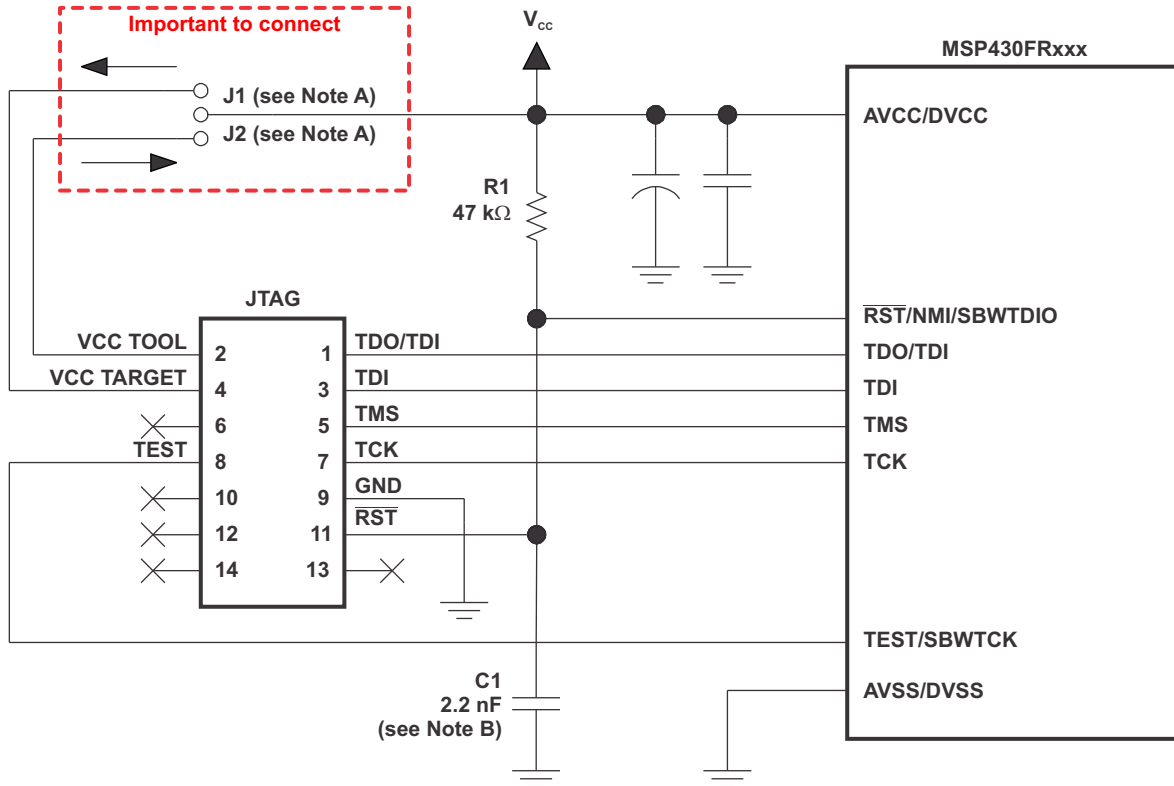
See the application report *MSP430 32-kHz Crystal Oscillators* ([SLAA322](#)) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. [Figure 7-3](#) shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. [Figure 7-4](#) shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

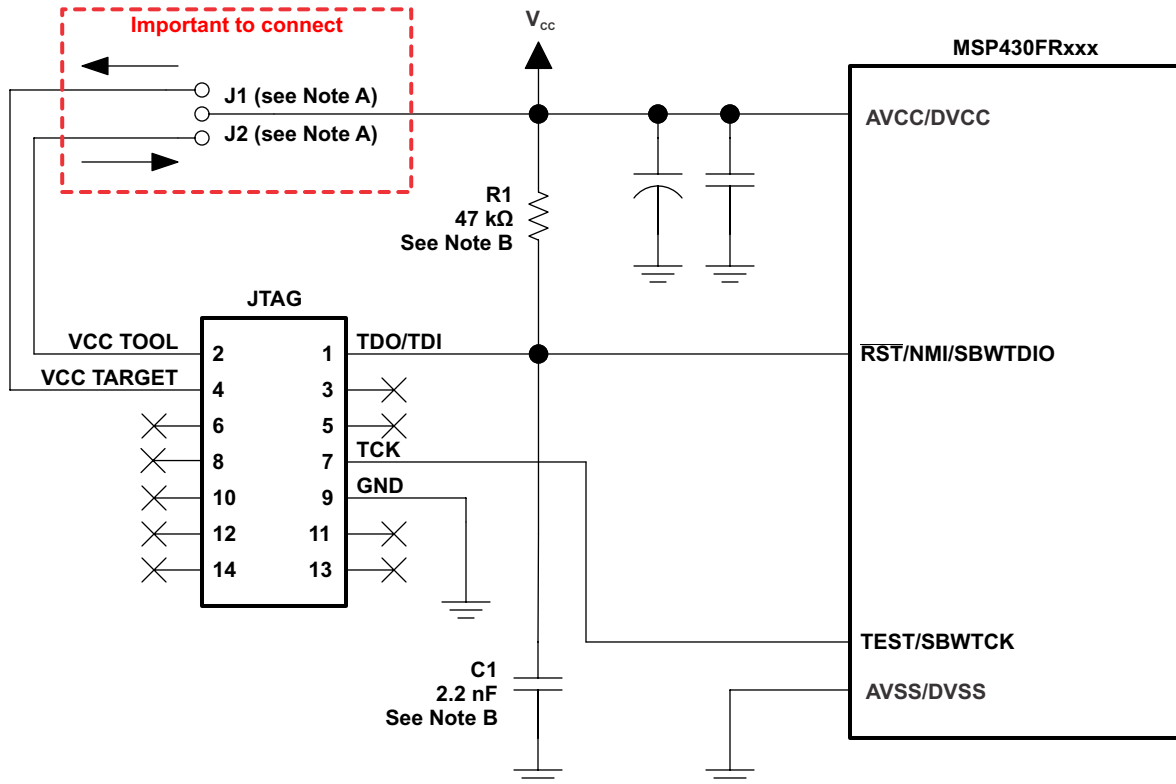
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. [Figure 7-3](#) and [Figure 7-4](#) show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)).



- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 2.2 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device $\overline{\text{RST}}/\text{NMI}/\text{SBWTIO}$ pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}/\text{NMI}$ pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}/\text{NMI}$ pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}/\text{NMI}$ pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}/\text{NMI}$ pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-k Ω pullup resistor to the $\overline{\text{RST}}/\text{NMI}$ pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR58xx*, *MSP430FR59xx*, *MSP430FR68xx*, and *MSP430FR69xx Family User's Guide (SLAU367)* for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.5](#).

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See the application report *MSP430 32-kHz Crystal Oscillators* ([SLAA322](#)) for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Refer to the *Circuit Board Layout Techniques* design guide ([SLOA089](#)) for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See the application report *MSP430 System-Level ESD Considerations* ([SLAA530](#)) for guidelines.

7.1.7 Do's and Don'ts

It is recommended to power AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC12_B Peripheral

7.2.1.1 Partial Schematic

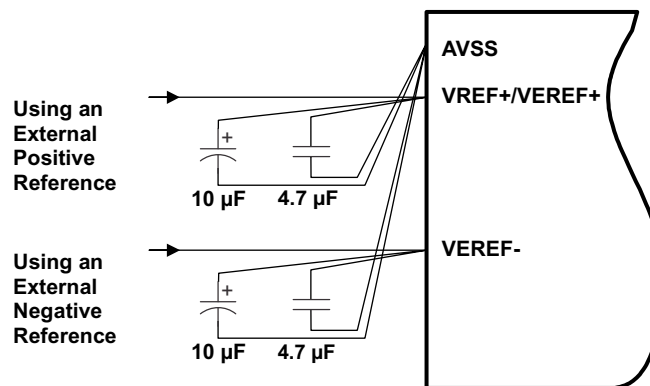


Figure 7-5. ADC12_B Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 7.1.1](#) combined with the connections shown in [Section 7.2.1.1](#) prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommend to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as specified in the $I_{O(VREF+)}$ specification of the Reference module.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- μ F capacitor is used to buffer the reference pin and filter any low-frequency ripple. A bypass capacitor of 4.7 μ F is used to filter out any high frequency noise.

7.2.1.3 Detailed Design Procedure

For additional design information, see the application report *Designing With the MSP430FR58xx, FR59xx, FR68xx, and FR69xx ADC* ([SLAA624](#)).

7.2.1.4 Layout Guidelines

Component that are shown in the partial schematic (see [Figure 7-5](#)) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the ADC12_B, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Getting Started

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the [Getting Started page](#).

8.1.1.2 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

8.1.1.2.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* ([SLAU157](#)) for details on the available features. See the application reports *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6* ([SLAA393](#)) and *MSP430™ Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology* ([SLAA603](#)) for further information.

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER	LPMx.5 DEBUGGING SUPPORT	EnergyTrace+ +
MSP430Xv2	Yes	Yes	3	Yes	Yes	No	No	Yes	Yes

EnergyTrace™ technology is supported with Code Composer Studio version 6.0 and newer. It requires specialized debugger circuitry, which is supported with the second-generation onboard eZ-FET flash emulation tool and second-generation standalone MSP-FET JTAG emulator. See the application report *MSP430™ Advanced Power Optimizations: ULP Advisor™ and EnergyTrace™ Technology* ([SLAA603](#)), the *Code Composer Studio for MSP430 User's Guide* ([SLAU157](#)), and the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)) for more detailed information.

8.1.1.2.2 Recommended Hardware Options

8.1.1.2.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

PACKAGE	TARGET BOARD AND PROGRAMMER BUNDLE	TARGET BOARD ONLY
64-pin LQFP (PM)	MSP-FET430U64F	MSP-TS430PM64F

8.1.1.2.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. The MSP430FR6989 LaunchPad™ Development Kit ([MSP-EXP430FR6989](#)) can be used to experiment with the devices in this data sheet. See www.ti.com/msp430tools for details.

8.1.1.2.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third-party suppliers. See the full list of available tools at www.ti.com/msp430tools.

PART NUMBER	PC PORT	FEATURES	PROVIDER
MSP-FET	USB	Fast download and debugging. Supports EnergyTrace++ Technology. Compatible with 4-wire JTAG and 2-wire Spy-Bi-Wire (SBW) JTAG modes. Small form factor.	Texas Instruments
MSP-FET430UIF	USB	Legacy interface – superseded by MSP-FET. Compatible with 4-wire JTAG and 2-wire Spy-Bi-Wire (SBW) JTAG modes.	Texas Instruments

8.1.1.2.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

PART NUMBER	PC PORT	FEATURES	PROVIDER
MSP-GANG	Serial and USB	Program up to eight devices at a time. Works with PC or standalone.	Texas Instruments

8.1.1.2.3 Recommended Software Options

8.1.1.2.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

8.1.1.2.3.2 MSPWare

[MSPWare](#) is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSPWare also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSPWare is available as a component of CCS or as a standalone package.

8.1.1.2.3.3 TI-RTOS Kernel

[TI-RTOS Kernel](#) is an advanced real-time operating system for the MSP430 microcontrollers. It features preemptive deterministic multi-tasking, hardware abstraction, memory management, and real-time analysis. TI-RTOS Kernel is available free of charge and is provided with full source code.

8.1.1.2.3.4 Command-Line Programmer

[MSP430 Flasher](#) is an open-source shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 microcontroller without the need for an IDE.

8.1.1.3 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430FR59721). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the electrical specifications for the final device

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed TI's internal qualification testing.

MSP – Fully-qualified development-support product

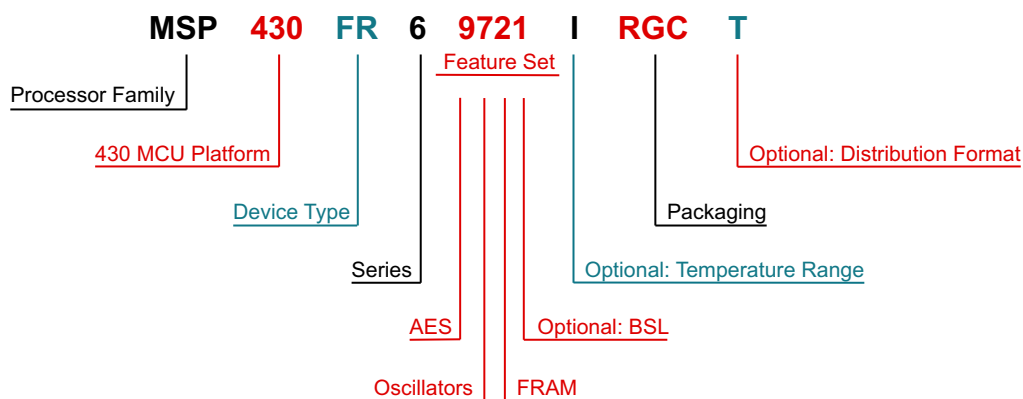
XMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGC) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.



Processor Family	MSP = Mixed Signal Processor XMS = Experimental Silicon			
430 MCU Platform	TI's 16-bit Low-Power Microcontroller Platform			
Device Type	Memory Type FR = FRAM			
Series	FRAM 6 Series = Up to 16 MHz with LCD FRAM 5 Series = Up to 16 MHz without LCD			
Feature Set	AES 9 = AES 8 = No AES	Oscillators 7 = HFXT + LFXT 2 = LFXT	FRAM (KB) 2 = 64 0 = 32	Optional - BSL 1 = I ² C No value = UART
Optional: Temperature Range	S = 0°C to 50°C I = -40°C to 85°C T = -40°C to 105°C			
Packaging	http://www.ti.com/packaging			
Optional: Distribution Format	T = Small Reel R = Large Reel No Markings = Tube or Tray			
Optional: Additional Features	-Q1 = Automotive Qualified -EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C)			

Figure 8-1. Device Nomenclature

8.2 Documentation Support

The following documents describe the MSP430FR597x(1), MSP430FR592x(1) and MSP430FR587x(1) microcontrollers. Copies of these documents are available on the Internet at www.ti.com.

- [SLAU367](#) *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, MSP430FR69xx Family User's Guide.* Detailed description of all modules and peripherals available in this device family.
- [SLAZ631](#) *MSP430FR5972 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ643](#) *MSP430FR59721 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ665](#) *MSP430FR5922 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ666](#) *MSP430FR59221 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ637](#) *MSP430FR5970 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ632](#) *MSP430FR5872 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ644](#) *MSP430FR58721 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.
- [SLAZ638](#) *MSP430FR5870 Device Erratasheet.* Describes the known exceptions to the functional specifications for each silicon revision of this device.

8.3 Related Links

Table 8-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430FR5972	Click here	Click here	Click here	Click here	Click here
MSP430FR59721	Click here	Click here	Click here	Click here	Click here
MSP430FR5970	Click here	Click here	Click here	Click here	Click here
MSP430FR5922	Click here	Click here	Click here	Click here	Click here
MSP430FR59221	Click here	Click here	Click here	Click here	Click here
MSP430FR5872	Click here	Click here	Click here	Click here	Click here
MSP430FR58721	Click here	Click here	Click here	Click here	Click here
MSP430FR5870	Click here	Click here	Click here	Click here	Click here

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.5 Trademarks

EnergyTrace++, MSP430, ULP Advisor, EnergyTrace, LaunchPad, Code Composer Studio, E2E are trademarks of Texas Instruments.

Microsoft is a registered trademark of Microsoft Corporation.

All other trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR5870IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5870	Samples
MSP430FR5870IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5870	Samples
MSP430FR58721IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR58721	Samples
MSP430FR58721IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR58721	Samples
MSP430FR5872IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5872	Samples
MSP430FR5872IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5872	Samples
MSP430FR59221IG56R	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59221	Samples
MSP430FR59221IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59221	Samples
MSP430FR59221IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59221	Samples
MSP430FR5922IG56R	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5922	Samples
MSP430FR5922IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5922	Samples
MSP430FR5922IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5922	Samples
MSP430FR5922IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5922	Samples
MSP430FR5970IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5970	Samples
MSP430FR5970IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5970	Samples
MSP430FR59721IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59721	Samples
MSP430FR59721IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59721	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR59721IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR59721	Samples
MSP430FR5972IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5972	Samples
MSP430FR5972IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5972	Samples
MSP430FR5972IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	FR5972	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

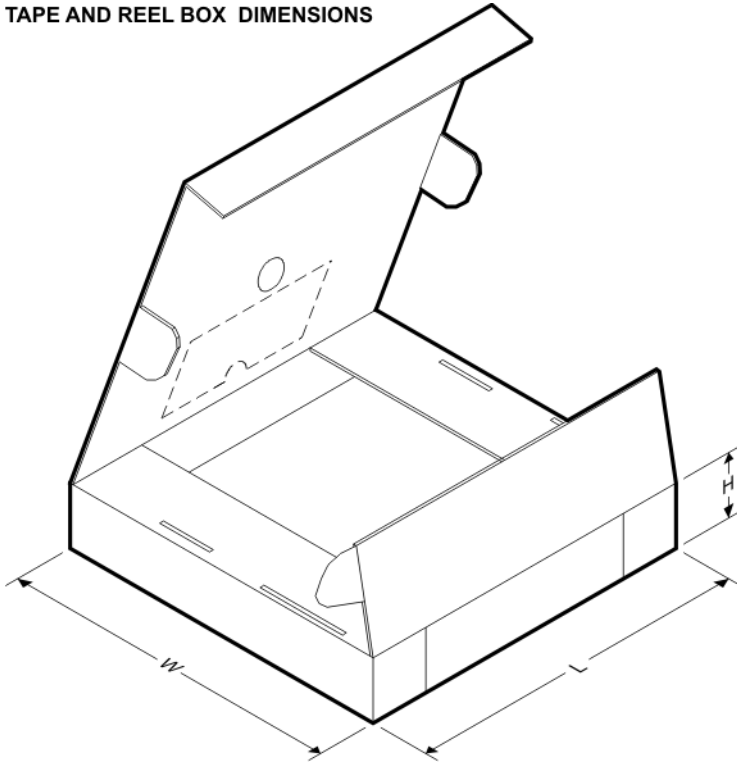
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR5870IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5870IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR58721IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR58721IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5872IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5872IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR59221IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR59221IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR59221IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5922IG56R	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
MSP430FR5922IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5922IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5970IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5970IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR59721IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR59721IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP430FR5972IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430FR5972IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR5870IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5870IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR58721IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR58721IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR5872IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5872IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR59221IG56R	TSSOP	DGG	56	2000	367.0	367.0	45.0
MSP430FR59221IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR59221IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR5922IG56R	TSSOP	DGG	56	2000	367.0	367.0	45.0
MSP430FR5922IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5922IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR5970IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5970IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR59721IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR59721IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430FR5972IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430FR5972IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0

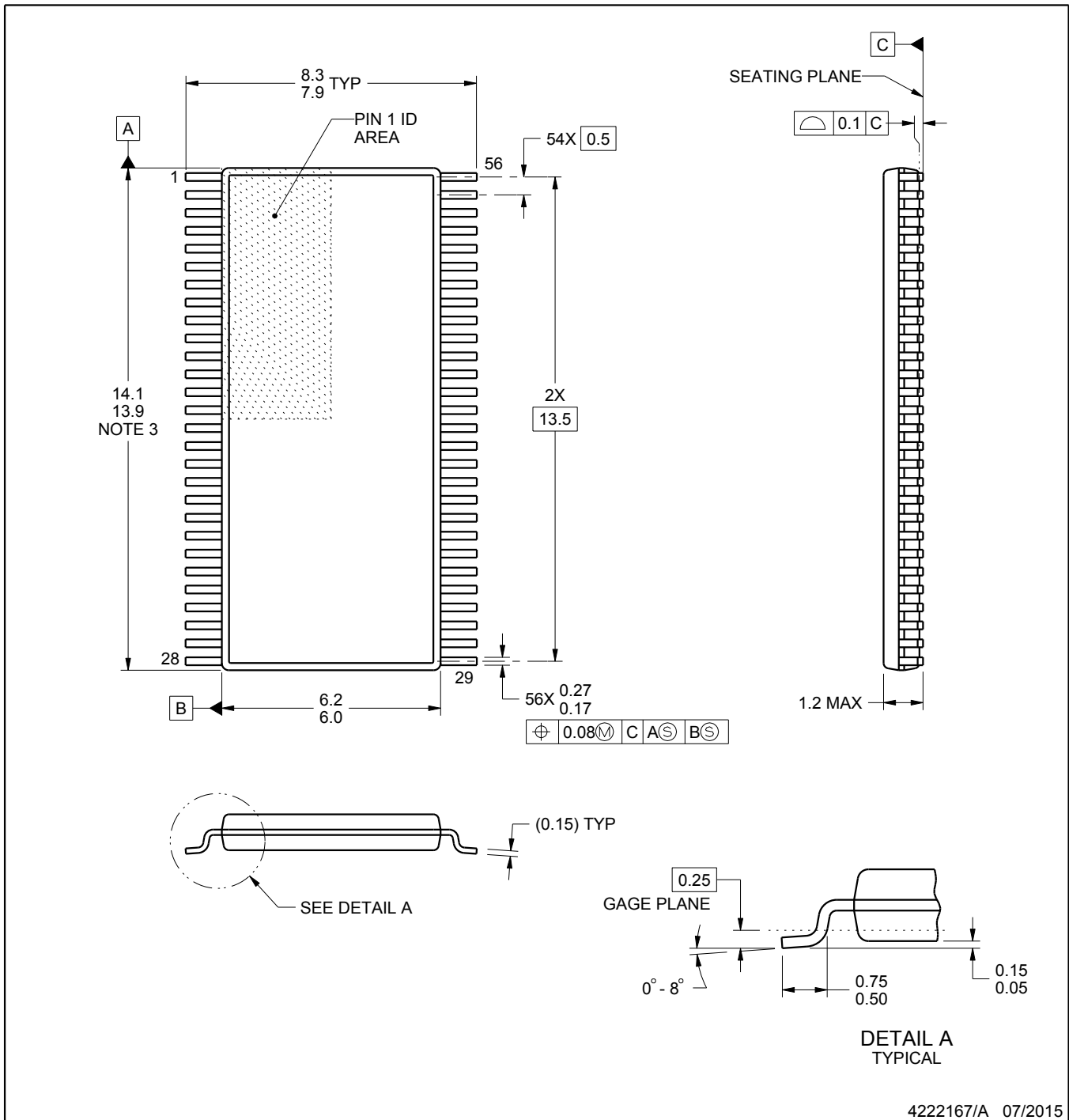
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4222167/A 07/2015

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

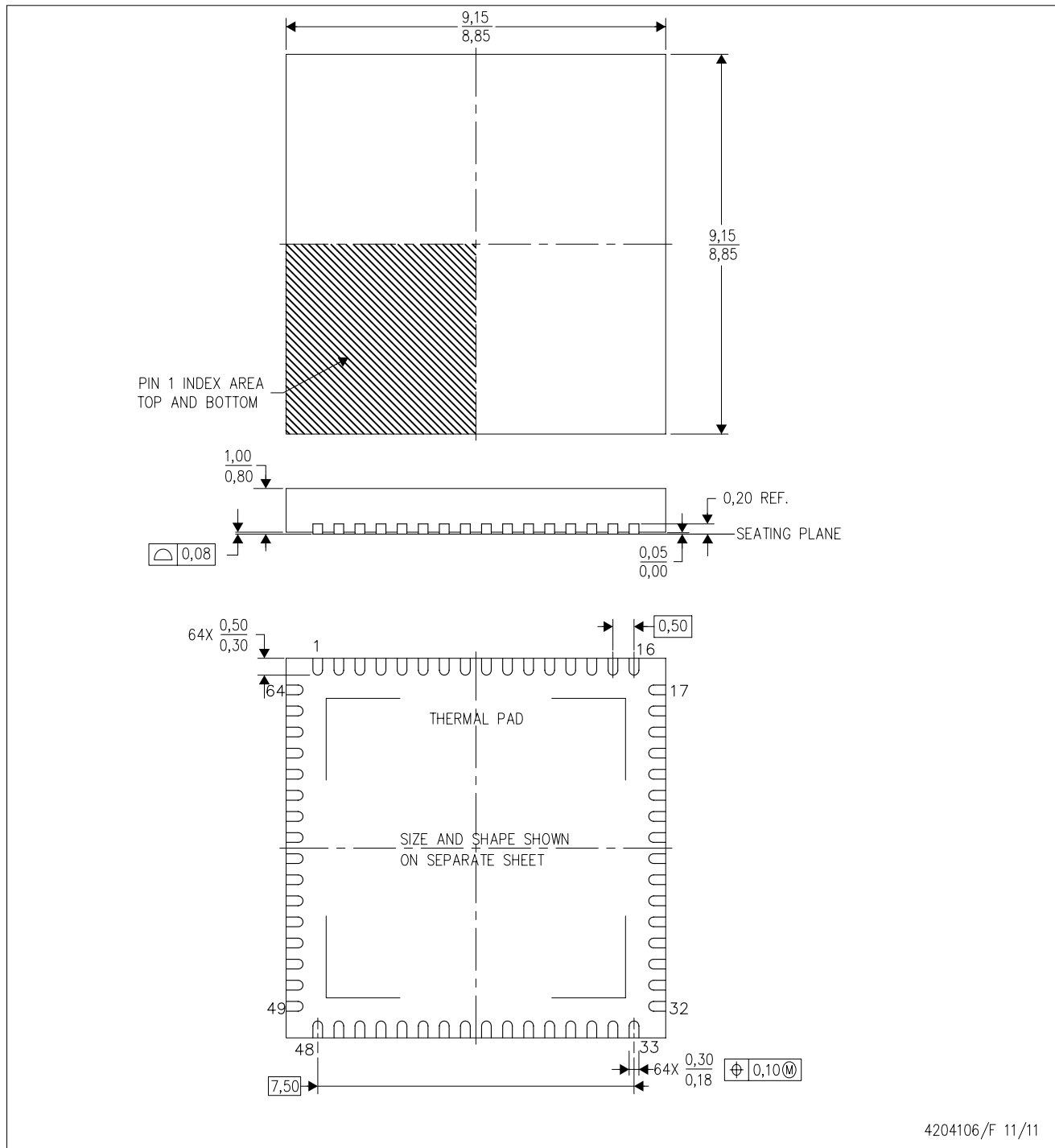
4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



4204106/F 11/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

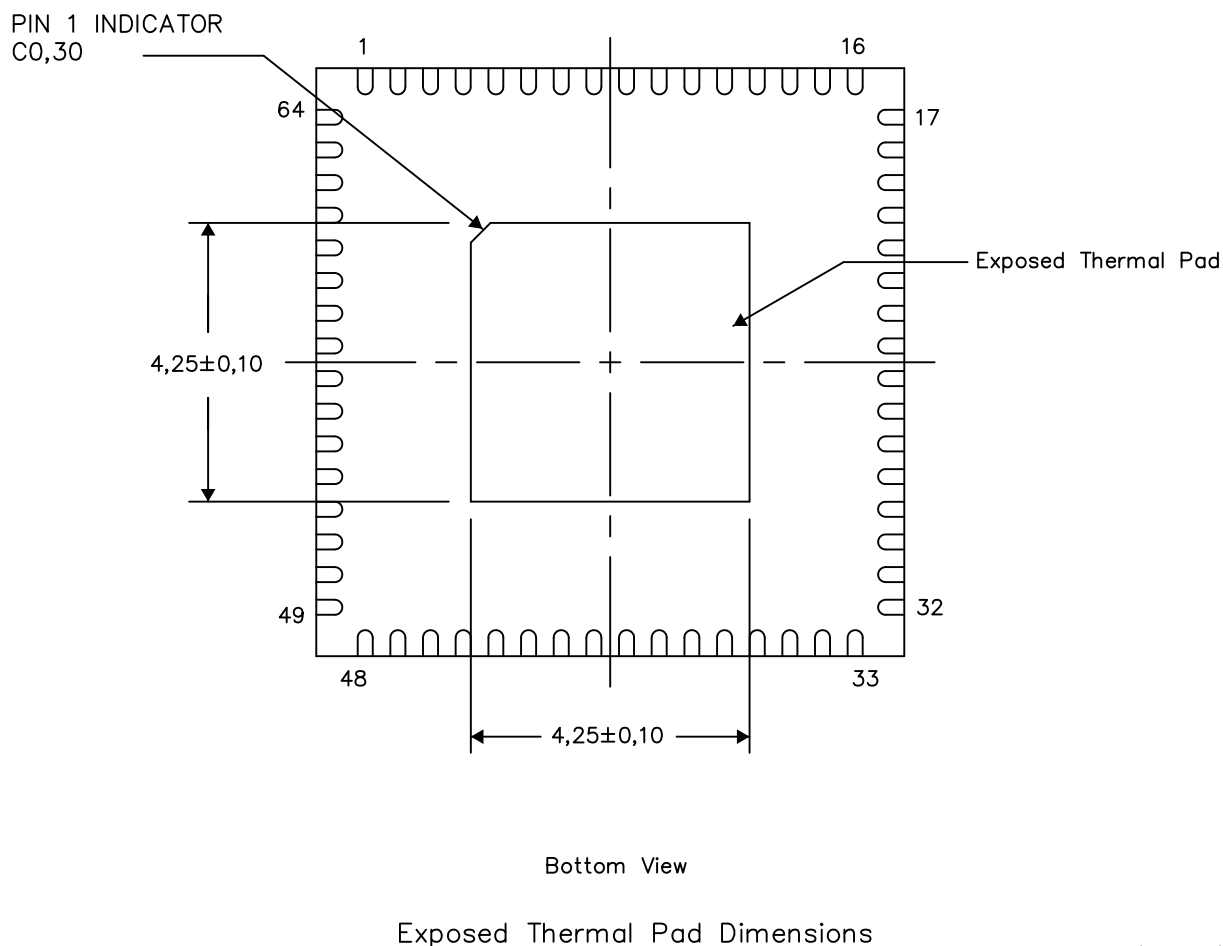
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

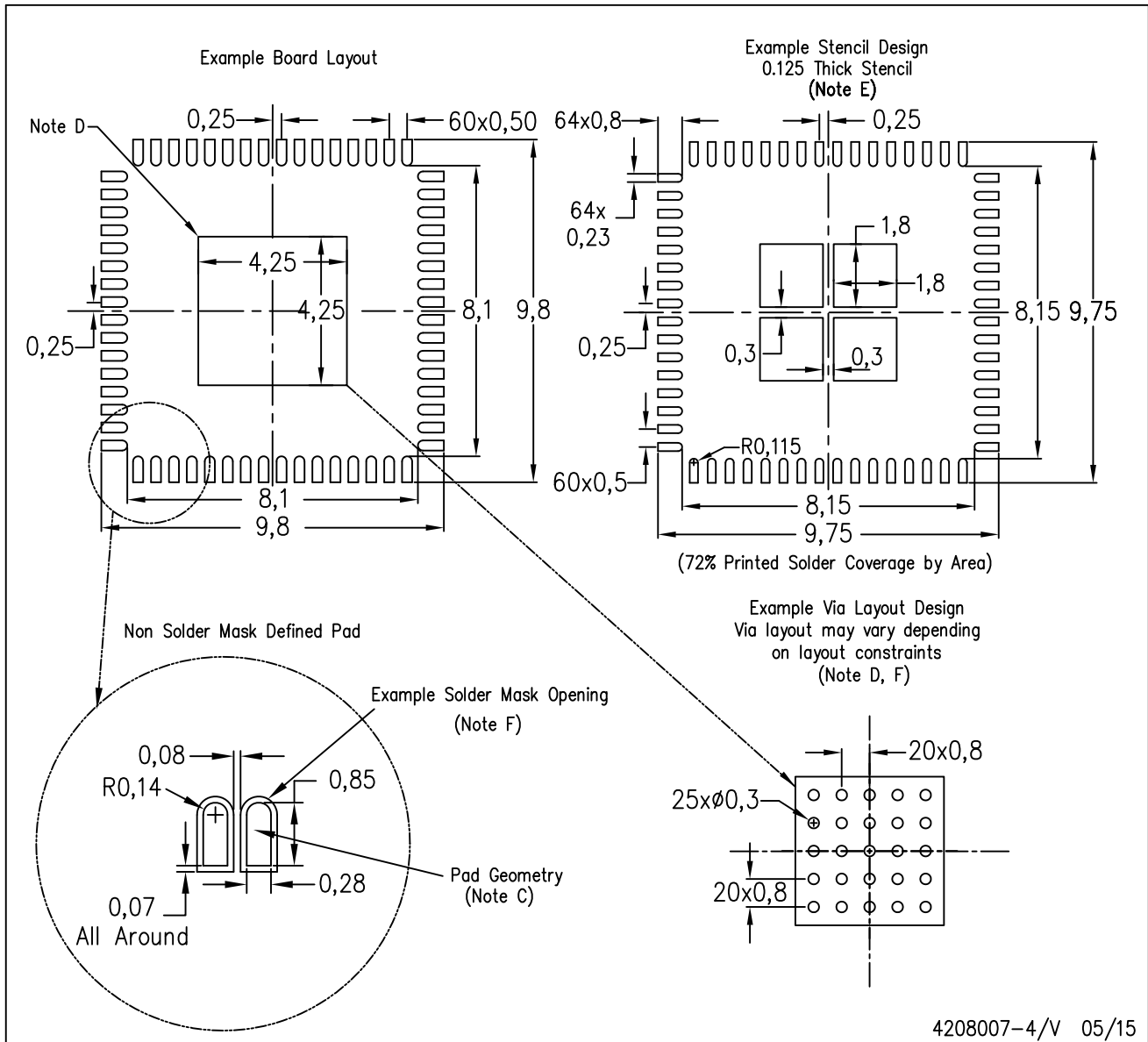


4206192-3/AE 03/15

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD

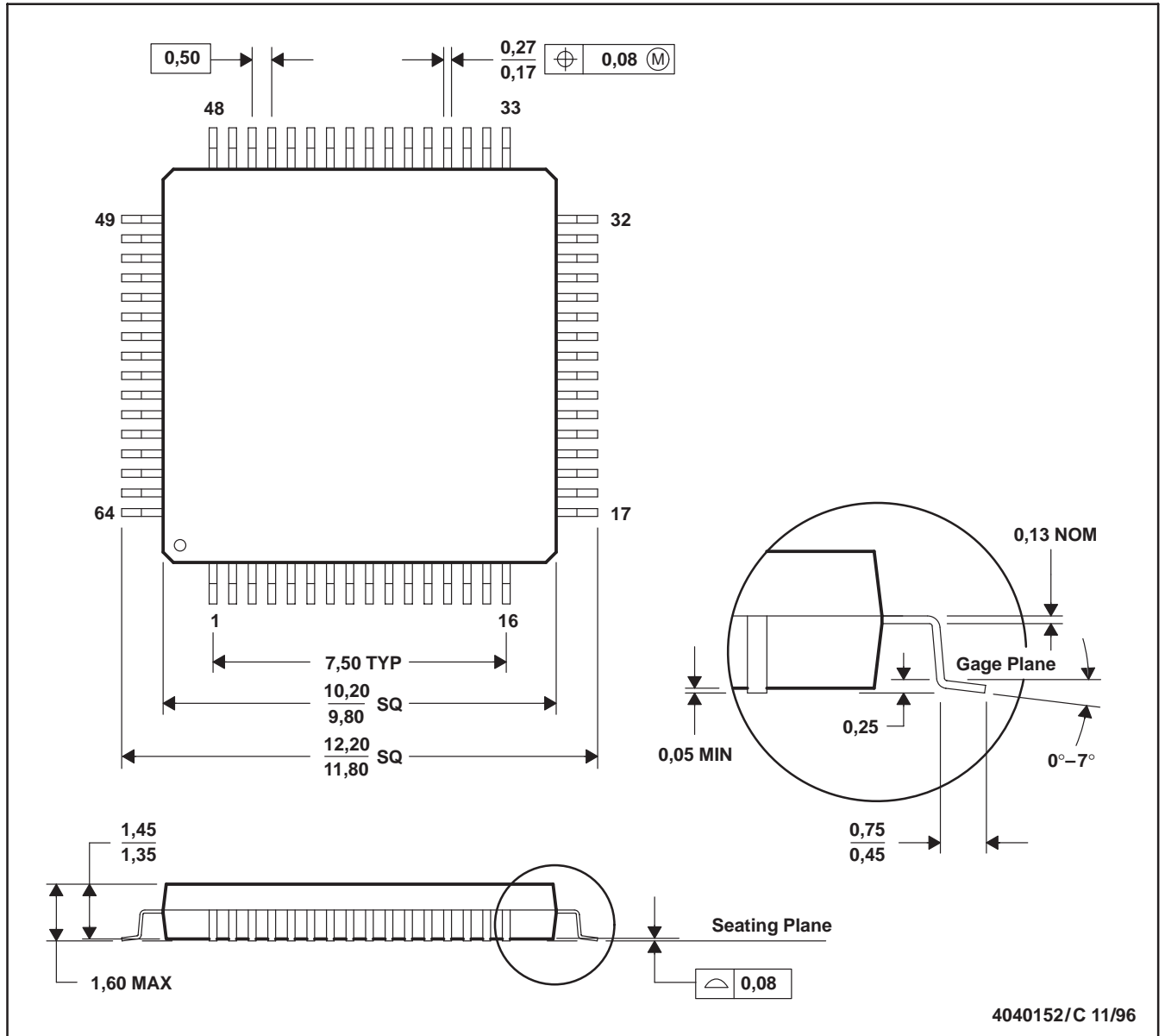


4208007-4/V 05/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PM (S-PQFP-G64)

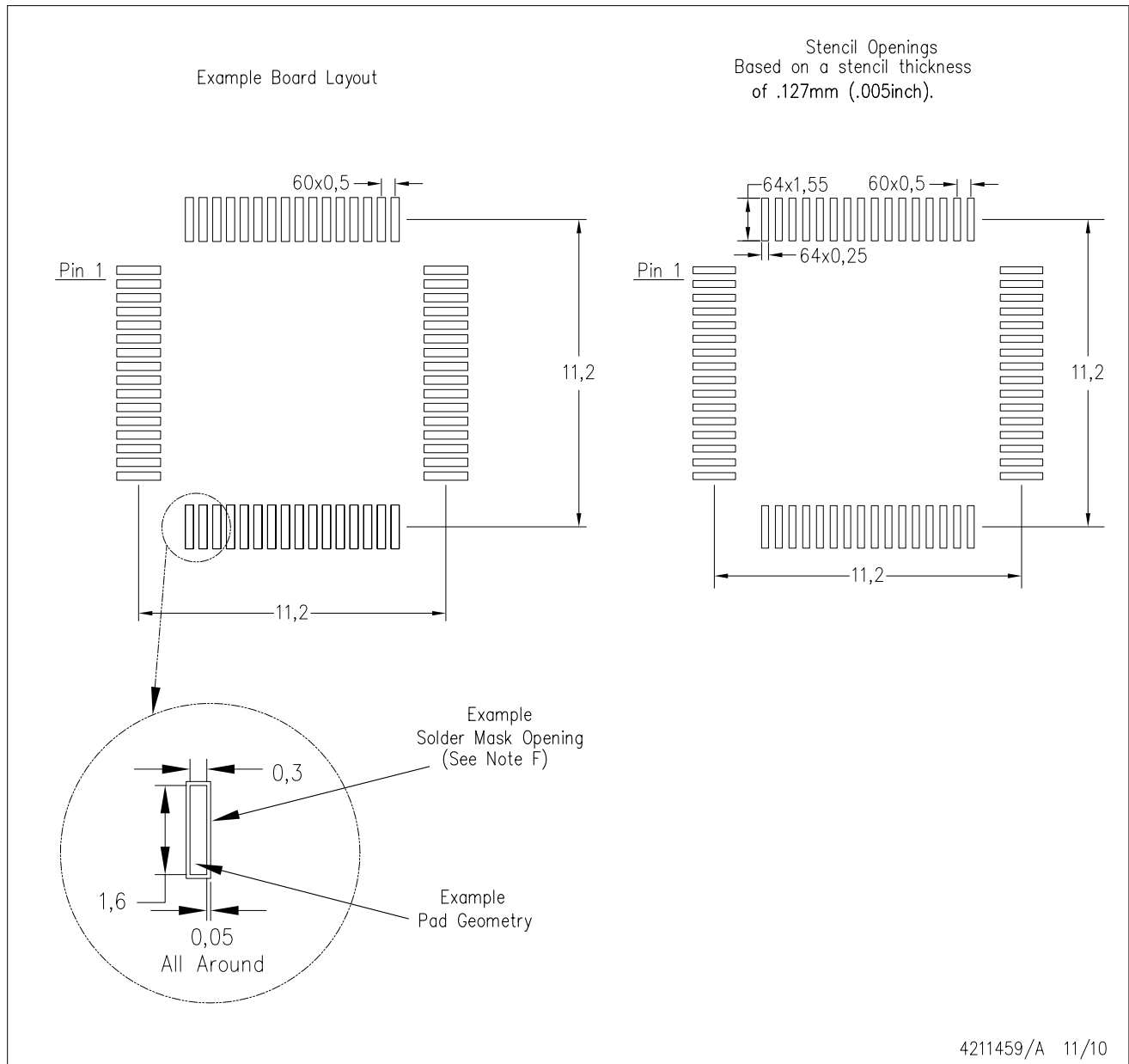
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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