MSP430FG43x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low Supply-Voltage Range, 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 300 µA at 1 MHz, 2.2 V
  - Standby Mode: 1.1 µA
  - Off Mode (RAM Retention): 0.1 µA
- Five Power-Saving Modes
- Wakeup From Standby Mode in Less Than 6 µs
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- Single-Channel Internal DMA
- 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold and Autoscan Feature
- Three Configurable Operational Amplifiers
- Dual 12-Bit Digital-to-Analog Converters (DACs) With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Serial Communication Interface (USART), Select Asynchronous UART or Synchronous SPI by Software
- Brownout Detector
- Supply-Voltage Supervisor and Monitor With Programmable Level Detection
- Bootstrap Loader (BSL)
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Integrated Liquid Crystal Display (LCD) Driver for up to 128 Segments
- Available in 113-Ball BGA (ZCA) and 80-Pin QFP (PN) Packages
- Section 3 Summarizes the Available Family Members
- For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide* (SLAU056)

1.2 Applications

- Analog and Digital Sensor Systems
- Digital Motor Control
- Remote Controls
- Thermostats
- Digital Timers
- Hand-Held Meters

1.3 Description

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 6 µs.

The MSP430FG43x devices are microcontrollers with two 16-bit timers, a high-performance 12-bit ADC, dual 12-bit DACs, three configurable operational amplifiers, one universal synchronous/asynchronous communication interface, DMA, 48 I/O pins, and an LCD driver.

Table 1-1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430FG439PN	LQFP (80)	12 mm x 12 mm
MSP430FG439ZCA	BGA (113)	7 mm x 7 mm

(1) For the most current device, package, and ordering information, see the Package Option Addendum in Section 8, or see the TI web site at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the Mechanical Data in Section 8.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.

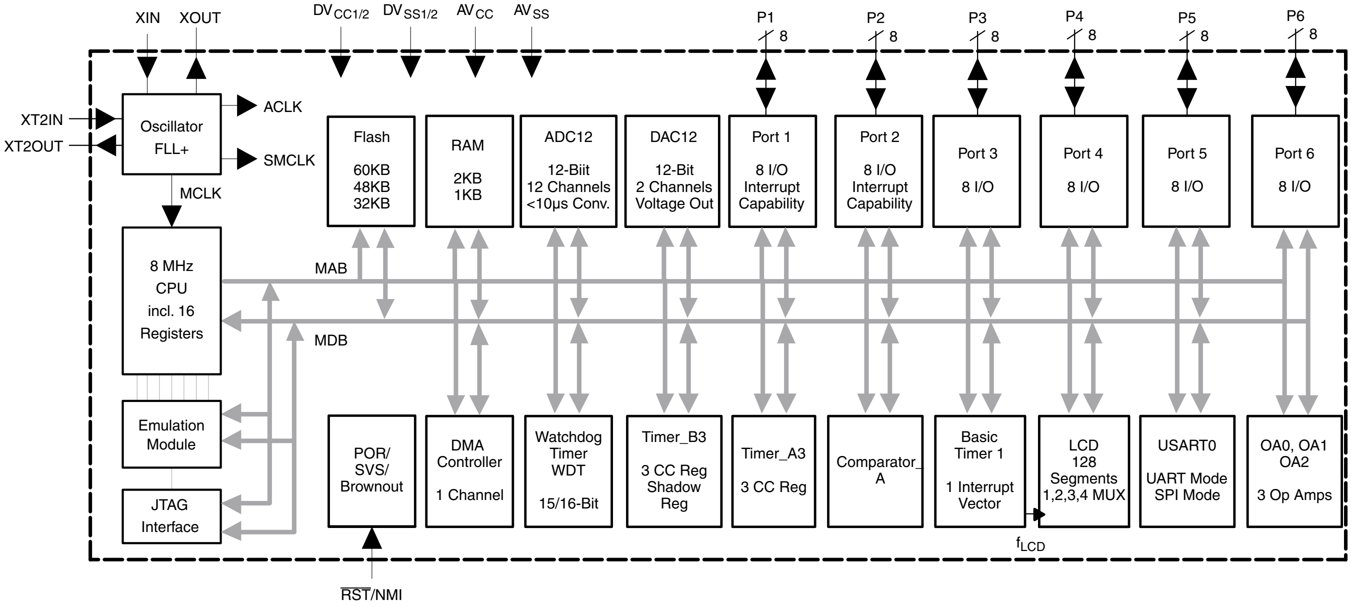

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2011) to Revision D	Page
• Document format and organization changes throughout, including addition of section numbering	1
• Added Section 1.2	1
• Added Device Information table	1
• Added Section 3	5
• Added ZCA package pinout	7
• Added ZCA package to Table 4-1	8
• Added Section 5 and moved all electrical specifications to it	12
• Added Section 5.2 and moved T_{stg} to it	12
• Added ZCA package to BSL table	47
• Added ZCA package to Timer_A3 table	49
• Added ZCA package to Timer_B3 table	50
• Moved Section 6.10	55
• Changed the values in the $\overline{\text{Port}}$/LCD column	59
• Changed the input signals (LCDPx[0:2]) in the top left of the figure	60
• Changed the input signal (LCDPx[2]) in the top left of the figure	61
• Changed the values in the DEVICE, PORT FUNCTION, and LCD SEGMENT FUNCTION columns	62
• Changed the input "1, If LCDPx ≥ 01h" near the top left of the figure	63
• Changed the values in the DEVICE, PORT FUNCTION, and LCD SEGMENT FUNCTION columns	63
• Changed the input "1, If LCDPx ≥ 01h" near the top left of the figure	64
• Changed the values in the DEVICE, PORT FUNCTION, and LCD SEGMENT FUNCTION columns	64
• Changed the input "1, If LCDPx ≥ 01h" near the top left of the figure	65
• Changed the values in the DEVICE, PORT FUNCTION, and LCD SEGMENT FUNCTION columns	65
• Changed the input "1, If LCDPx ≥ 01h" near the top left of the figure	66
• Changed the LCDPx column heading and values	66
• Changed the value in the $\overline{\text{Port}}$/LCD column	66
• Added Section 7	78
• Added Section 8	81

3 Device Comparison

The following table summarizes the available family members.

Table 3-1. Device Comparison(1) (2)

Device	FLASH (KB)	SRAM (KB)	ADC12	DAC12	Comp_A	Timer_A(3)	Timer_B(4)	USART	LCD	I/Os	Package Type
MSP430FG439	60	2	12 channels	2 channels	16 channels	3	3	Yes	Yes	48	80 PN 113 ZCA
MSP430FG438	48	2	12 channels	2 channels	16 channels	3	3	Yes	Yes	48	80 PN 113 ZCA
MSP430FG437	32	1	12 channels	2 channels	16 channels	3	3	Yes	Yes	48	80 PN 113 ZCA

(1) For the most current package and ordering information, see the Package Option Addendum in Section 8, or see the TI web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 capture/compare registers and PWM output generators and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pin assignments for the 80-pin PN package.

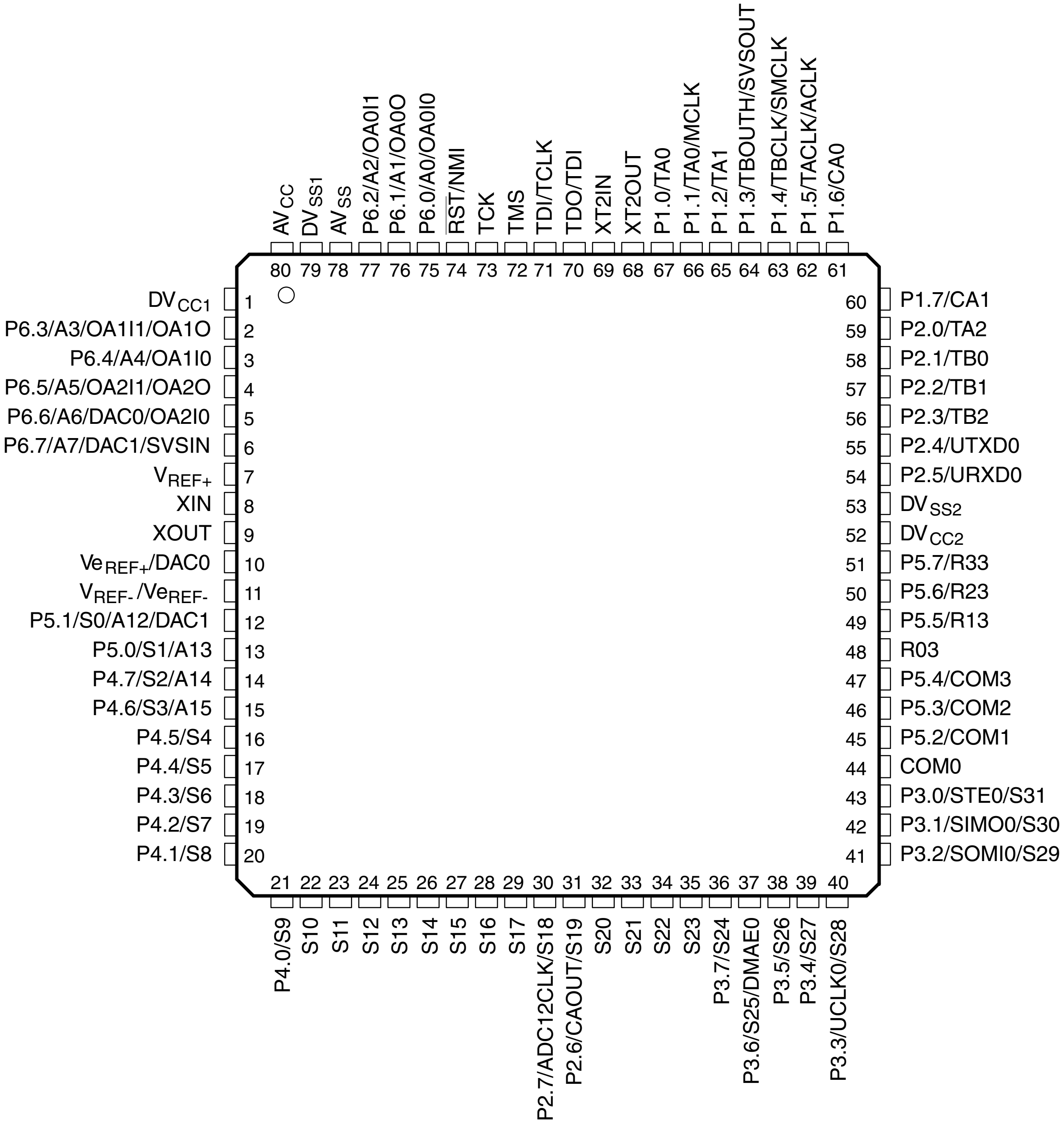
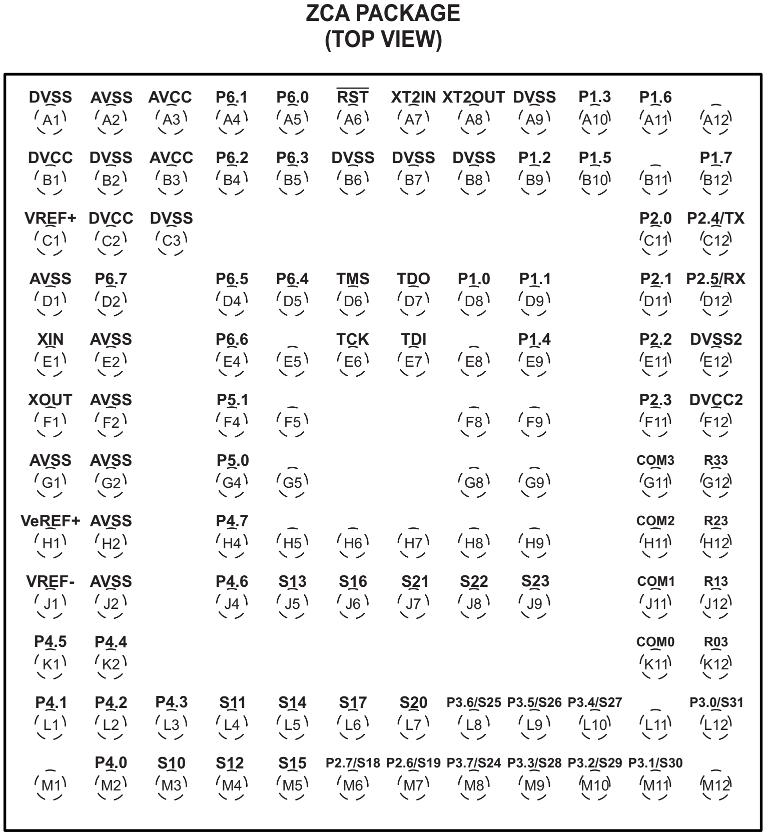


Figure 4-1. 80-Pin PN Package (Top View)

Figure 4-2 shows the pin assignments for the 113-pin ZCA package.



ZCA PACKAGE
(TOP VIEW)

DVSS A1	AVSS A2	AVCC A3	P6.1 A4	P6.0 A5	$\overline{\text{RST}}$ A6	XT2IN A7	XT2OUT A8	DVSS A9	P1.3 A10	P1.6 A11	A12
DVCC B1	DVSS B2	AVCC B3	P6.2 B4	P6.3 B5	DVSS B6	DVSS B7	DVSS B8	P1.2 B9	P1.5 B10	B11	P1.7 B12
VREF+ C1	DVCC C2	DVSS C3								P2.0 C11	P2.4/TX C12
AVSS D1	P6.7 D2		P6.5 D4	P6.4 D5	TMS D6	TDO D7	P1.0 D8	P1.1 D9		P2.1 D11	P2.5/RX D12
XIN E1	AVSS E2		P6.6 E4	E5	TCK E6	TDI E7	E8	P1.4 E9		P2.2 E11	DVSS2 E12
XOUT F1	AVSS F2		P5.1 F4	F5			F8	F9		P2.3 F11	DVCC2 F12
AVSS G1	AVSS G2		P5.0 G4	G5			G8	G9		COM3 G11	R33 G12
VeREF+ H1	AVSS H2		P4.7 H4	H5	H6	H7	H8	H9		COM2 H11	R23 H12
VREF- J1	AVSS J2		P4.6 J4	S13 J5	S16 J6	S21 J7	S22 J8	S23 J9		COM1 J11	R13 J12
P4.5 K1	P4.4 K2									COM0 K11	R03 K12
P4.1 L1	P4.2 L2	P4.3 L3	S11 L4	S14 L5	S17 L6	S20 L7	P3.6/S25 L8	P3.5/S26 L9	P3.4/S27 L10	L11	P3.0/S31 L12
M1	P4.0 M2	S10 M3	S12 M4	S15 M5	P2.7/S18 M6	P2.6/S19 M7	P3.7/S24 M8	P3.3/S28 M9	P3.2/S29 M10	P3.1/S30 M11	M12

Figure 4-2. 113-Pin ZCA Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PN	ZCA		
DVCC1	1	B1, C2		Digital supply voltage, positive terminal.
P6.3/A3/OA1I1/OA1O	2	B5	I/O	General-purpose digital I/O Analog input a3—12-bit ADC OA1 output and/or input multiplexer on +terminal and −terminal
P6.4/A4/OA1I0	3	D5	I/O	General-purpose digital I/O Analog input a4—12-bit ADC OA1 input multiplexer on +terminal and −terminal
P6.5/A5/OA2I1/OA2O	4	D4	I/O	General-purpose digital I/O Analog input a5—12-bit ADC OA2 output and/or input multiplexer on +terminal and −terminal
P6.6/A6/DAC0/OA2I0	5	E4	I/O	General-purpose digital I/O Analog input a6—12-bit ADC DAC12.0 output OA2 input multiplexer on +terminal and −terminal
P6.7/A7/DAC1/SVSIN	6	D2	I/O	General-purpose digital I/O Analog input a7—12-bit ADC DAC12.1 output/analog input to supply voltage supervisor
VREF+	7	C1	O	Positive output terminal of the reference voltage in the ADC
XIN	8	E1	I	Input terminal of crystal oscillator XT1
XOUT	9	F1	O	Output terminal of crystal oscillator XT1
VeREF+/DAC0	10	H1	I/O	Positive input terminal for an external reference voltage to the 12-bit ADC/DAC12.0 output
VREF−/VeREF−	11	J1	I	Negative terminal for the 12-bit ADC's reference voltage for both sources, the internal reference voltage or an external applied reference voltage to the 12-bit ADC.
P5.1/S0/A12/DAC1	12	F4	I/O	General-purpose digital I/O LCD segment output 0 Analog input a12—12-bit ADC DAC12.1 output
P5.0/S1/A13	13	G4	I/O	General-purpose digital I/O LCD segment output 1 Analog input a13—12-bit ADC
P4.7/S2/A14	14	H4	I/O	General-purpose digital I/O LCD segment output 2 Analog input a14—12-bit ADC
P4.6/S3/A15	15	J4	I/O	General-purpose digital I/O LCD segment output 3 Analog input a15—12-bit ADC
P4.5/S4	16	K1	I/O	General-purpose digital I/O LCD segment output 4
P4.4/S5	17	K2	I/O	General-purpose digital I/O LCD segment output 5
P4.3/S6	18	L3	I/O	General-purpose digital I/O LCD segment output 6
P4.2/S7	19	L2	I/O	General-purpose digital I/O LCD segment output 7
P4.1/S8	20	L1	I/O	General-purpose digital I/O LCD segment output 8
P4.0/S9	21	M2	I/O	General-purpose digital I/O LCD segment output 9
S10	22	M3	O	LCD segment output 10

Table 4-1. Signal Descriptions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PN	ZCA		
S11	23	L4	O	LCD segment output 11
S12	24	M4	O	LCD segment output 12
S13	25	J5	O	LCD segment output 13
S14	26	L5	O	LCD segment output 14
S15	27	M5	O	LCD segment output 15
S16	28	J6	O	LCD segment output 16
S17	29	L6	O	LCD segment output 17
P2.7/ADC12CLK/S18	30	M6	I/O	General-purpose digital I/O Conversion clock—12-bit ADC LCD segment output 18
P2.6/CAOUT/S19	31	M7	I/O	General-purpose digital I/O Comparator_A output / LCD segment output 19
S20	32	L7	O	LCD segment output 20
S21	33	J7	O	LCD segment output 21
S22	34	J8	O	LCD segment output 22
S23	35	J9	O	LCD segment output 23
P3.7/S24	36	M8	I/O	General-purpose digital I/O LCD segment output 24
P3.6/S25/DMAE0	37	L8	I/O	General-purpose digital I/O LCD segment output 25/DMA Channel 0 external trigger
P3.5/S26	38	L9	I/O	General-purpose digital I/O LCD segment output 26
P3.4/S27	39	L10	I/O	General-purpose digital I/O LCD segment output 27
P3.3/UCLK0/S28	40	M9	I/O	General-purpose digital I/O External clock input—USART0/UART or SPI mode, clock output—USART0/SPI mode LCD segment output 28
P3.2/SOMI0/S29	41	M10	I/O	General-purpose digital I/O Slave out/master in of USART0/SPI mode LCD segment output 29
P3.1/SIMO0/S30	42	M11	I/O	General-purpose digital I/O Slave in/master out of USART0/SPI mode LCD segment output 30
P3.0/STE0/S31	43	L12	I/O	General-purpose digital I/O Slave transmit enable-USART0/SPI mode LCD segment output 31
COM0	44	K11	O	Common output, COM0−3 are used for LCD backplanes.
P5.2/COM1	45	J11	I/O	General-purpose digital I/O Common output, COM0−3 are used for LCD backplanes.
P5.3/COM2	46	H11	I/O	General-purpose digital I/O Common output, COM0−3 are used for LCD backplanes.
P5.4/COM3	47	G11	I/O	General-purpose digital I/O Common output, COM0−3 are used for LCD backplanes.
R03	48	K12	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	49	J12	I/O	General-purpose digital I/O input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	50	H12	I/O	General-purpose digital I/O Input port of second most positive analog LCD level (V2)
P5.7/R33	51	G12	I/O	General-purpose digital I/O Output port of most positive analog LCD level (V1)
DVCC2	52	F12		Digital supply voltage, positive terminal

Table 4-1. Signal Descriptions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PN	ZCA		
DVSS2	53	E12		Digital supply voltage, negative terminal
P2.5/URXD0	54	D12	I/O	General-purpose digital I/O Receive data in—USART0/UART mode
P2.4/UTXD0	55	C12	I/O	General-purpose digital I/O Transmit data out—USART0/UART mode
P2.3/TB2	56	F11	I/O	General-purpose digital I/O Timer_B3 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	57	E11	I/O	General-purpose digital I/O Timer_B3 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	58	D11	I/O	General-purpose digital I/O Timer_B3 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	59	C11	I/O	General-purpose digital I/O Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA1	60	B12	I/O	General-purpose digital I/O Comparator_A input
P1.6/CA0	61	A11	I/O	General-purpose digital I/O Comparator_A input
P1.5/TACLK/ACLK	62	B10	I/O	General-purpose digital I/O Timer_A, clock signal TACLK input ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/SMCLK	63	E9	I/O	General-purpose digital I/O Input clock TBCLK—Timer_B3 Submain system clock SMCLK output
P1.3/TBOUTH/SVSOUT	64	A10	I/O	General-purpose digital I/O Switch all PWM digital output ports to high impedance—Timer_B3 TB0 to TB2 SVS: output of SVS comparator
P1.2/TA1	65	B9	I/O	General-purpose digital I/O Timer_A, Capture: CCI1A, compare: Out1 output
P1.1/TA0/MCLK	66	D9	I/O	General-purpose digital I/O Timer_A. Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin BSL receive
P1.0/TA0	67	D8	I/O	General-purpose digital I/O Timer_A. Capture: CCI0A input, compare: Out0 output BSL transmit
XT2OUT	68	A8	O	Output terminal of crystal oscillator XT2
XT2IN	69	A7	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	70	D7	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	71	E7	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	72	D6	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	73	E6	I	Test clock. TCK is the clock input port for device programming and test.
RST/NMI	74	A6	I	Reset or nonmaskable interrupt input
P6.0/A0/OA0I0	75	A5	I/O	General-purpose digital I/O Analog input a0 − 12-bit ADC OA0 input multiplexer on +terminal and −terminal
P6.1/A1/OA0O	76	A4	I/O	General-purpose digital I/O Analog input a1 − 12-bit ADC OA0 output
P6.2/A2/OA0I1	77	B4	I/O	General-purpose digital I/O Analog input a2 − 12-bit ADC OA0 input multiplexer on + terminal and − terminal

Table 4-1. Signal Descriptions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PN	ZCA		
AVSS	78	A2, D1, E2, F2, G2, G1, H2, J2		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1, and LCD resistive divider circuitry.
DVSS1	79	A1, B2, C3, B6, B7, B8, A9		Digital supply voltage, negative terminal
AVCC	80	A3, B3		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DVCC1/DVCC2.
Reserved		(1)		Reserved

(1) A12, B11, E5, E8, F5, F8, F9, G5, G8, G9, H5, H6, H7, H8, H9, L11, M1, M12 are reserved and should be connected to ground.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin(2)	–0.3	V_{CC} + 0.3	V
Diode current at any device terminal		±2	mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}.The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

5.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range	Unprogrammed device	-55	150	°C
		Programmed device	-40	85	

5.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(1) (AVCC = DVCC1 = DVCC2 = V_{CC})	During program execution		1.8		3.6	V
		During program execution, SVS enabled and PORON = 1(2)		2		3.6	
		During flash memory programming		2.7		3.6	
V_{SS}	Supply voltage(1) (AVSS = DVSS1 = DVSS2 = V_{SS})			0		0	V
T_A	Operating free-air temperature range			–40		85	°C
$f_{(LFXT1)}$	XT1 crystal frequency(3)	LF selected, XTS_FLL = 0	Watch crystal		32.768		kHz
		XT1 selected, XTS_FLL = 1	Ceramic resonator	450		8000	
		XT1 selected, XTS_FLL = 1	Crystal	1000		8000	
$f_{(XT2)}$	XT2 crystal frequency		Ceramic resonator	450		8000	kHz
			Crystal	1000		8000	
$f_{(System)}$	Processor frequency (signal MCLK)		V_{CC} = 1.8 V	dc		4.15	MHz
			V_{CC} = 3.6 V	dc		8	

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.

(2) The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.

(3) In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

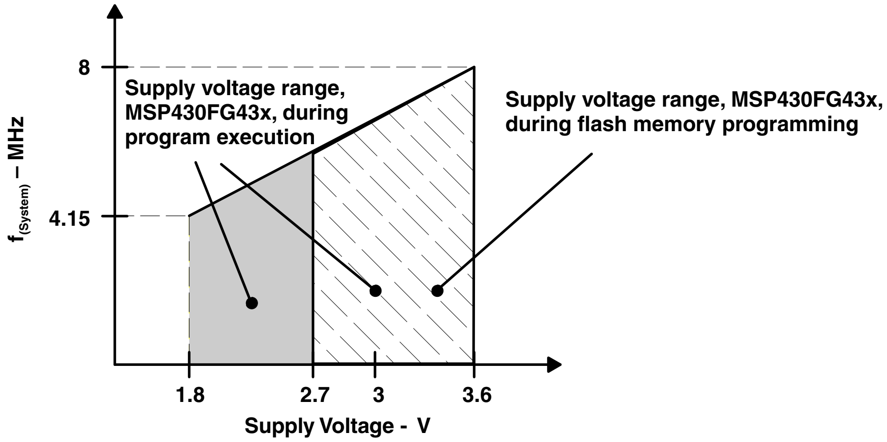


Figure 5-1. Frequency vs Supply Voltage, Typical Characteristic

5.4 Supply Current Into AV_{CC} + DV_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode (1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32768 Hz, XTS_FLL = 0, SELM = (0,1)	–40°C to 85°C	2.2 V		300	370	µA
			3 V		470	570	
$I_{(LPM0)}$	Low-power mode (LPM0) (1) (2)	–40°C to 85°C	2.2 V		55	70	µA
			3 V		95	110	
$I_{(LPM2)}$	Low-power mode (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 0 (3) (2)	–40°C to 85°C	2.2 V		11	14	µA
			3 V		17	22	
$I_{(LPM3)}$	Low-power mode (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1 (3) (4) (2)	–40°C	2.2 V		1	2	µA
		25°C			1.1	2	
		60°C			2	3	
		85°C			3.5	6	
		–40°C	3 V		1.8	2.8	
		25°C			1.6	2.7	
		60°C			2.5	3.5	
		85°C			4.2	7.5	
$I_{(LPM4)}$	Low-power mode (LPM4) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (3) (2)	–40°C	2.2 V		0.1	0.5	µA
		25°C			0.1	0.5	
		60°C			0.7	1.1	
		85°C			1.7	3	
		–40°C	3 V		0.1	0.8	
		25°C			0.1	0.8	
		60°C			0.8	1.2	
		85°C			1.9	3.5	

(1) Timer_B is clocked by $f_{(DCOCLK)} = f_{(DCO)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for brownout included.
(3) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(4) The current consumption in LPM3 is measured with active Basic Timer1 and LCD (ACLK selected). The current consumption of the Comparator_A and the SVS module are specified in the respective sections. The LPM3 currents are characterized with a KDS Daishinku DT−38 (6 pF) crystal and OSCCAPx = 01h.

Current consumption of active mode versus system frequency:

$$I_{(AM)} = I_{(AM)} [1\ \text{MHz}] \times f_{(System)} [\text{MHz}]$$

Current consumption of active mode versus supply voltage:

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

5.5 Schmitt-Trigger Inputs – Ports P1 to P6, $\overline{\text{RST}}$/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	2.2 V	1.1	1.55	V
		3 V	1.5	1.98	
V_{IT-}	Negative-going input threshold voltage	2.2 V	0.4	0.9	V
		3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	2.2 V	0.3	1.1	V
		3 V	0.5	1	

5.6 Inputs Px.y, TAx, TBx

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag(1)	2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer_A or Timer_B capture timing	TA0, TA1, TA2 TB0, TB1, TB2	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$	Timer_A or Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
$f_{(TBext)}$			3 V		10	
$f_{(TAint)}$	Timer_A or Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
$f_{(TBint)}$			3 V		10	

(1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It might be set with trigger signals shorter than $t_{(int)}$.

5.7 Leakage Current – Ports P1 to P6(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current, Port Px	V(Px.y)(2)	V_{CC} = 2.2 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The port pin must be selected as input.

5.8 Outputs – Ports P1 to P6

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)} = –1.5$ mA, $V_{CC} = 2.2$ V (1)	$V_{CC} – 0.25$	V_{CC}	V
		$I_{OH(max)} = –6$ mA, $V_{CC} = 2.2$ V (2)	$V_{CC} – 0.6$	V_{CC}	
		$I_{OH(max)} = –1.5$ mA, $V_{CC} = 3$ V (1)	$V_{CC} – 0.25$	V_{CC}	
		$I_{OH(max)} = –6$ mA, $V_{CC} = 3$ V (2)	$V_{CC} – 0.6$	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)} = 1.5$ mA, $V_{CC} = 2.2$ V (1)	V_{SS}	$V_{SS} + 0.25$	V
		$I_{OL(max)} = 6$ mA, $V_{CC} = 2.2$ V (2)	V_{SS}	$V_{SS} + 0.6$	
		$I_{OL(max)} = 1.5$ mA, $V_{CC} = 3$ V (1)	V_{SS}	$V_{SS} + 0.25$	
		$I_{OL(max)} = 6$ mA, $V_{CC} = 3$ V (2)	V_{SS}	$V_{SS} + 0.6$	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.

(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

5.9 Output Frequency

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	$(1 \le \times \le 6, 0 \le y \le 7)$	$C_L = 20$ F, $I_L = ±1.5$ mA	$V_{CC} = 2.2$ V, 3 V	dc		$f_{(System)}$	MHz
$f_{(MCLK)}$ $f_{(SMCLK)}$ $f_{(ACLK)}$	P1.1/TA0/MCLK P1.4/TBCLK/SMCLK P1.5/TACLK/ACLK	$C_L = 20$ pF				$f_{(System)}$	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK, $C_L = 20$ pF, $V_{CC} = 2.2$ V, 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, $C_L = 20$ pF, $V_{CC} = 2.2$ V, 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50% – 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, $C_L = 20$ pF, $V_{CC} = 2.2$ V, 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50% – 15 ns	50%	50%+ 15 ns	

5.10 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

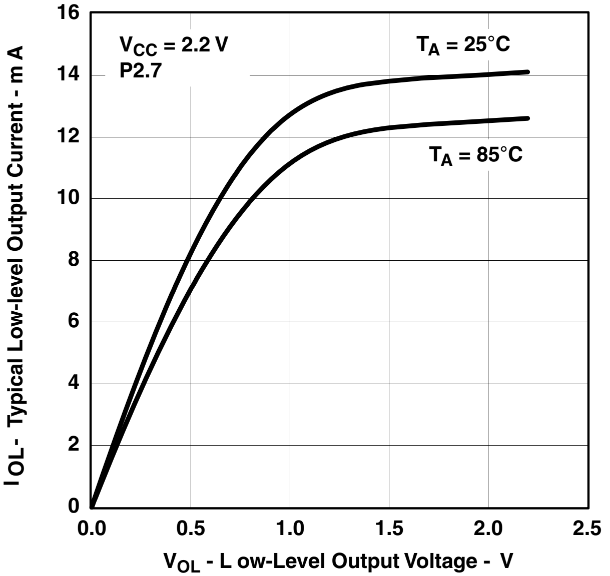


Figure 5-2. Typical Low-Level Output Current vs Typical Low-Level Output Current

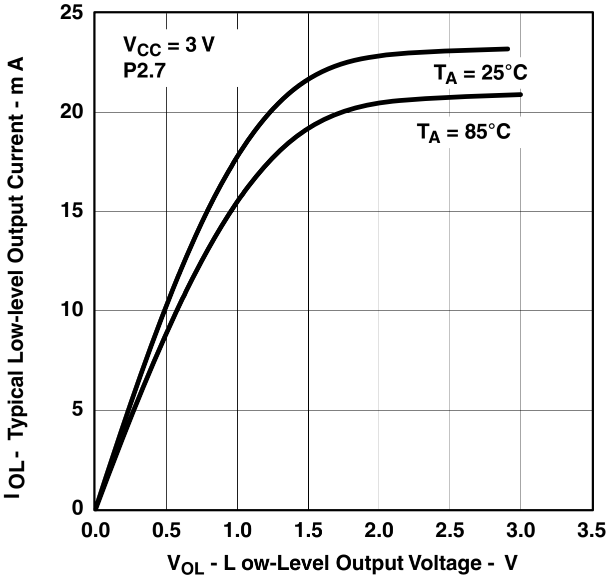


Figure 5-3. Typical Low-Level Output Current vs Typical Low-Level Output Current

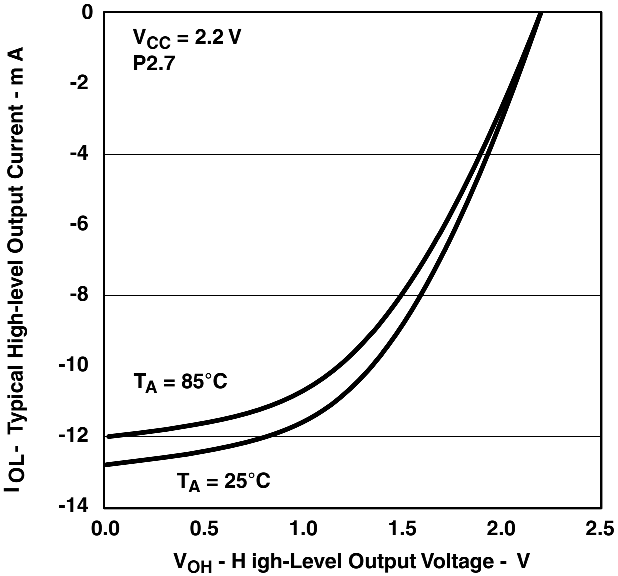


Figure 5-4. Typical High-Level Output Current vs Typical High-Level Output Current

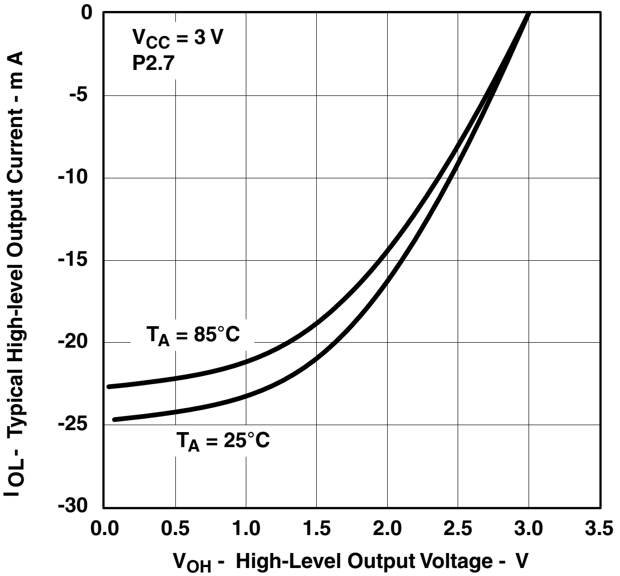


Figure 5-5. Typical High-Level Output Current vs Typical High-Level Output Current

5.11 Wake-Up From LPM3

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V, 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

5.12 RAM

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{RAMh}	CPU halted(1)	1.6		V

(1) This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.13 LCD

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} + 0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$[V_{(33)} - V_{(03)}] \times 2/3 + V_{(03)}$		
$V_{(13)}$		Voltage at P5.5/R13			$[V_{(33)} - V_{(03)}] \times 1/3 + V_{(03)}$		
$V_{(33)}$-$V_{(03)}$		Voltage at R33 to R03		2.5		V_{CC} + 0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = $V_{CC}/3$				±20	
$I_{(R23)}$		P5.6/R23 = 2 × $V_{CC}/3$				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = −3 µA, V_{CC} = 3 V		$V_{(03)}$		$V_{(03)}$ - 1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ - 1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ - 1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ - 1	

5.14 Comparator_A[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = (1,2,3), No load at P1.6/CA0 and P1.7/CA1	2.2 V		30	50	µA
			3 V		45	71	
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	(Voltage at 0.55 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 5-6 and Figure 5-7	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V, 3 V	0		V_{CC} –1	V
$V_p – V_S$	Offset voltage	See [2]	2.2 V, 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	160	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	

(1) The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

5.15 Comparator_A Typical Characteristics

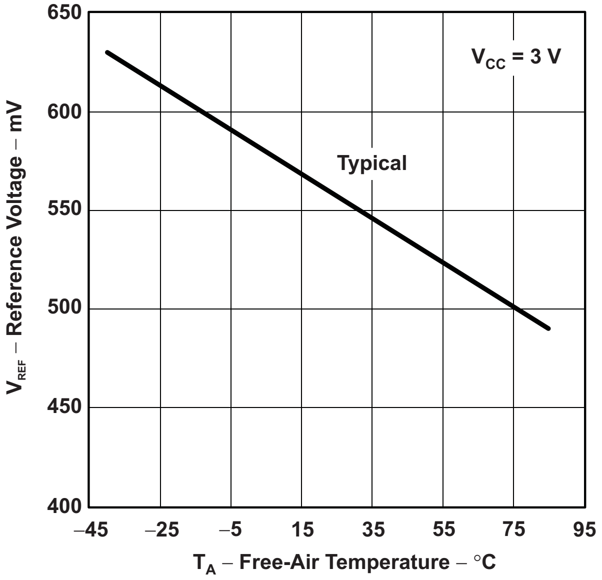


Figure 5-6. Reference Voltage vs Free-Air Temperature

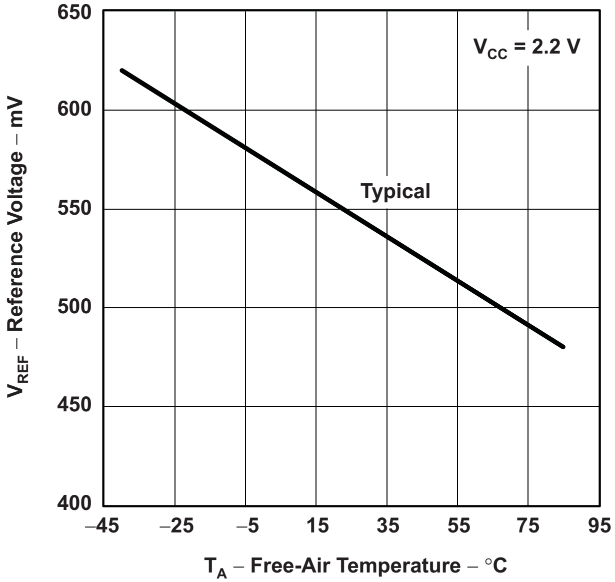


Figure 5-7. Reference Voltage vs Free-Air Temperature

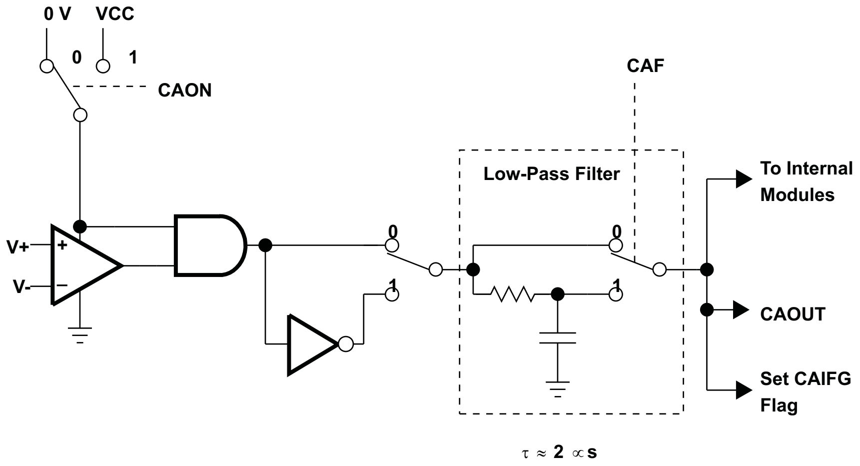


Figure 5-8. Block Diagram of Comparator_A Module

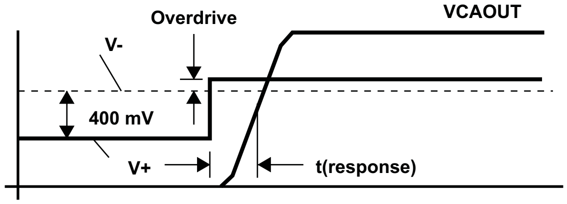


Figure 5-9. Overdrive Definition

5.16 Power-On Reset (POR) and Brownout Reset (BOR)[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout[2]				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-10 through Figure 5-12)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 5-10)	70	130	210	mV
$t_{(reset)}$		Pulse length needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V, 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

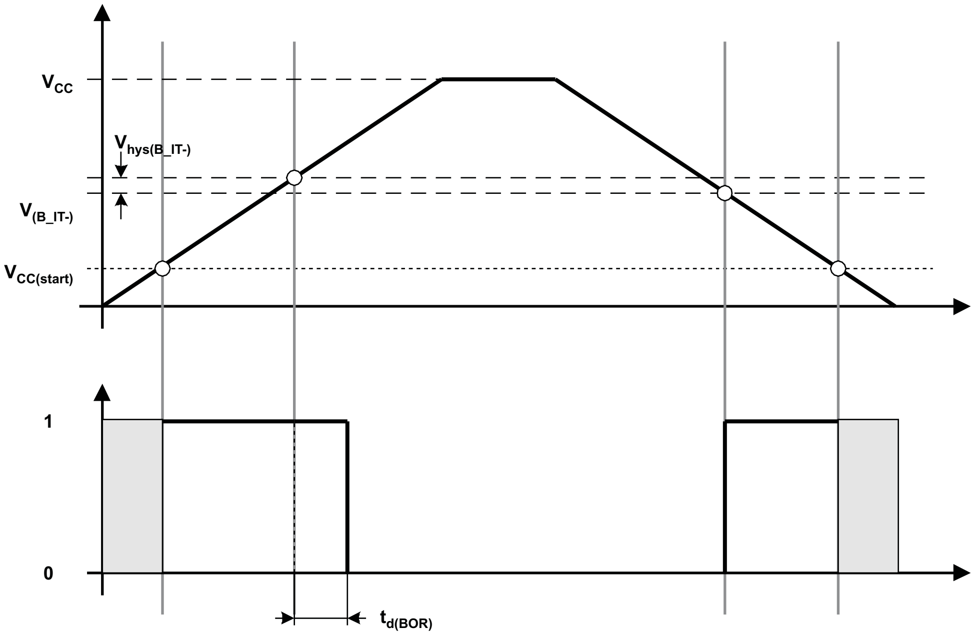


Figure 5-10. POR and BOR vs Supply Voltage

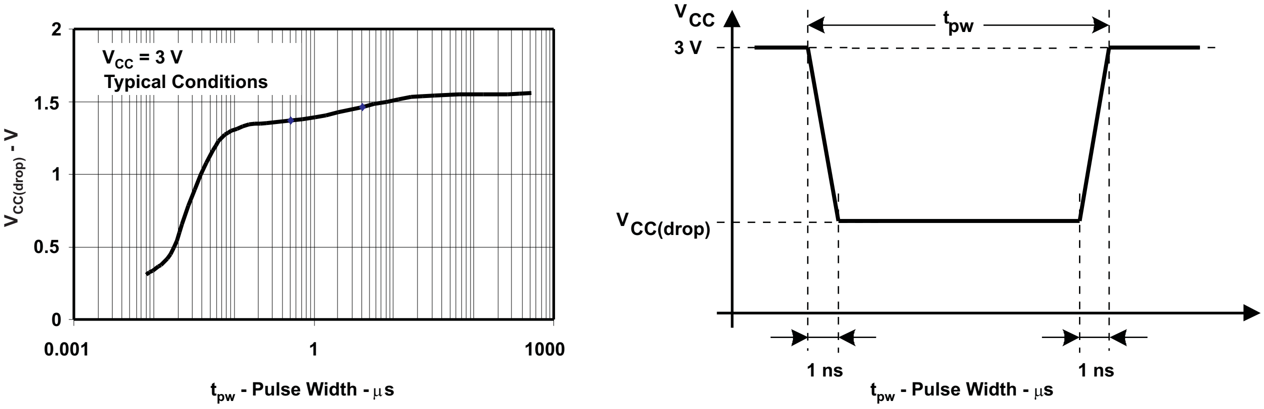


Figure 5-11. $V_{CC(drop)}$ Level with a Square Voltage Drop to Generate a POR or BOR Signal

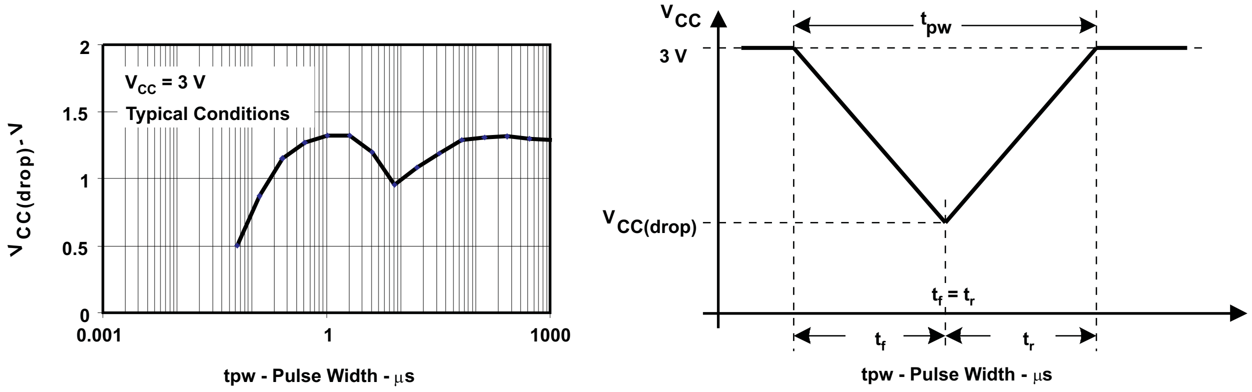


Figure 5-12. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

5.17 Supply Voltage Supervisor (SVS) and Supply Voltage Monitor (SVM)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 5-13)		5		150	µs
	dV_{CC}/dt ≤ 30 V/ms				2000	
$t_{d(SVSon)}$	SVS on, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0[1]				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 5-13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-13)	VLD = 1	70	120	155	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)}$ × 0.001		$V_{(SVS\_IT-)}$ × 0.016	
	V_{CC}/dt ≤ 3 V/s (see Figure 5-13), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.23	
		VLD = 3	2.05	2.2	2.35	
		VLD = 4	2.14	2.3	2.46	
		VLD = 5	2.24	2.4	2.58	
		VLD = 6	2.33	2.5	2.69	
		VLD = 7	2.46	2.65	2.84	
		VLD = 8	2.58	2.8	2.97	
		VLD = 9	2.69	2.9	3.10	
		VLD = 10	2.83	3.05	3.26	
		VLD = 11	2.94	3.2	3.39	
		VLD = 12	3.11	3.35	3.58[2]	
		VLD = 13	3.24	3.5	3.73[2]	
		VLD = 14	3.43	3.7[2]	3.96[2]	
	V_{CC}/dt ≤ 3 V/s (see Figure 5-13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$[3]	VLD ≠ 0, V_{CC} = 2.2 V, 3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

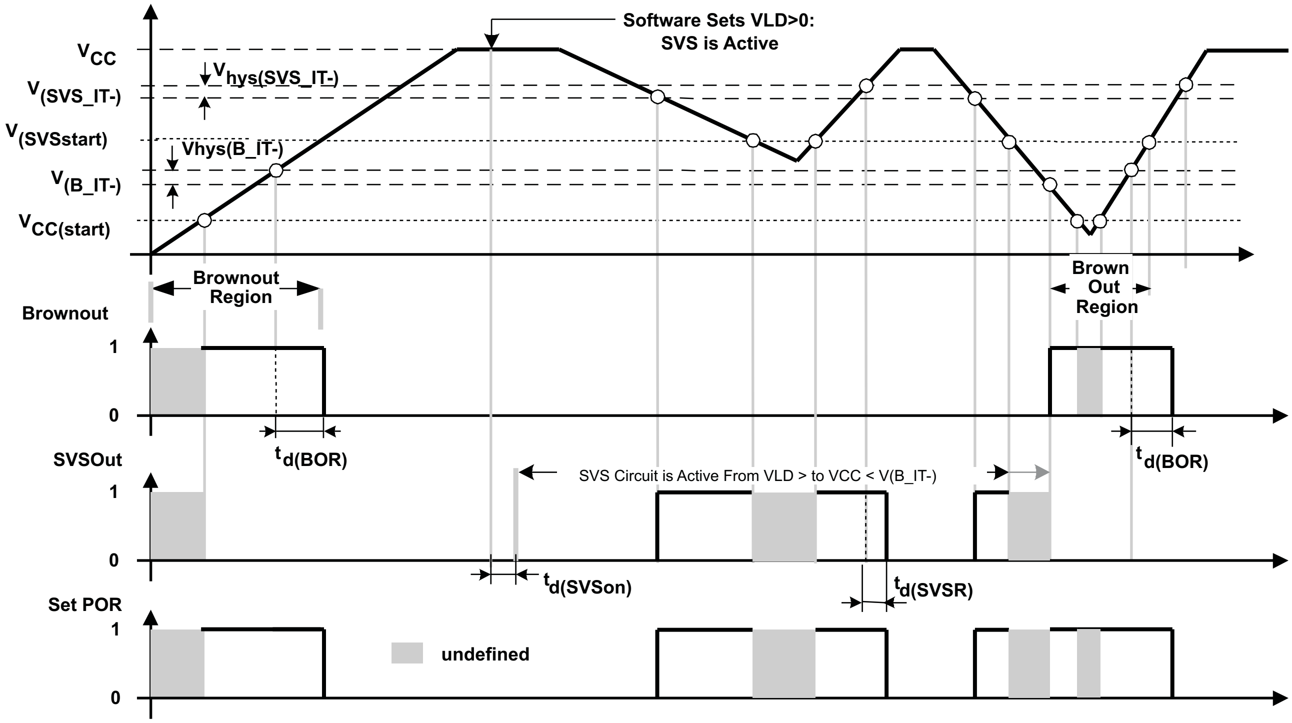


Figure 5-13. SVS Reset (SVSR) vs Supply Voltage

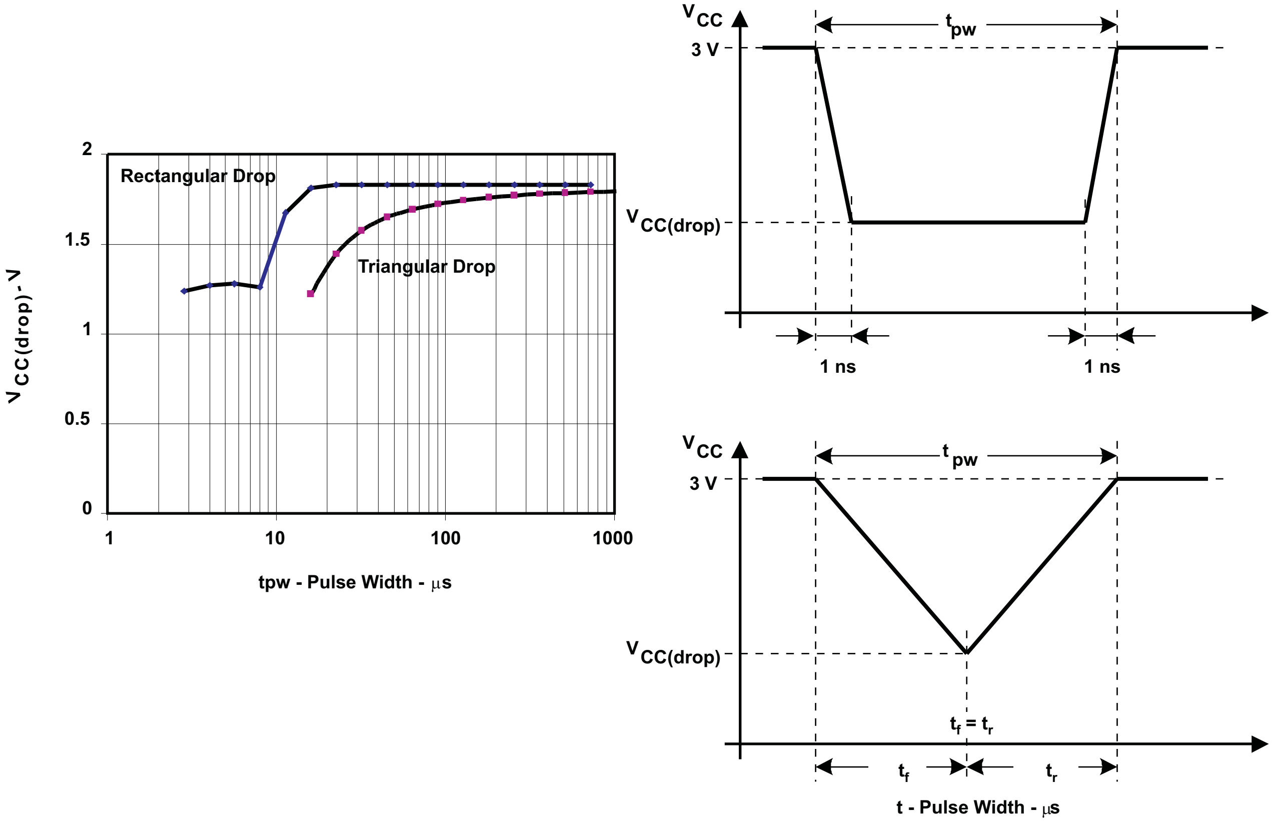


Figure 5-14. $V_{CC(drop)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

5.18 DCO

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0, $f_{Crystal}$ = 32.738 kHz	2.2 V, 3 V		1		MHz
$f_{(DCO=2)}$	FN_8=FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO=27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO=2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO=27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 1, DCOPLUS = 1	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO=2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO=27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO=2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO=27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO=2)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO=27)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$ (see Figure 5-16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01Eh, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V, 3 V	0	5	15	%/V

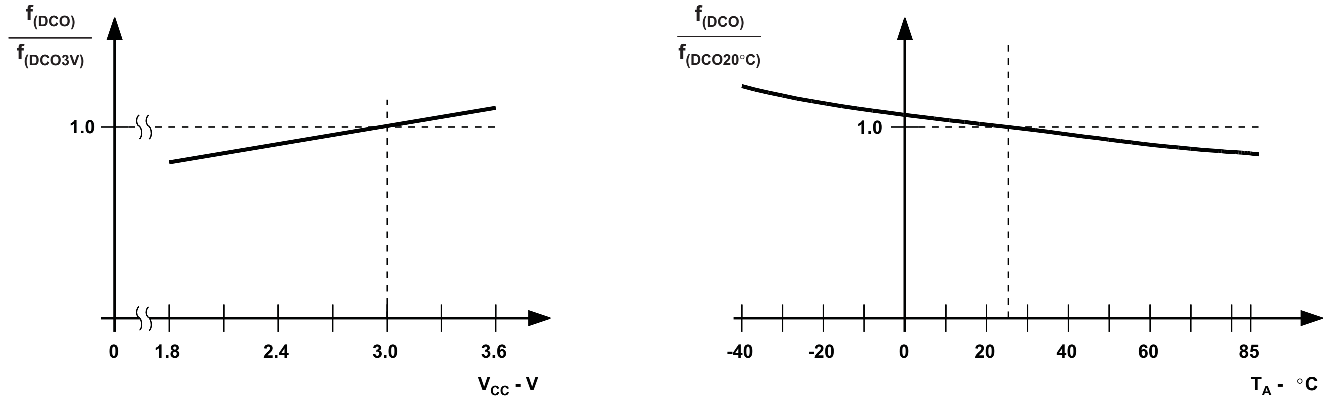


Figure 5-15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

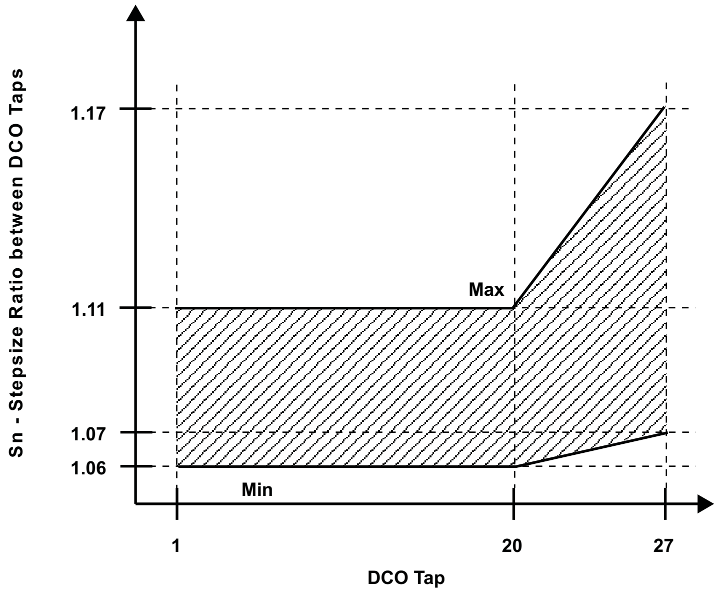


Figure 5-16. DCO Tap Step Size

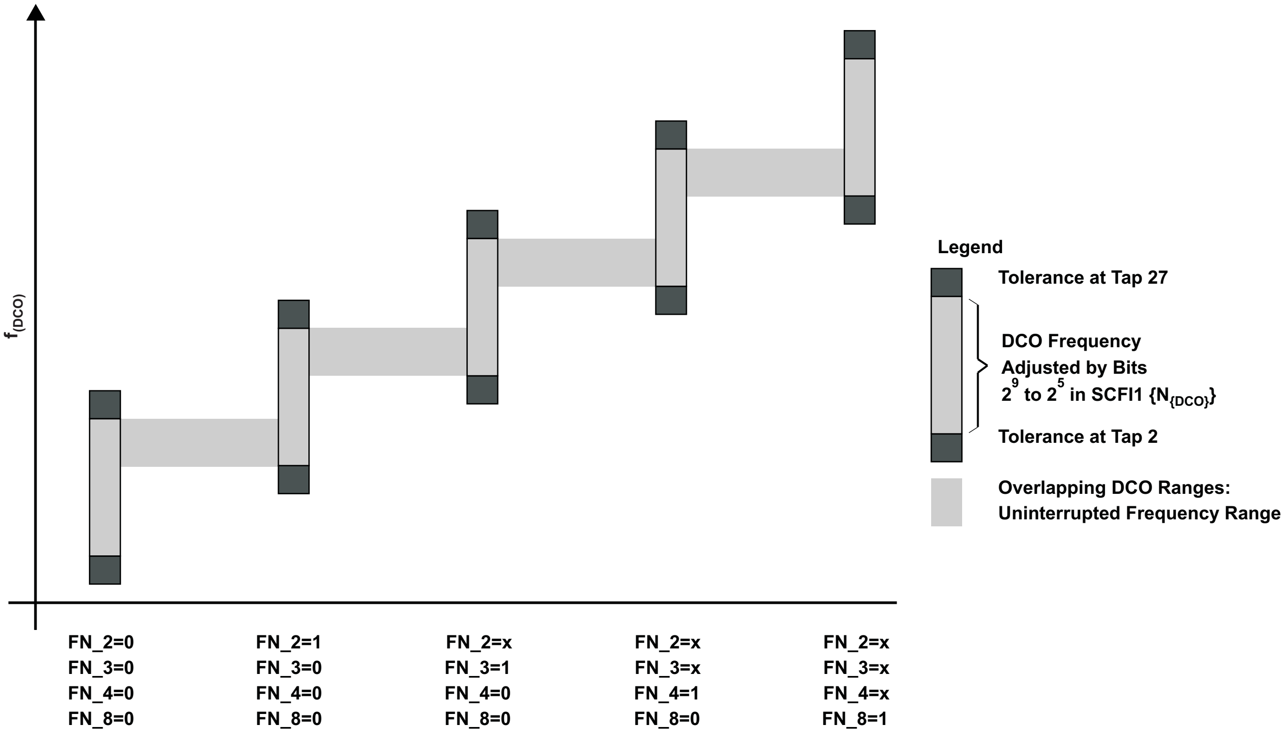


Figure 5-17. Five Overlapping DCO Ranges Controlled by FN_x Bits

5.19 Crystal Oscillator, XT1 Oscillator(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance(3)	OSCCAPx = 0h, V_{CC} = 2.2 V, 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V, 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V, 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V, 3 V		18		
C_{XOUT}	Integrated output capacitance(3)	OSCCAPx = 0h, V_{CC} = 2.2 V, 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V, 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V, 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V, 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V, 3 V(4)	V_{SS}		0.2 × V_{CC}	V
V_{IH}			0.8 × V_{CC}		V_{CC}	

(1) The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is (C_{XIN} × C_{XOUT}) / (C_{XIN}+ C_{XOUT}). This is independent of XTS_FLL.
(2) To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
  - Keep the trace between the device and the crystal as short as possible.
  - Design a good ground plane around the oscillator pins.
  - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
  - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
(3) External capacitance is recommended for precision real-time clock applications, OSCCAPx = 0h.
(4) Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.

5.20 Crystal Oscillator, XT2 Oscillator(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XT2IN}	Integrated input capacitance	V_{CC} = 2.2 V, 3 V		2		pF
C_{XT2OUT}	Integrated output capacitance	V_{CC} = 2.2 V, 3 V		2		pF
V_{IL}	Input levels at XT2IN	V_{CC} = 2.2 V, 3 V(2)	V_{SS}		0.2 × V_{CC}	V
V_{IH}			0.8 × V_{CC}		V_{CC}	V

(1) The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
(2) Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

5.21 USART0(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART0 deglitch time	V_{CC} = 2.2 V, SYNC = 0, UART mode	200	430	800	ns
		V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	

(1) The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

5.22 12-Bit ADC, Power Supply and Input Range Conditions(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range(2)	All external Ax terminals, Analog inputs selected in ADC12MCTLx register and P6Sel.x = 1, $V_{(AVSS)} \le V_{Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into the AVCC terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	V_{CC} = 2.2 V		0.65	1.3	mA
			V_{CC} = 3 V		0.8	1.6	
I_{REF+}	Operating supply current into the AVCC terminal(4)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	V_{CC} = 3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0 REFON = 1, REF2_5V = 0	V_{CC} = 2.2 V		0.5	0.8	mA
			V_{CC} = 3 V		0.5	0.8	
C_I	Input capacitance	Only one terminal can be selected at one time, Ax	V_{CC} = 2.2 V			40	pF
R_I	Input MUX ON resistance	$0\text{ V} \le V_{Ax} \le V_{AVCC}$	V_{CC} = 3 V			2000	Ω

(1) The leakage current is defined in the leakage current table with Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

5.23 12-Bit ADC, External Reference(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		0		1.2	V
(V_{eREF+} – V_{REF-}/V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (4)		1.4		V_{AVCC}	V
I_{VeREF+}	Static input current	$0\text{ V} \le V_{eREF+} \le V_{AVCC}$	V_{CC} = 2.2 V, 3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0\text{ V} \le V_{eREF-} \le V_{AVCC}$	V_{CC} = 2.2 V, 3 V			±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

5.24 12-Bit ADC, Built-In Reference

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built in reference voltage output	REF2_5V = 1 for 2.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	2.2 V, 3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built in reference active	REF2_5V = 0, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min		2.2			V
		REF2_5V = 1, I_{VREF+}min ≥ I_{VREF+} ≥ –0.5 mA		2.8			
		REF2_5V = 1, I_{VREF+}min ≥ I_{VREF+} ≥ – 1 mA		2.9			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V	0.01		–1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$	Load current regulation, V_{REF+} terminal	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, ax ≈ 0.5 × V_{REF+}, Error of conversion result ≤ 1 LSB	3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (1)	REFON =1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	2.2 V, 3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA	2.2 V, 3 V			±100	ppm/°C
t_{REFON}	Settle time of internal reference voltage (see Figure 5-18) (2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

(1) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.

(2) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

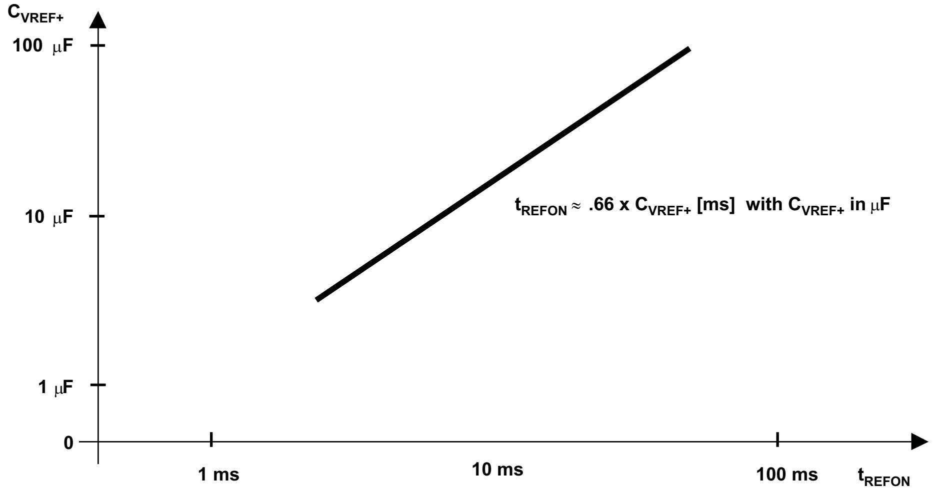


Figure 5-18. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

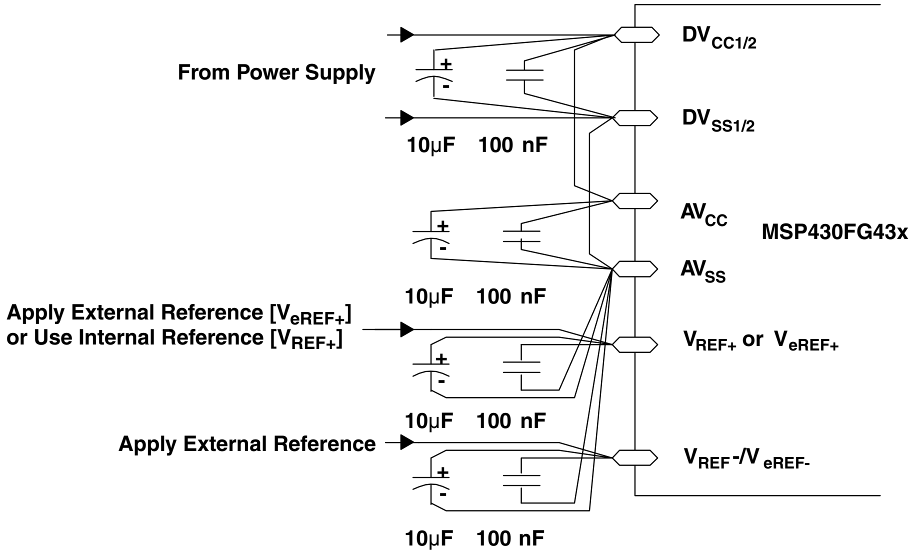


Figure 5-19. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

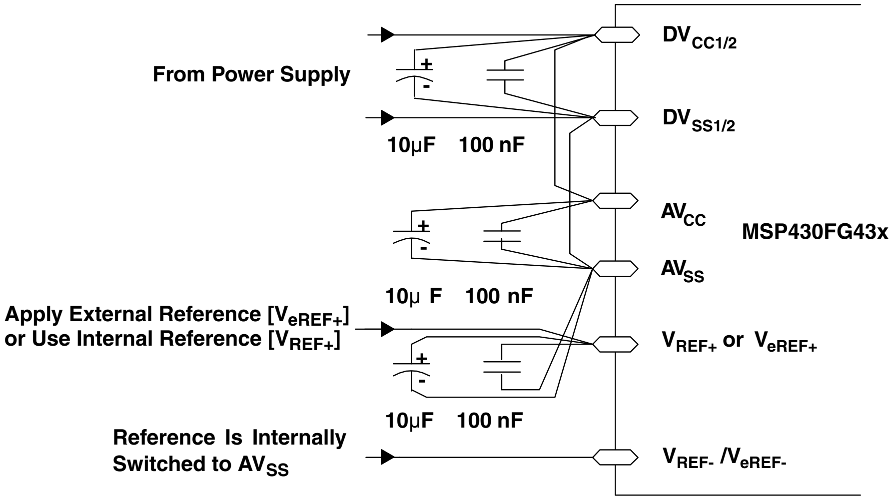


Figure 5-20. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} = AV_{SS}, Internally Connected

5.25 12-Bit ADC, Timing Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC12 clock frequency	For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V, 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			13 × ADC12DIV × $1/f_{ADC12CLK}$		µs
$t_{ADC12ON}$	Turn on settling time of the ADC	See (1)				100	ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (2)	3 V	1220			ns
			2.2 V	1400			

(1) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

(2) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance.

5.26 12-Bit ADC, Linearity Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	$1.4\text{ V} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})\text{ min} \leq 1.6\text{ V}$	2.2 V, 3 V			±2	LSB
		$1.6\text{ V} < (V_{eREF+} - V_{REF-}/V_{eREF-})\text{ min} \leq V_{AVCC}$				±1.7	
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})\text{ min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V			±1	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})\text{ min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, Internal impedance of source RS < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±4	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF-}/V_{eREF-})\text{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} =10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	$(V_{eREF+} - V_{REF-}/V_{eREF-}\ )\text{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±5	LSB

5.27 12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal(1)	REFON = 0, INCH = 0Ah, ADC12ON = NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}	See (2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V, 3 V		986		mV
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V, 3 V		3.55 ± 3%		mV/°C
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11(4)	ADC12ON = 1, INCH = 0Bh	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V		1.1	1.10 ± 0.04	V
			3 V		1.5	1.50 ± 0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(2) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

5.28 12-Bit DAC, Supply Specifications

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS}$ = 0 V		2.2		3.6	V
I_{DD}	Supply current, single DAC channel(1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0800h	2.2 V, 3 V		50	110	µA
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h , $V_{eREF+} = V_{REF+} = AV_{CC}$			50	110	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{eREF+} = V_{REF+} = AV_{CC}$			200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{eREF+} = V_{REF+} = AV_{CC}$			700	1500	
PSRR	Power-supply rejection ratio(3) (4)	DAC12_xDAT = 0800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100 mV	2.2 V		70		dB
		DAC12_xDAT = 0800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV	3 V				

(1) No load at the output pin, DAC0 or DAC1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1, current flows through the input divider (see Reference Input specifications).
(3) PSRR = 20 × log(ΔAV_{CC} / ΔV_{DAC12_xOUT}).
(4) V_{REF} is applied externally. The internal reference is not used.

5.29 12-Bit DAC, Linearity Specifications

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5-21)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic		12			bits
INL	Integral nonlinearity[1]	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2.0	±8.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
DNL	Differential nonlinearity[1]	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±0.4	±1.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
E_O	Offset voltage without calibration[1] [2]	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±21	mV
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
	Offset voltage with calibration[1] [2]	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±2.5	
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
$d_{E(O)}/d_T$	Offset error temperature coefficient[1]		2.2 V, 3 V		±30		µV/°C
E_G	Gain error[1]	V_{REF} = 1.5 V	2.2 V			±3.5	%FSR
		V_{REF} = 2.5 V	3 V				
$d_{E(G)}/d_T$	Gain temperature coefficient[1]		2.2 V, 3 V		10		ppm of FSR/°C
$t_{Offset\ Cal}$	Time for offset calibration[3]	DAC12AMPx = 2	2.2 V, 3 V			100	ms
		DAC12AMPx = 3, 5				32	
		DAC12AMPx = 4, 6, 7				6	

(1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: $y = a + b \times x$. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (V_{eREF+} / 4095) \times$ DAC12_xDAT, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON.
(3) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

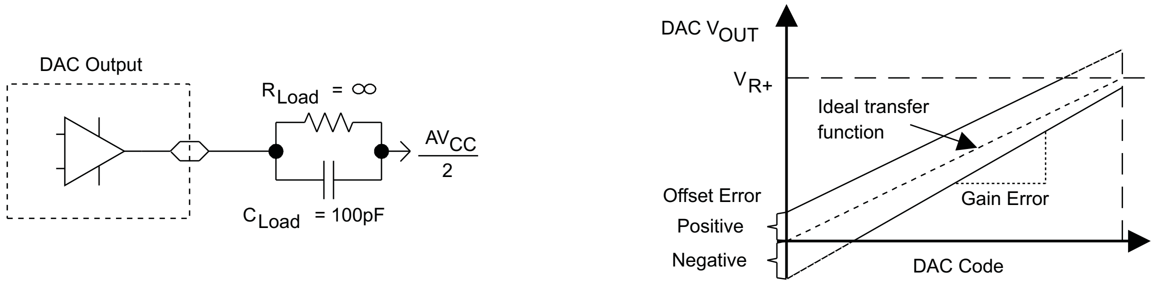


Figure 5-21. Linearity Test Load Conditions and Gain/Offset Definition

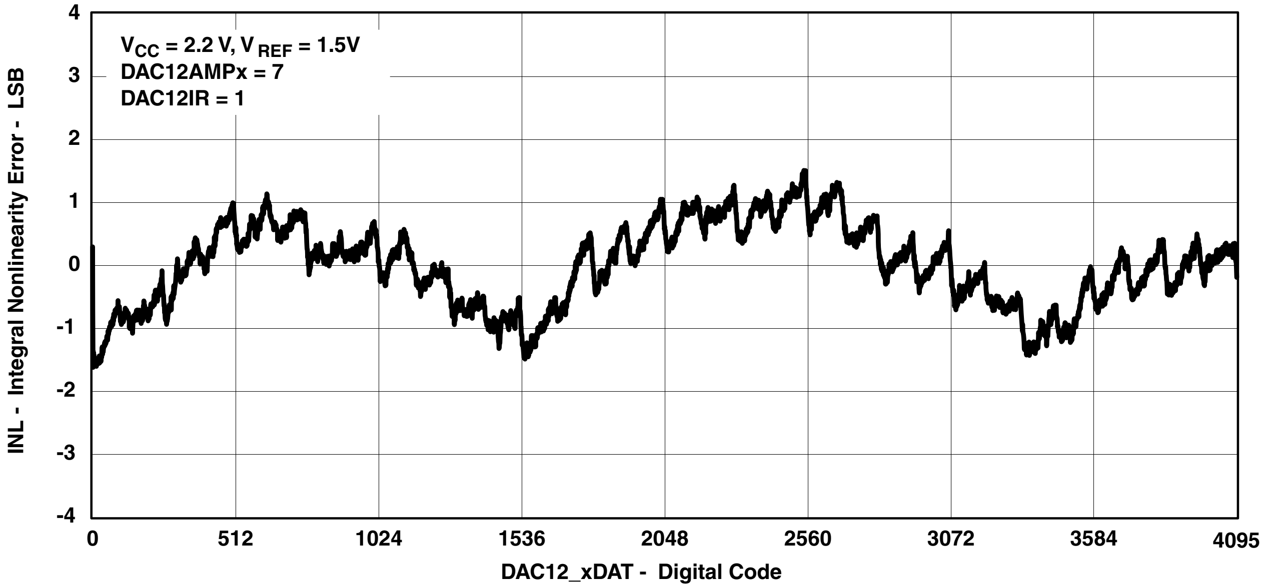


Figure 5-22. Typical INL Error vs Digital Input Data

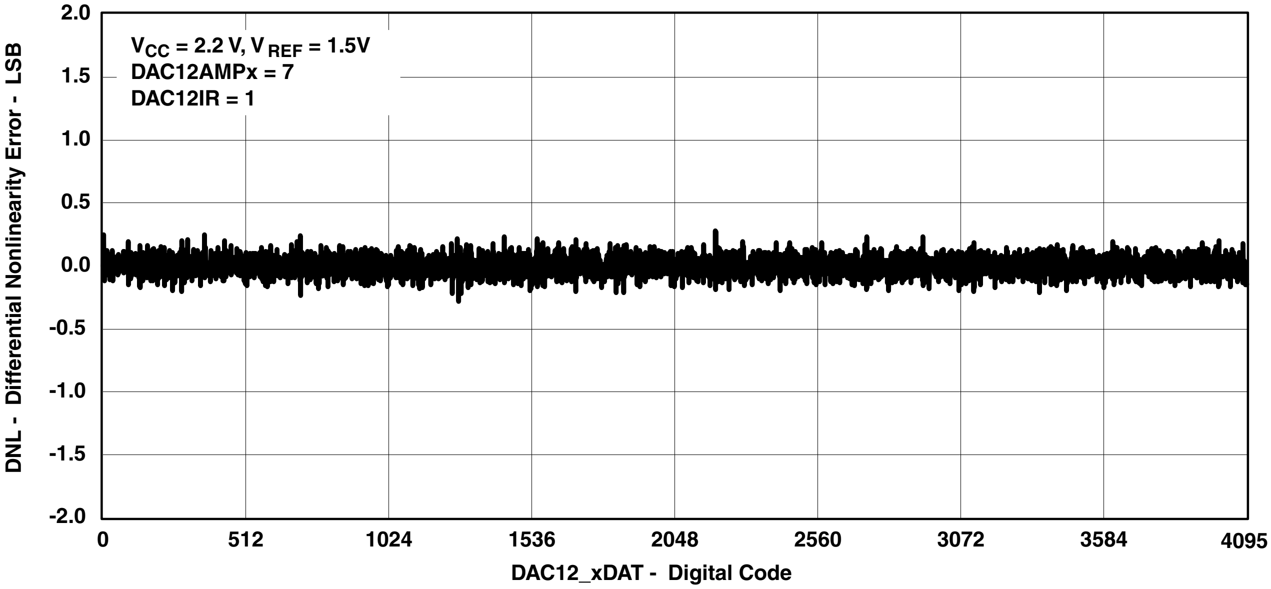


Figure 5-23. Typical DNL Error vs Digital Input Data

5.30 12-Bit DAC, Output Specifications

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range[1] (see Figure 5-24)	No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3 V	0		0.005	V
		No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.13		AV_{CC}	
$C_{L(DAC12)}$	Maximum DAC12 load capacitance		2.2 V, 3 V			100	pF
$I_{L(DAC12)}$	Maximum DAC12 load current		2.2 V	–0.5		+0.5	mA
			3 V	–1.0		+1.0	
$R_{O/P(DAC12)}$	Output resistance (see Figure 5-24)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)} < 0.3$ V, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} > AV_{CC} - 0.3$ V, DAC12AMPx = 7, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, $0.3\ V \le V_{O/P(DAC12)} \le AV_{CC} - 0.3\ V$ DAC12AMPx = 7			1	4	

(1) Data is valid after the offset calibration of the output amplifier.

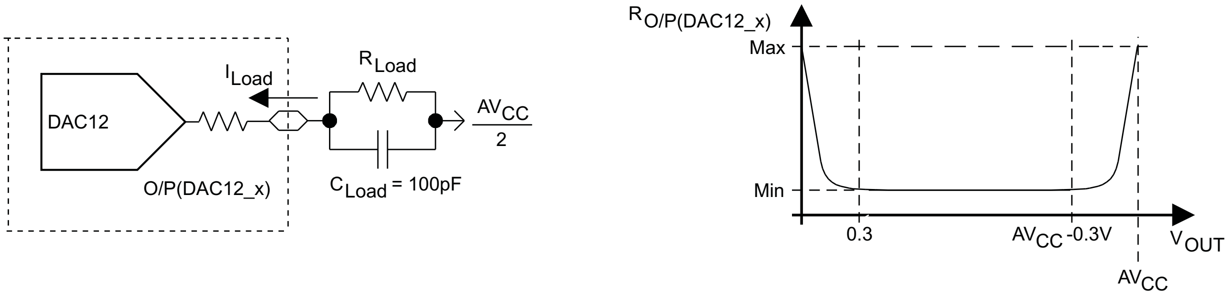


Figure 5-24. DAC12_x Output Resistance Tests

5.31 12-Bit DAC, Reference Input Specifications

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Ve_{REF+}	Reference input voltage range	DAC12IR = 0 (1) (2)	2.2 V, 3 V		AV_{CC} / 3	AV_{CC} + 0.2	V
		DAC12IR = 1 (3) (4)			AV_{CC}	AV_{CC} + 0.2	
$Ri_{(VREF+)}$, $(Ri_{(VeREF+)}$	Reference input resistance	DAC12_0 IR = DAC12_1 IR = 0	2.2 V, 3 V	20			MΩ
		DAC12_0 IR = 1, DAC12_1 IR = 0		40	48	56	kΩ
		DAC12_0 IR = 0, DAC12_1 IR = 1		40	48	56	
		DAC12_0 IR = DAC12_1 IR =1, DAC12_0 SREFx = DAC12_1 SREFx (5)		20	24	28	

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
(2) The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} – V_{E(O)}] / [3 × (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
(4) The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} – V_{E(O)}] / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel, reducing the reference input resistance.

5.32 12-Bit DAC, Dynamic Specifications

$V_{ref} = V_{CC}$, DAC12IR = 1, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5-25 and Figure 5-26)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (1) (see Figure 5-25)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h→F7Fh→80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3, 5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C–C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→408h→3F8h BF8h→C08h→BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3, 5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate	DAC12_xDAT = 80h→ F7Fh→ 80h (2)	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.12		V/µs
			DAC12AMPx = 3, 5		0.35	0.7		
			DAC12AMPx = 4, 6, 7		1.5	2.7		
	Glitch energy, full scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx = 2	2.2 V, 3 V		10		nV-s
			DAC12AMPx = 3, 5			10		
			DAC12AMPx = 4, 6, 7			10		

(1) R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 5-25.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

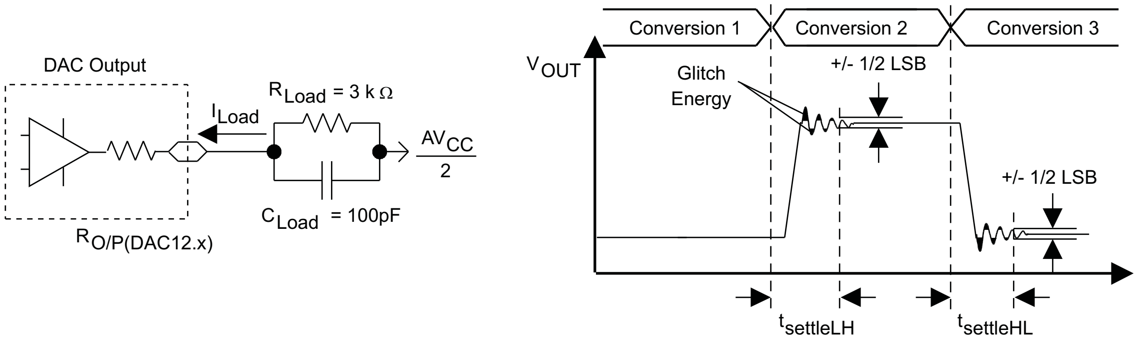


Figure 5-25. Settling Time and Glitch Energy Testing

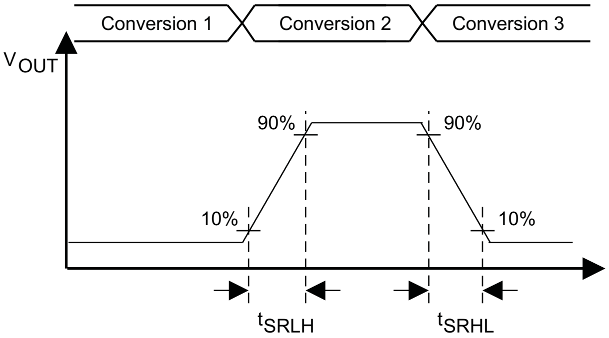


Figure 5-26. Slew Rate Testing

5.33 12-Bit DAC, Dynamic Specifications (Continued)

T_A = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 VPP (see Figure 5-27)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V, 3 V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550			
	Channel-to-channel crosstalk(1) (see Figure 5-28)	DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h↔F7Fh, R_{Load} = 3 kΩ f_{DAC12_1OUT} = 10 kHz with 50/50 duty cycle	2.2 V, 3 V		–80		dB
		DAC12_0DAT = 80h↔F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No Load, f_{DAC12_0OUT} = 10 kHz with 50/50 duty cycle			–80		

(1) R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

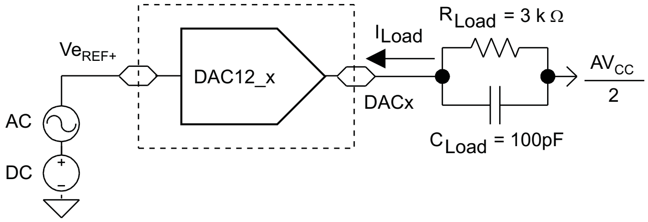


Figure 5-27. Test Conditions for 3-dB Bandwidth Specification

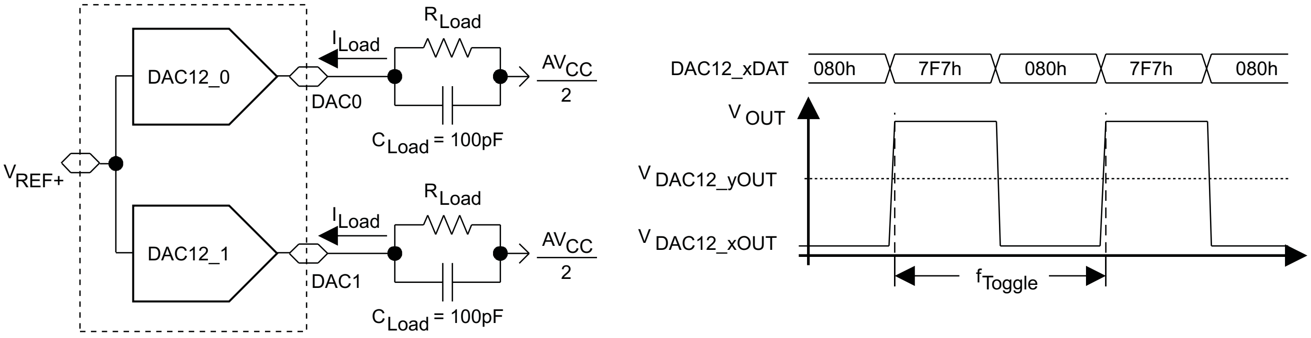


Figure 5-28. Crosstalk Test Conditions

5.34 Operational Amplifier (OA), Supply Specifications

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			2.2		3.6	V
I_{CC}	Supply current(1)	Fast Mode, RRIP OFF	2.2 V, 3 V		180	290	µA
		Medium Mode, RRIP OFF			110	190	
		Slow Mode, RRIP OFF			50	80	
		Fast Mode, RRIP ON			300	490	
		Medium Mode, RRIP ON			190	350	
		Slow Mode, RRIP ON			90	190	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V, 3 V		70		dB

(1) P6SEL.x = 1 for each corresponding pin when used in OA input or OA output mode.

5.35 Operational Amplifier (OA), Input/Output Specifications

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Voltage supply, I/P	RRIP OFF			–0.1		V_{CC} – 1.2	V
		RRIP ON			–0.1		V_{CC} + 0.1	
I_{lkg}	Input leakage current, I/P(1) (2)	T_A = –40°C to +55°C			–5	±0.5	5	nA
		T_A = +55°C to +85°C			–20	±5	20	
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz			50		nV/√Hz
		Medium Mode				80		
		Slow Mode				140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium Mode				50		
		Slow Mode				65		
V_{IO}	Offset voltage, I/P			2.2 V, 3 V			±10	mV
	Offset temperature drift, I/P	See (3)		2.2 V, 3 V		±10		µV/°C
	Offset voltage drift with supply, I/P	0.3 V ≤ V_{IN} ≤ V_{CC} – 0.3 V ΔV_{CC} ≤ ±10%, T_A = 25°C		2.2 V, 3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ –500 µA		2.2 V	V_{CC} – 0.2		V_{CC}	V
		Slow Mode, I_{SOURCE} ≤ –150 µA		3 V	V_{CC} – 0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500 µA		2.2 V	V_{SS}		0.2	V
		Slow Mode, I_{SOURCE} ≤ +150 µA		3 V	V_{SS}		0.1	
$R_{O/P\ (OAx)}$	Output resistance(4) (see Figure 5-29)	R_{Load} = 3 kΩ,C_{Load} = 50 pF, RRIP ON, $V_{O/P(OAx)}$ < 0.2 V		2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ,C_{Load} = 50 pF, RRIP ON, $V_{O/P(OAx)}$ > AV_{CC} – 0.2 V				150	250	
		R_{Load} = 3 kΩ,C_{Load} = 50 pF, RRIP ON, 0.2 V ≤ $V_{O/P(OAx)}$ ≤ AV_{CC} – 0.2 V				0.1	4	
CMRR	Common-mode rejection ratio	Non-inverting		2.2 V, 3 V		70		dB

(1) ESD damage can degrade input current leakage.
(2) The input bias current is overridden by the input leakage current.
(3) Calculated using the box method.
(4) Specification valid for voltage-follower OAx configuration.

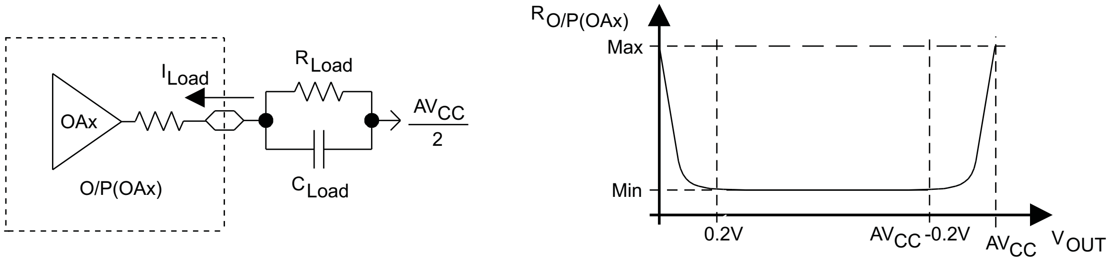


Figure 5-29. OAx Output Resistance Tests

5.36 Operational Amplifier (OA), Dynamic Specifications

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode			1.2		V/µs
		Medium Mode			0.8		
		Slow Mode			0.3		
	Open-loop voltage gain				100		dB
φ_m	Phase margin	C_L = 50 pF			60		deg
	Gain margin	C_L = 50 pF			20		dB
GBW	Gain-bandwidth product (see Figure 5-30 and Figure 5-31)	Non-inverting, Fast Mode, R_L = 47 kΩ,C_L = 50 pF	2.2 V, 3 V		2.2		MHz
					1.4		
		Non-inverting, Medium Mode, R_L = 300 kΩ, C_L = 50 pF					
		Non-inverting, Slow Mode, R_L = 300 kΩ, C_L = 50 pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, non-inverting, Gain = 1	2.2 V, 3 V		10	20	µs
$t_{en(off)}$	Enable time off		2.2 V, 3 V			1	µs

5.37 OA Dynamic Specifications Typical Characteristics

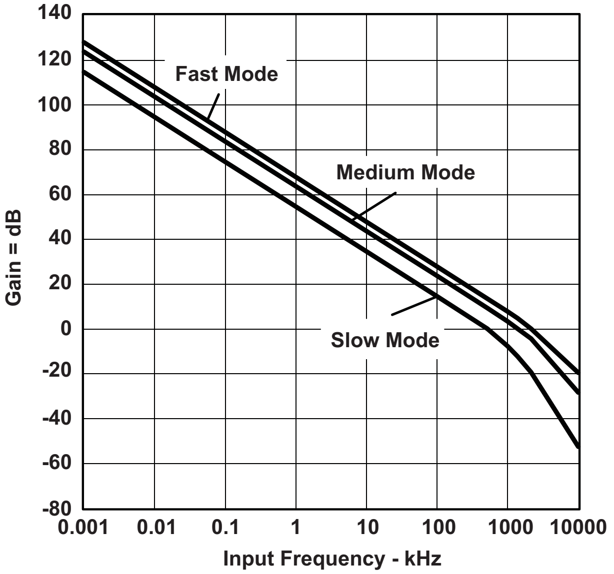


Figure 5-30. Typical Open-Loop Gain vs Frequency

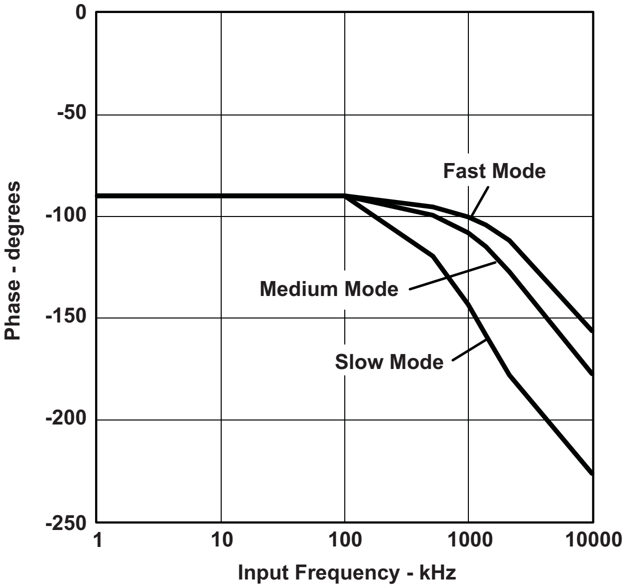


Figure 5-31. Typical Phase vs Frequency

5.38 Flash Memory

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/\ ERASE)}$	Program and erase supply voltage			2.7		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V, 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V, 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	See (1)	2.7 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time	See (2)	2.7 V, 3.6 V	200			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See (3)			35		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word				30		
$t_{Block,\ 1\text{-}63}$	Block program time for each additional byte or word				21		
$t_{Block,\ End}$	Block program end-sequence wait time				6		
$t_{Mass\ Erase}$	Mass erase time				5297		
$t_{Seg\ Erase}$	Segment erase time				4819		

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

(2) The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297 × $1/f_{FTG,max}$ = 5297 × 1 / 476 kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).

(3) These values are hard-wired into the flash controller's state machine ($t_{FTG} = 1 / f_{FTG}$).

5.39 JTAG Interface

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	See (1)	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	See (2)	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

(2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

5.40 JTAG Fuse(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	**PC/R0**
Stack Pointer	**SP/R1**
Status Register	**SR/CG1/R2**
Constant Generator	**CG2/R3**
General-Purpose Register	**R4**
General-Purpose Register	**R5**
General-Purpose Register	**R6**
General-Purpose Register	**R7**
General-Purpose Register	**R8**
General-Purpose Register	**R9**
General-Purpose Register	**R10**
General-Purpose Register	**R11**
General-Purpose Register	**R12**
General-Purpose Register	**R13**
General-Purpose Register	**R14**
General-Purpose Register	**R15**

6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 shows examples of the three types of instruction formats; Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC→(TOS), R8 →PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S (1)	D (1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)→ M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2→ R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source D = destination

6.3 Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL+ loop control is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-3. Interrupt Sources, Flags, and Vectors of MSP430FG43x Configurations

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (1) OFIFG (1) ACCVIFG (1)	(Non)maskable (2) (Non)maskable (Non)maskable	0FFFCh	14
Timer_B3	TBCCR0 CCIFG0 (3)	Maskable	0FFFAh	13
Timer_B3	TBCCR1 CCIFG1 and TBCCR2 CCIFG2, TBIFG (1) (3)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
USART0 Receive	URXIFG0	Maskable	0FFF2h	9
USART0 Transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12	ADC12IFG (1) (3)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG0 (3)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (1) (3)	Maskable	0FFEAh	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (1) (3)	Maskable	0FFE8h	4
DAC12 DMA	DAC12.0IFG, DAC12.1IFG, DMA0IFG (1) (3)	Maskable	0FFE6h	3
			0FFE4h	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (1) (3)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

(1) Multiple source flags
(2) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.

6.5 Special Function Registers (SFRs)

The MSP430 SFRs are located in the lowest address space and are organized as byte-mode registers. SFRs should be accessed with byte instructions.

Legend	
rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), rw-1	Bit can be read and written. It is Reset or Set by POR.
▨	SFR bit is not present in device.

6.5.1 Interrupt Enable Registers 1 and 2

Figure 6-1. Interrupt Enable Register 1 (Address = 0h)

7	6	5	4	3	2	1	0
UTXIE0	URXIE0	ACCVIE	NMIIE	▨	▨	OFIE	WDTIE
rw–0	rw–0	rw–0	rw–0			rw–0	rw–0

Table 6-4. Interrupt Enable Register 1 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	UTXIE0	RW	0h	USART0: UART and SPI transmit-interrupt enable
6	URXIE0	RW	0h	USART0: UART and SPI receive-interrupt enable
5	ACCVIE	RW	0h	Flash access violation interrupt enable
4	NMIIE	RW	0h	Nonmaskable-interrupt enable
1	OFIE	RW	0h	Oscillator-fault-interrupt enable
0	WDTIE	RW	0h	Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

Figure 6-2. Interrupt Enable Register 2 (Address = 1h)

7	6	5	4	3	2	1	0
BTIE	▨	▨	▨	▨	▨	▨	▨
rw–0							

Table 6-5. Interrupt Enable Register 2 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BTIE	RW	0h	Basic timer interrupt enable

6.5.2 *Interrupt Flag Registers 1 and 2*

Figure 6-3. Interrupt Flag Register 1 (Address = 2h)

7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
rw–1	rw–0		rw–0			rw–1	rw–(0)

Table 6-6. Interrupt Flag Register 1 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	UTXIFG0	RW	1h	USART0: UART and SPI transmit flag
6	URXIFG0	RW	0h	USART0: UART and SPI receive flag
4	NMIIFG	RW	0h	Set by $\overline{\text{RST}}$/NMI pin
1	OFIFG	RW	1h	Flag set on oscillator fault
0	WDTIFG	RW	0h	Set on watchdog timer overflow (in watchdog mode) or security key violation Reset on V_{CC} power-on or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode

Figure 6-4. Interrupt Flag Register 2 (Address = 3h)

7	6	5	4	3	2	1	0
BTIFG							
rw–0							

Table 6-7. Interrupt Flag Register 2 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BTIFG	RW	0h	Basic timer flag

6.5.3 *Module Enable Registers 1 and 2*

Figure 6-5. Module Enable Register 1 (Address = 4h)

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0						
rw–0	rw–0						

Table 6-8. Module Enable Register 1 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	UTXE0	RW	0h	USART0: UART mode transmit enable
6	URXE0	RW	0h	USART0: UART mode receive enable
	USPIE0	RW	0h	USART0: SPI mode transmit and receive enable

Figure 6-6. Module Enable Register 2 (Address = 5h)

7	6	5	4	3	2	1	0

6.6 Memory Organization

Table 6-9 shows the memory organization for all device variants.

Table 6-9. Memory Organization

		MSP430FG437	MSP430FG438	MSP430FG439
Memory	Size	32KB	48KB	60KB
Main: interrupt vector	Flash	0FFFFh-0FFE0h	0FFFFh-0FFE0h	0FFFFh-0FFE0h
Main: code memory	Flash	0FFFFh-08000h	0FFFFh-04000h	0FFFFh-01100h
Information memory	Size	256 Byte	256 Byte	256 Byte
	Flash	010FFh-01000h	010FFh-01000h	010FFh-01000h
Boot memory	Size	1KB	1KB	1KB
	ROM	0FFFh-0C00h	0FFFh-0C00h	0FFFh-0C00h
RAM	Size	1KB	2KB	2KB
		05FFh-0200h	09FFh-0200h	09FFh-0200h
Peripherals	16-bit	01FFh-0100h	01FFh-0100h	01FFh-0100h
	8-bit	0FFh-010h	0FFh-010h	0FFh-010h
	8-bit SFR	0Fh-00h	0Fh-00h	0Fh-00h

6.7 Bootstrap Loader (BSL)

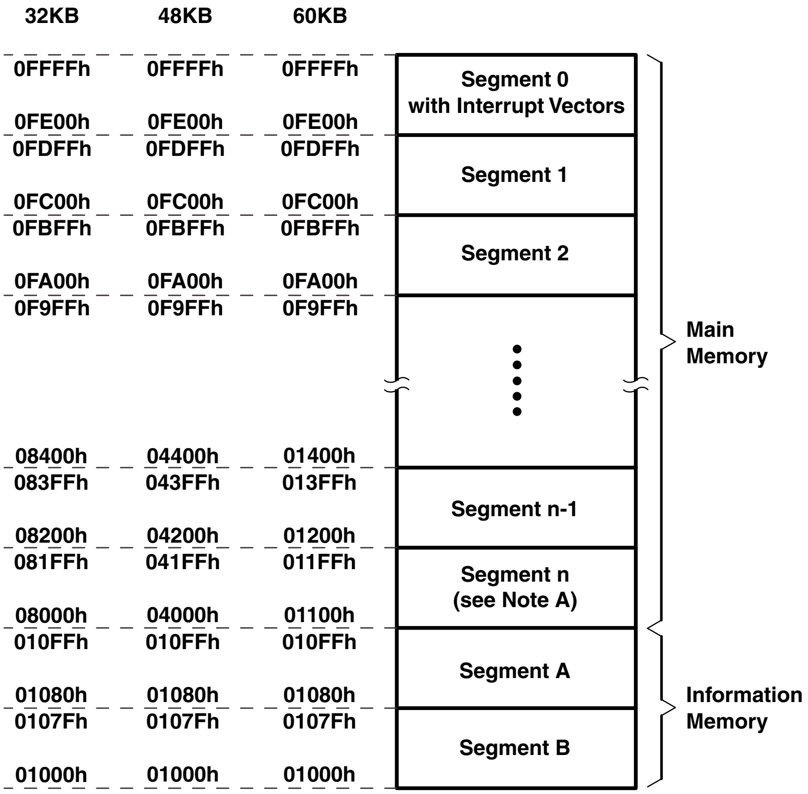
The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see *MSP430 Programming Via the Bootstrap Loader (BSL)* (SLAU319).

BSL FUNCTION	PN PACKAGE PINS	ZCA PACKAGE PINS
Data Transmit	67 – P1.0	D8 – P1.0
Data Receiver	66 – P1.1	D9 – P1.1

6.8 Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called information memory.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



A. MSP430FG43x flash segment n = 256 bytes.

Figure 6-7. Flash Memory Segments

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide* (SLAU056).

6.9.1 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

6.9.2 Oscillator and System Clock

The clock system in the MSP430FG43x family of devices is supported by the FLL+ module, which includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO), and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

6.9.3 Brownout, Supply Voltage Supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must make sure that the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.9.4 Digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions

6.9.5 Basic Timer1

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

6.9.6 LCD Drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

6.9.7 OA

The MSP430FG43x has three configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offers a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

6.9.8 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.9 USART0

The MSP430FG43x has one hardware universal synchronous/asynchronous receive transmit (USART) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

6.9.10 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. Timer_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
ZCA	PN					PN	ZCA
B10 - P1.5	62 - P1.5	TACLK	TACLK				
		ACLK	ACLK				
		SMCLK	SMCLK	Timer	NA		
B10 - P1.5	62 - P1.5	TACLK	INCLK				
D8 - P1.0	67 - P1.0	TA0	CCI0A			67 - P1.0	D8 - P1.0
D9 - P1.1	66 - P1.1	TA0	CCI0B				
		DVSS	GND	CCR0	TA0		
		DVCC	VCC				
B9 - P1.2	65 - P1.2	TA1	CCI1A			65 - P1.2	B9 - P1.2
		CAOUT (internal)	CCI1B			ADC12 (internal)	
		DVSS	GND	CCR1	TA1		
		DVCC	VCC				
C11 - P2.0	59 - P2.0	TA2	CCI2A			59 - P2.0	C11 - P2.0
		ACLK (internal)	CCI2B				
		DVSS	GND	CCR2	TA2		
		DVCC	VCC				

6.9.11 Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. Timer_B3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
ZCA	PN					PN	ZCA
E9 - P1.4	63 - P1.4	TBCLK	TBCLK				
		ACLK	ACLK				
		SMCLK	SMCLK	Timer	NA		
E9 - P1.4	63 - P1.4	TBCLK	INCLK				
D11 - P2.1	58 - P2.1	TB0	CCI0A			58 - P2.1	D11 - P2.1
D11 - P2.1	58 - P2.1	TB0	CCI0B			ADC12 (internal)	
		DVSS	GND	CCR0	TB0		
		DVCC	VCC				
E11 - P2.2	57 - P2.2	TB1	CCI1A			57 - P2.2	E11 - P2.2
E11 - P2.2	57 - P2.2	TB1	CCI1B			ADC12 (internal)	
		DVSS	GND	CCR1	TB1		
		DVCC	VCC				
F11 - P2.3	56 - P2.3	TB2	CCI2A			56 - P2.3	F11 - P2.3
F11 - P2.3	56 - P2.3	TB2	CCI2B				
		DVSS	GND	CCR2	TB2		
		DVCC	VCC				

6.9.12 Comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

6.9.13 ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

6.9.14 DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

6.9.15 Peripheral File Map

Table 6-12 shows peripherals with word-access registers, and Table 6-13 shows peripherals with byte-access registers.

Table 6-12. Peripherals With Word Access

PERIPHERAL	REGISTER NAME	ACRONYM	OFFSET
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B3	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
Timer_A3	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DMA	DMA module control 0	DMACTL0	0122h
	DMA module control 1	DMACTL1	0124h
	DMA channel 0 control	DMA0CTL	01E0h
	DMA channel 0 source address	DMA0SA	01E2h
	DMA channel 0 destination address	DMA0DA	01E4h
	DMA channel 0 transfer size	DMA0SZ	01E6h

Table 6-12. Peripherals With Word Access (continued)

PERIPHERAL	REGISTER NAME	ACRONYM	OFFSET
ADC12 (See also Table 6-13)	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Interrupt-enable register	ADC12IE	01A6h
	Interrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h

Table 6-13. Peripherals With Byte Access

PERIPHERAL	REGISTER NAME	ACRONYM	OFFSET
OA2	Operational Amplifier 2 control register 1	OA2CTL1	0C5h
	Operational Amplifier 2 control register 0	OA2CTL0	0C4h
OA1	Operational Amplifier 1 control register 1	OA1CTL1	0C3h
	Operational Amplifier 1 control register 0	OA1CTL0	0C2h
OA0	Operational Amplifier 0 control register 1	OA0CTL1	0C1h
	Operational Amplifier 0 control register 0	OA0CTL0	0C0h
LCD	LCD memory 20	LCDM20	0A4h
	⋮	⋮	⋮
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	⋮	⋮	⋮
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h

Table 6-13. Peripherals With Byte Access (continued)

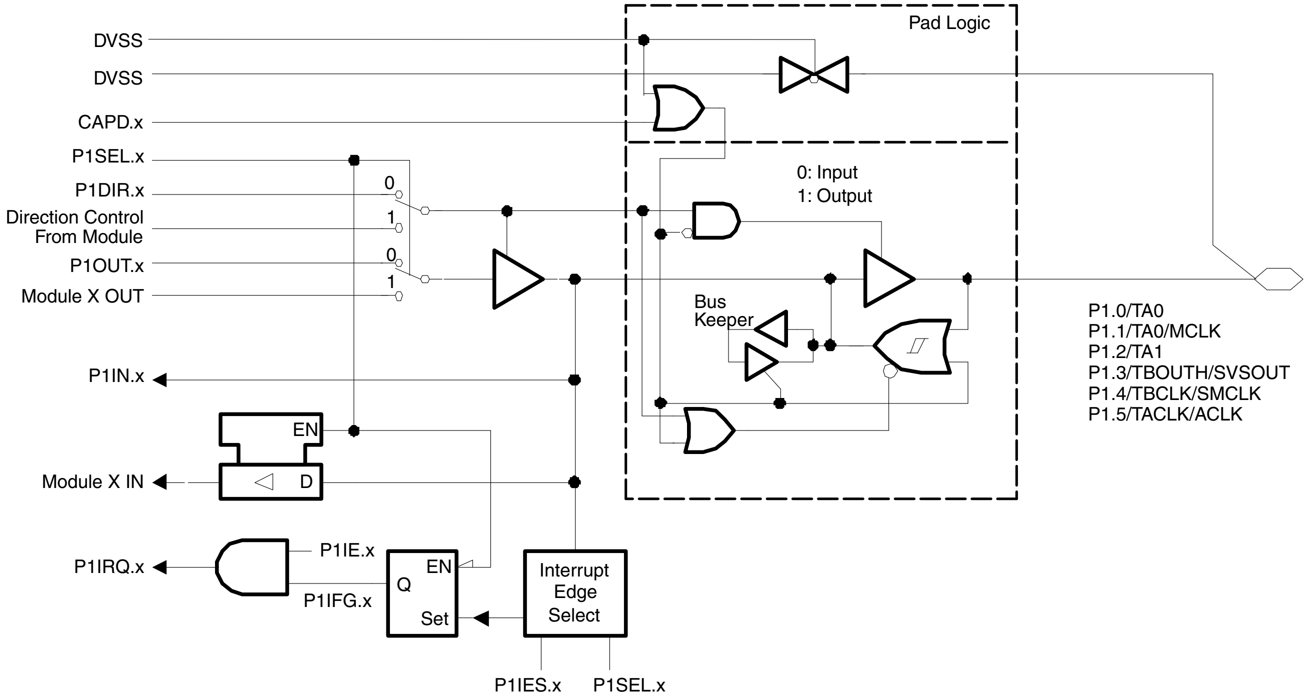
PERIPHERAL	REGISTER NAME	ACRONYM	OFFSET
ADC12 (Memory control registers require byte access)	ADC memory-control register 15	ADC12MCTL15	08Fh
	ADC memory-control register 14	ADC12MCTL14	08Eh
	ADC memory-control register 13	ADC12MCTL13	08Dh
	ADC memory-control register 12	ADC12MCTL12	08Ch
	ADC memory-control register 11	ADC12MCTL11	08Bh
	ADC memory-control register 10	ADC12MCTL10	08Ah
	ADC memory-control register 9	ADC12MCTL9	089h
	ADC memory-control register 8	ADC12MCTL8	088h
	ADC memory-control register 7	ADC12MCTL7	087h
	ADC memory-control register 6	ADC12MCTL6	086h
	ADC memory-control register 5	ADC12MCTL5	085h
	ADC memory-control register 4	ADC12MCTL4	084h
	ADC memory-control register 3	ADC12MCTL3	083h
	ADC memory-control register 2	ADC12MCTL2	082h
	ADC memory-control register 1	ADC12MCTL1	081h
	ADC memory-control register 0	ADC12MCTL0	080h
USART0 (UART or SPI mode)	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
BrownOUT, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h

Table 6-13. Peripherals With Byte Access (continued)

PERIPHERAL	REGISTER NAME	ACRONYM	OFFSET
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

6.10 Input/Output Schematics

6.10.1 Port P1, P1.0 to P1.5, Input/Output With Schmitt Trigger

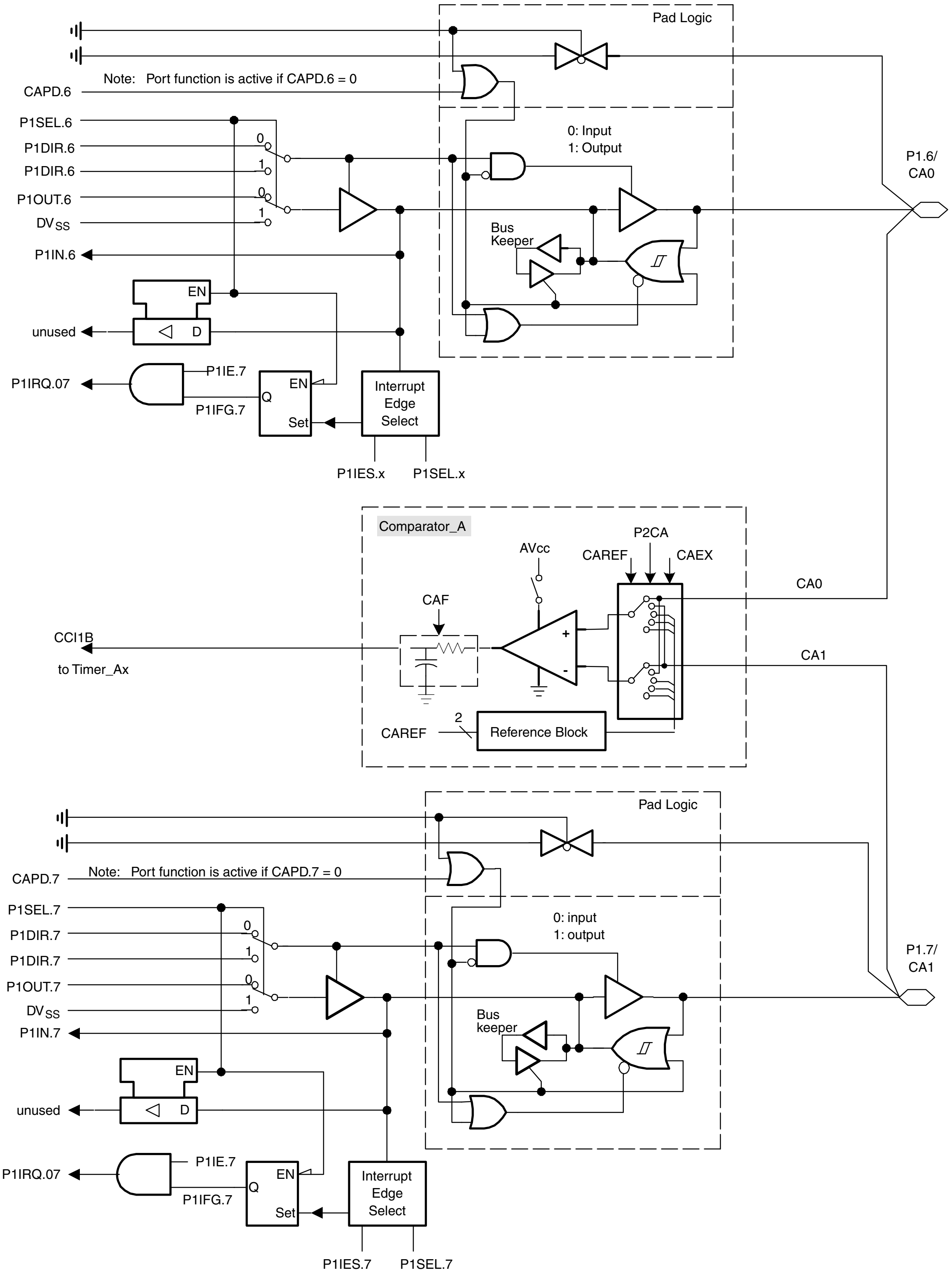


Note: 0 ≤ x ≤ 5
Note: Port function is active if CAPD.x = 0

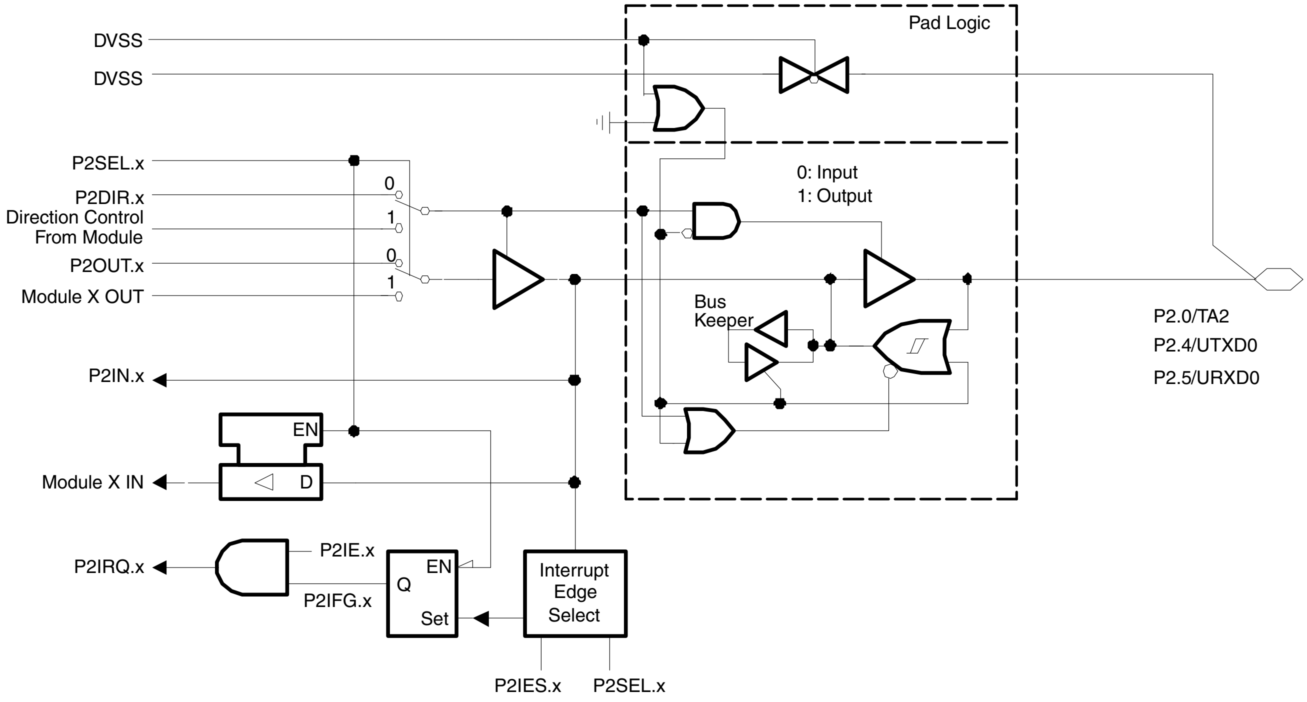
PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1SEL.0	P1DIR.0	P1DIR.0	P1OUT0	Out0 sig.(1)	P1IN.0	CCI0A(1)	P1IE.0	P1IFG.0	P1IES.0
P1SEL.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B(1)	P1IE.1	P1IFG.1	P1IES.1
P1SEL.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 sig.(1)	P1IN.2	CCI1A(1)	P1IE.2	P1IFG.2	P1IES.2
P1SEL.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOUT	P1IN.3	TBOUTH(2)	P1IE.3	P1IFG.3	P1IES.3
P1SEL.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	TBCLK(2)	P1IE.4	P1IFG.4	P1IES.4
P1SEL.5	P1DIR.5	P1DIR5	P1OUT.5	ACLK	P1IN.5	TACLK(1)	P1IE.5	P1IFG.5	P1IES.5

(1) Timer_A
(2) Timer_B

6.10.2 Port P1, P1.6 and P1.7, Input/Output With Schmitt Trigger



6.10.3 Port P2, P2.0 and P2.4 to P2.5, Input/Output With Schmitt Trigger

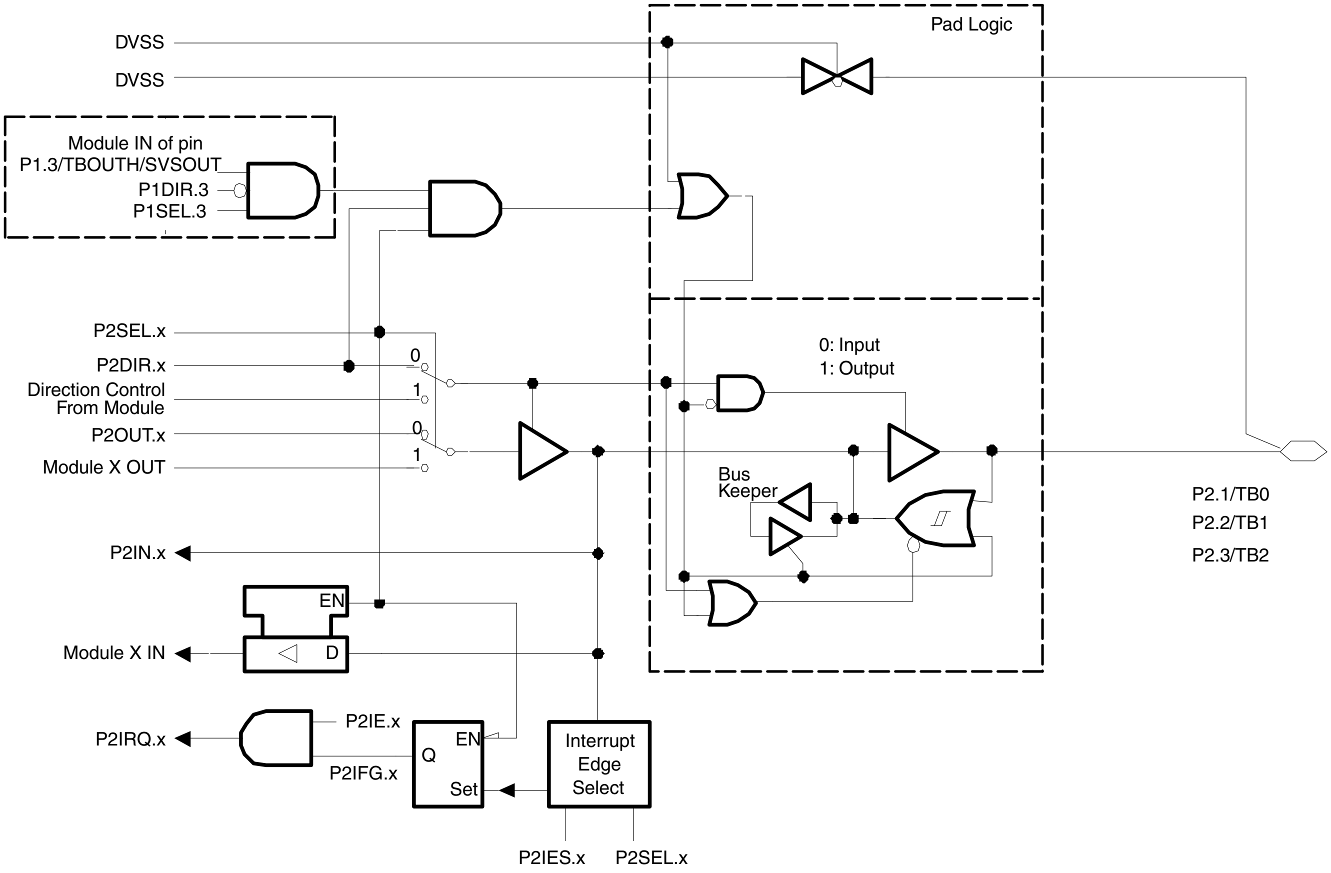


Note: x {0,4,5}

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 sig.(1)	P2IN.0	CCI2A(1)	P2IE.0	P2IFG.0	P2IES.0
P2Sel.4	P2DIR.4	DVCC	P2OUT.4	UTXD0(2)	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4
P2Sel.5	P2DIR.5	DVSS	P2OUT.5	DVSS	P2IN.5	URXD0(2)	P2IE.5	P2IFG.5	P2IES.5

(1) Timer_A
(2) USART0

6.10.4 Port P2, P2.1 to P2.3, Input/Output With Schmitt Trigger

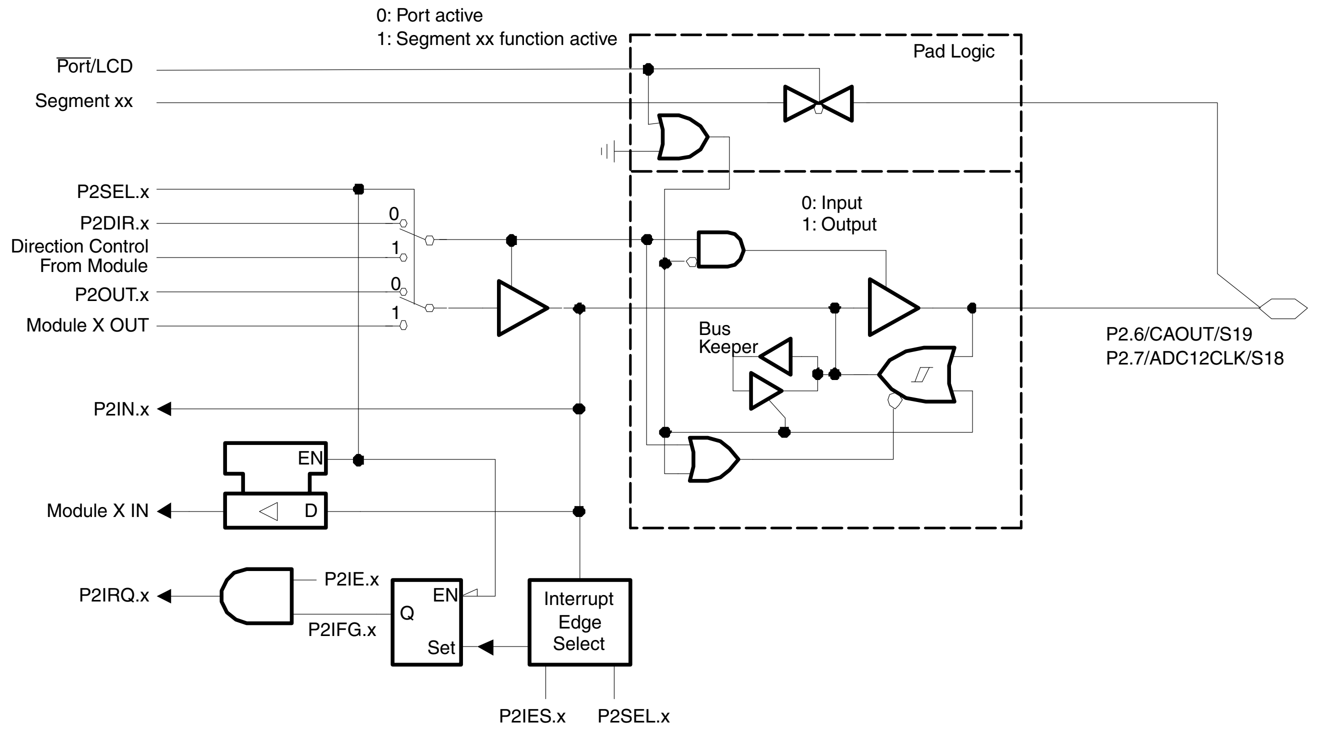


Note: 1 ≤ x ≤ 3

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	Out0 sig. (1)	P2IN.1	CCI0A (1) CCI0B	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out1 sig. (1)	P2IN.2	CCI1A (1) CCI1B	P2IE.2	P2IFG.2	P2IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out2 sig. (1)	P2IN.3	CCI2A (1) CCI2B	P2IE.3	P2IFG.3	P2IES.3

(1) Timer_B

6.10.5 Port P2, P2.6 and P2.7, Input/Output With Schmitt Trigger

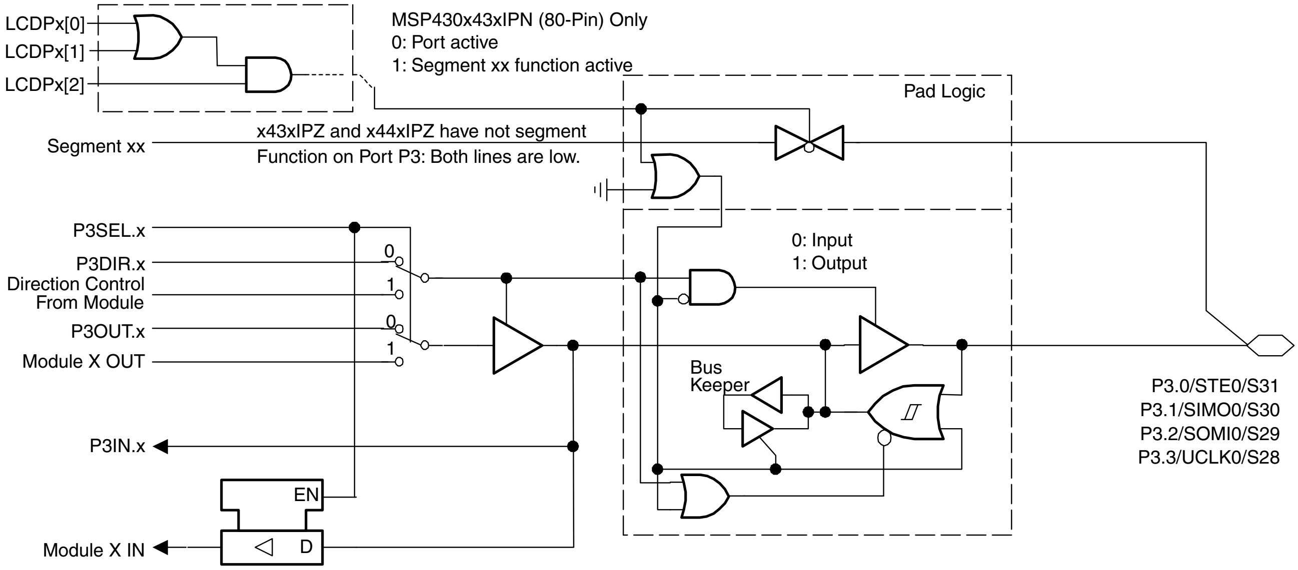


Note: 6 ≤ x ≤ 7

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x	Port/LCD
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	CAOUT (1)	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6	0: LCDPx < 02h
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	ADC12CLK (2)	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7	0: LCDPx < 02h

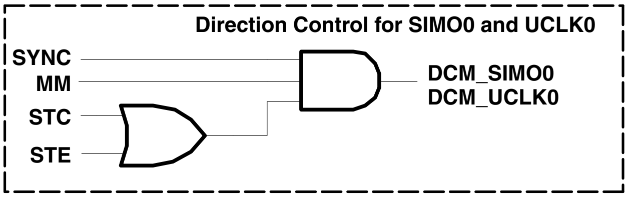
(1) Comparator_A
(2) ADC12

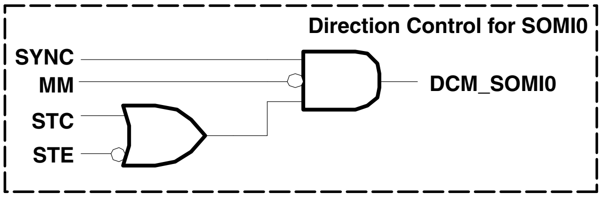
6.10.6 Port P3, P3.0 to P3.3, Input/Output With Schmitt Trigger



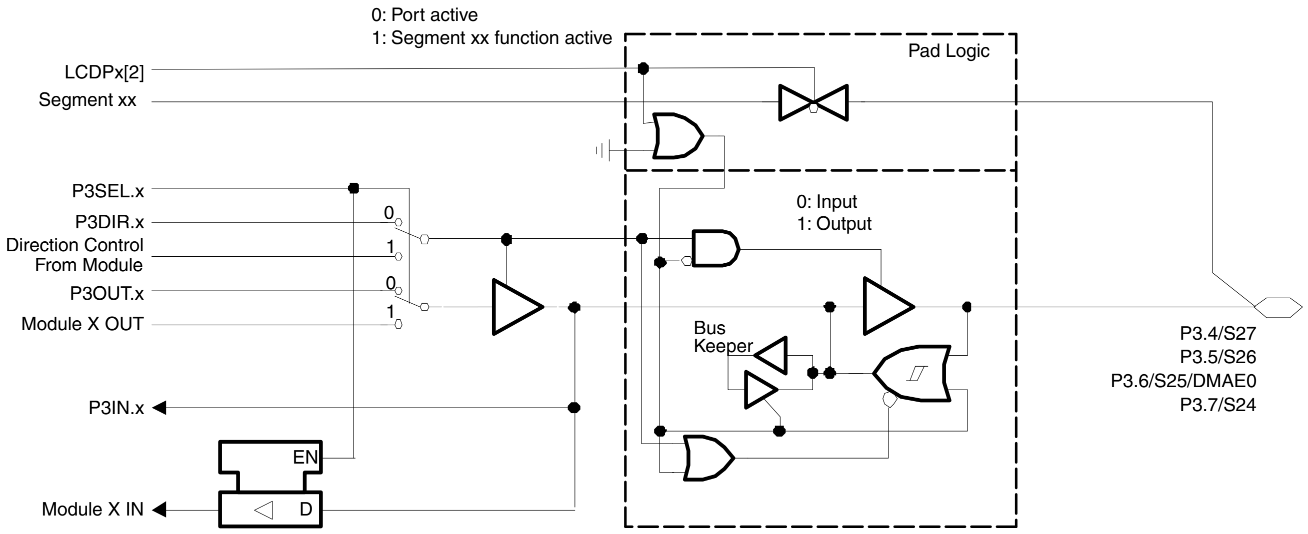
Note: 0 ≤ x ≤ 3

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.0	P3DIR.0	DVSS	P3OUT.0	DVSS	P3IN.0	STE0(in)
P3Sel.1	P3DIR.1	DCM_SIMO0	P3OUT.1	SIMO0(out)	P3IN.1	SIMO0(in)
P3Sel.2	P3DIR.2	DCM_SOMI0	P3OUT.2	SOMIO(out)	P3IN.2	SOMI0(in)
P3Sel.3	P3DIR.3	DCM_UCLK0	P3OUT.3	UCLK0(out)	P3IN.3	UCLK0(in)





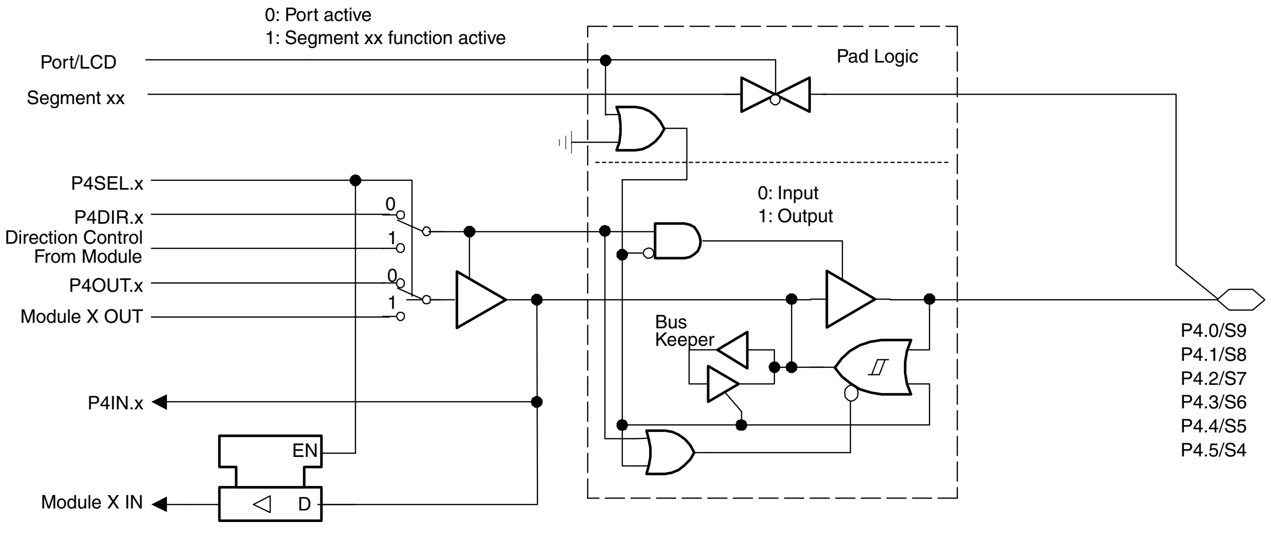
6.10.7 Port P3, P3.4 to P3.7, Input/Output With Schmitt Trigger



Note: 4 ≤ x ≤ 7

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3SEL.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS	P3IN.4	unused
P3SEL.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS	P3IN.5	unused
P3SEL.6	P3DIR.6	P3DIR.6	P3OUT.6	DVSS	P3IN.6	DMAE0
P3SEL.7	P3DIR.7	P3DIR.7	P3OUT.7	DVSS	P3IN.7	unused

6.10.8 Port P4, P4.0 to P4.5, Input/Output With Schmitt Trigger

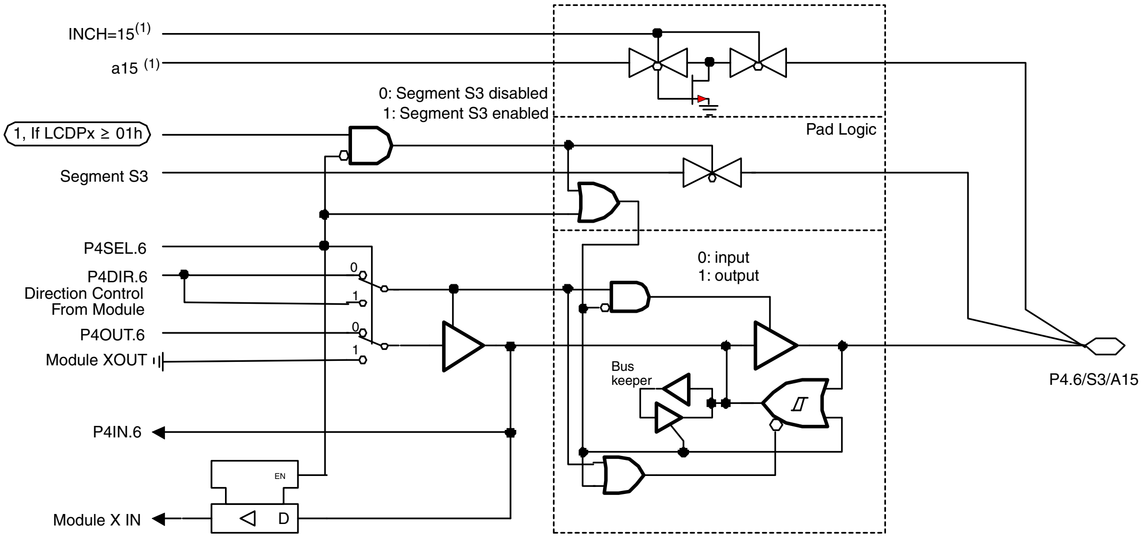


Note: 0 ≤ x ≤ 5

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4SEL.0	P4DIR.0	P4DIR.0	P4OUT.0	DVSS	P4IN.0	unused
P4SEL.1	P4DIR.1	P4DIR.1	P4OUT.1	DVSS	P4IN.1	unused
P4SEL.2	P4DIR.2	P4DIR.2	P4OUT.2	DVSS	P4IN.2	unused
P4SEL.3	P4DIR.3	P4DIR.3	P4OUT.3	DVSS	P4IN.3	unused
P4SEL.4	P4DIR.4	P4DIR.4	P4OUT.4	DVSS	P4IN.4	unused
P4SEL.5	P4DIR.5	P4DIR.5	P4OUT.5	DVSS	P4IN.5	unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEGMENT FUNCTION
MSP430FG43x	P4.0 to P4.5	LCDPx < 01h	LCDPx ≥ 01h

6.10.9 Port P4, P4.6, Input/Output With Schmitt Trigger

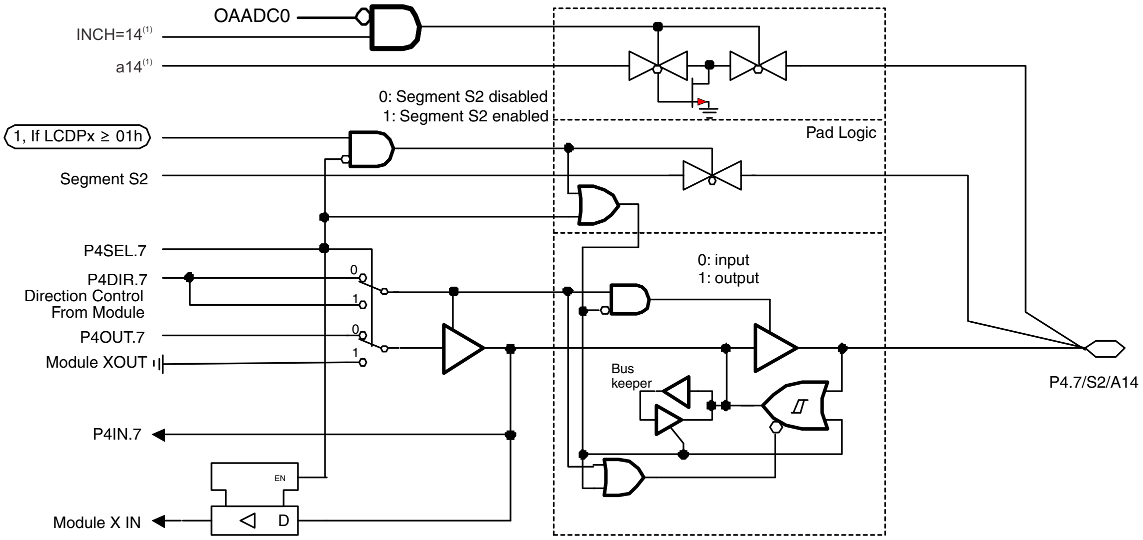


(1) Signal from or to ADC12

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4SEL.6	P4DIR.6	P4DIR.6	P4OUT.6	DVSS	P4IN.6	unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEGMENT FUNCTION
MSP430FG43x	P4.6	LCDPx < 01h	LCDPx ≥ 01h

6.10.10 Port P4, P4.7, Input/Output With Schmitt Trigger

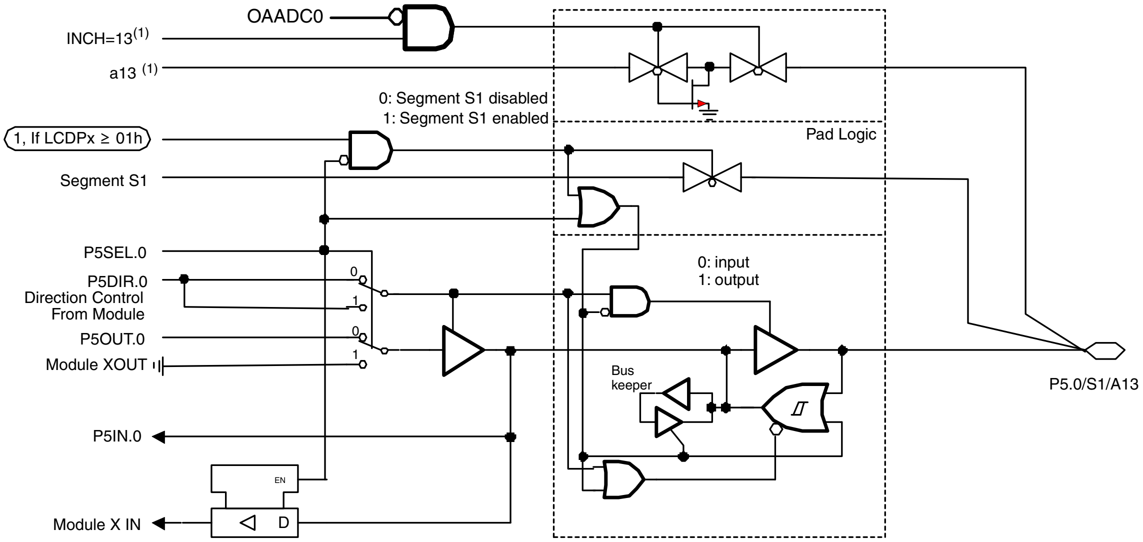


(1) Signal from or to ADC12

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4Sel.7	P4DIR.7	P4DIR.7	P4OUT.7	DVSS	P4IN.7	Unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEGMENT FUNCTION
MSP430FG43x	P4.7	LCDPx < 01h	LCDPx ≥ 01h

6.10.11 Port P5, P5.0, Input/Output With Schmitt Trigger

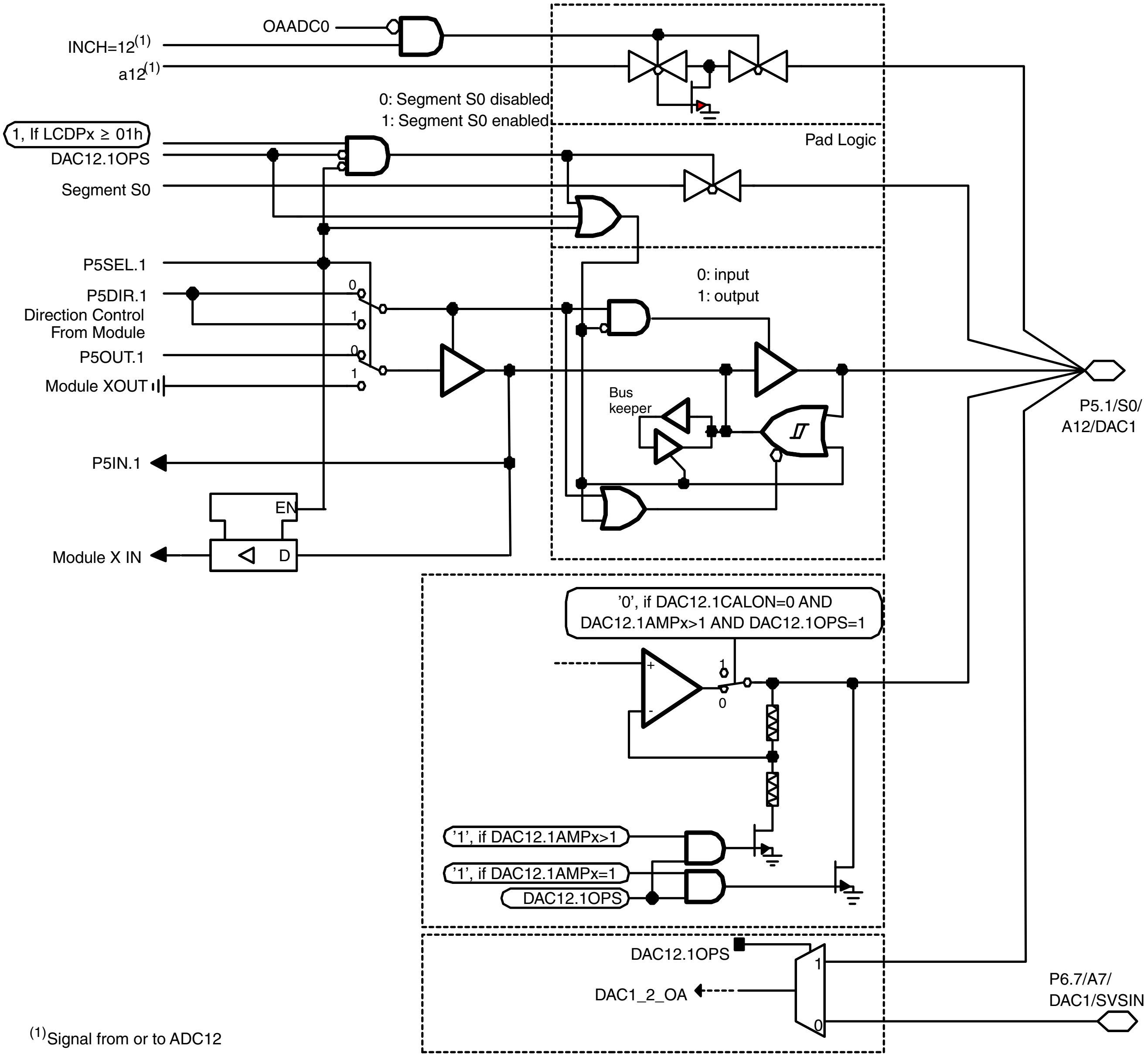


(1) Signal from or to ADC12

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P5SEL.0	P5DIR.0	P5DIR.0	P5OUT.0	DVSS	P5IN.0	unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEGMENT FUNCTION
MSP430FG43x	P5.0	LCDPx < 01h	LCDPx ≥ 01h

6.10.12 Port P5, P5.1, Input/Output With Schmitt Trigger

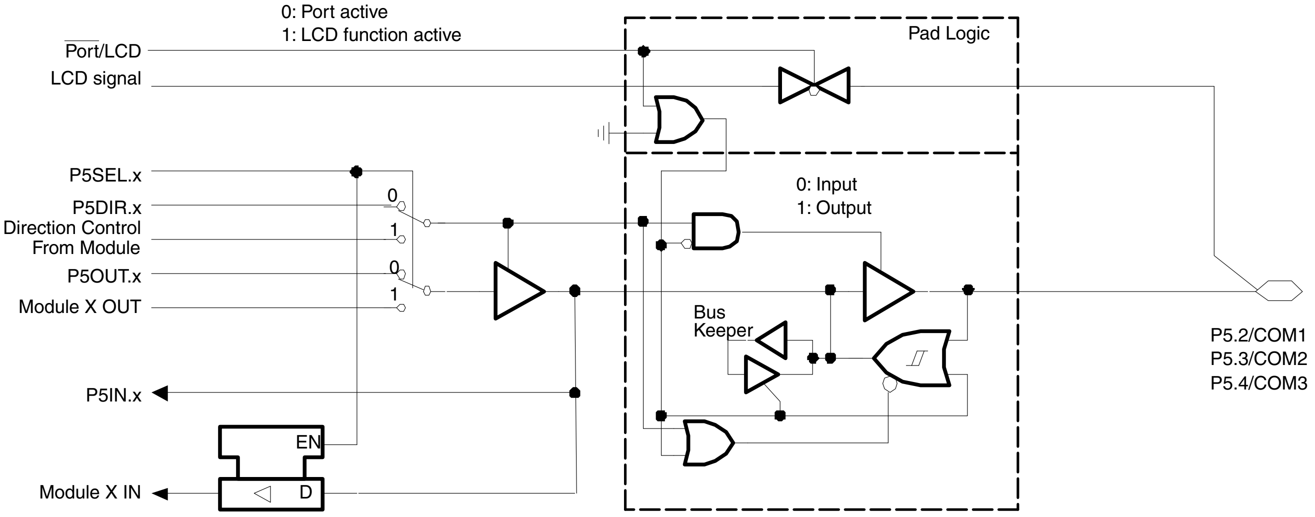


[1] Signal from or to ADC12

Function	Description	P5SEL.1	LCDPx	DAC12.1OPS	DAC12.1AMPx
DAC12	3-State	X	X	1	0
	0 V	X	X	1	1
	DAC1 output (the output voltage can be converted with ADC12, channel A12)	X	X	1	> 1
ADC12	Channel 12, A12	1	X	0	X
LCD	Segment S0, initial state	0	≥ 01h	0	X
Port	P5.1	0	< 01h	0	X

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment	$\overline{\text{Port}}$/LCD
P5SEL.1	P5DIR.1	P5DIR.1	P5OUT.1	DVSS	P5IN.1	Unused	S0	0: LCDPx < 01h

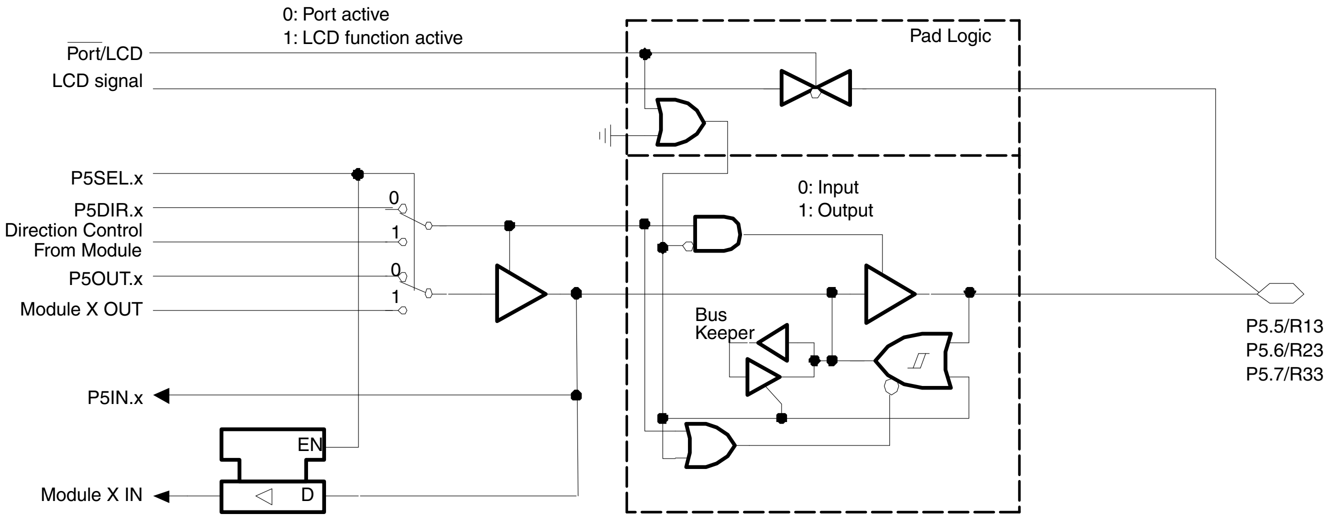
6.10.13 Port P5, P5.2 to P5.4, Input/Output With Schmitt Trigger



Note: 2 ≤ x ≤ 4

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	Port/LCD
P5Sel.2	P5DIR.2	P5DIR.2	P5OUT.2	DVSS	P5IN.2	Unused	COM1	P5SEL.2
P5Sel.3	P5DIR.3	P5DIR.3	P5OUT.3	DVSS	P5IN.3	Unused	COM2	P5SEL.3
P5Sel.4	P5DIR.4	P5DIR.4	P5OUT.4	DVSS	P5IN.4	Unused	COM3	P5SEL.4

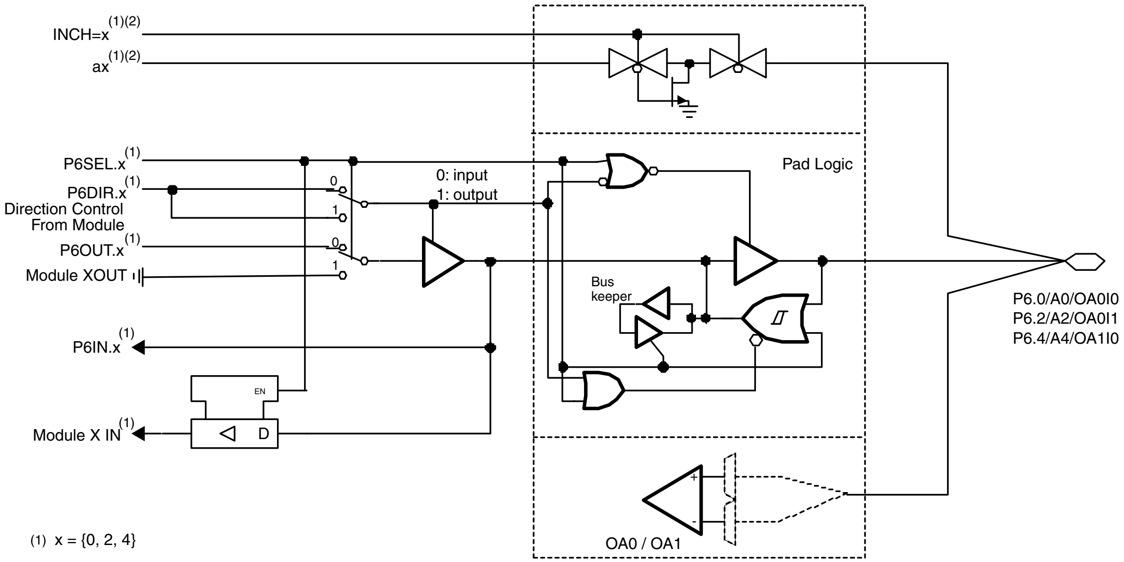
6.10.14 Port P5, P5.5 to P5.7, Input/Output With Schmitt Trigger



Note: 5 ≤ x ≤ 7

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	$\overline{\text{Port}}$/LCD
P5Sel.5	P5DIR.5	P5DIR.5	P5OUT.5	DVSS	P5IN.5	Unused	R13	P5SEL.5
P5Sel.6	P5DIR.6	P5DIR.6	P5OUT.6	DVSS	P5IN.6	Unused	R23	P5SEL.6
P5Sel.7	P5DIR.7	P5DIR.7	P5OUT.7	DVSS	P5IN.7	Unused	R33	P5SEL.7

6.10.15 Port P6, P6.0, P6.2, and P6.4, Input/Output With Schmitt Trigger



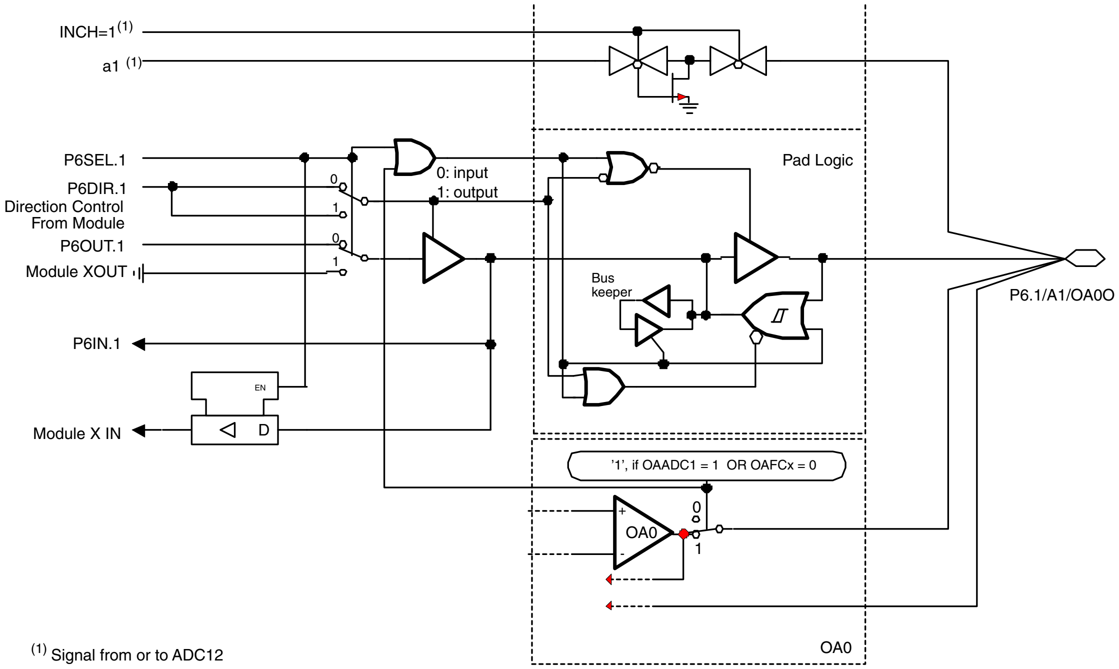
(1) x = {0, 2, 4}

(2) Signal from or to ADC12

PnSel.x[1]	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DVSS	P6IN.0	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DVSS	P6IN.2	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DVSS	P6IN.4	unused

(1) The signal at pin P6.x/Ax is used by the 12-bit ADC module.

6.10.16 Port P6, P6.1, Input/Output With Schmitt Trigger

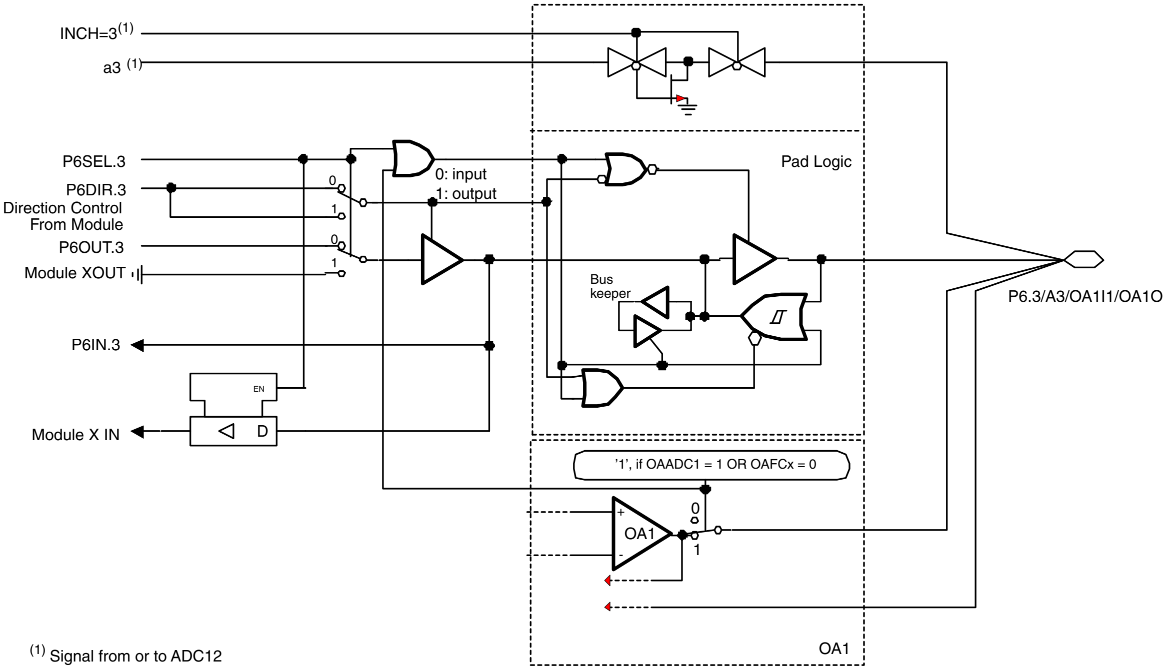


(1) Signal from or to ADC12

PnSel.x(1)	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DVSS	P6IN.1	unused

(1) The signal at pin P6.x/Ax is used by the 12-bit ADC module.

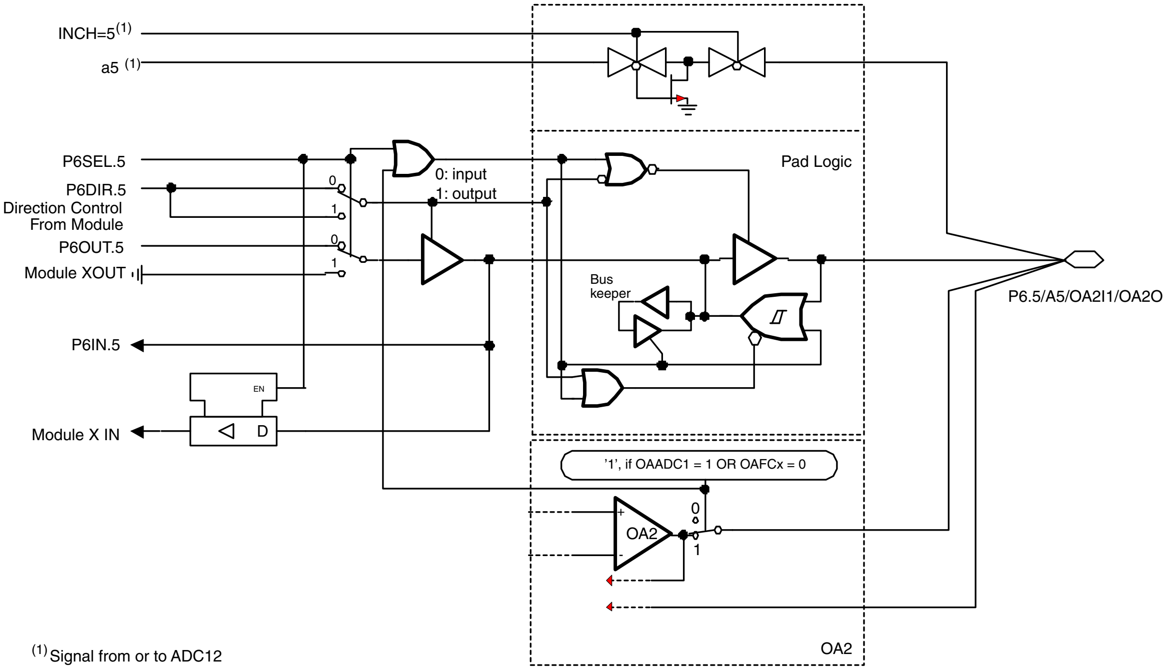
6.10.17 Port P6, P6.3, Input/Output With Schmitt Trigger



PnSel.x[1]	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DVSS	P6IN.3	unused

(1) The signal at pin P6.x/Ax is used by the 12-bit ADC module.

6.10.18 Port P6, P6.5, Input/Output With Schmitt Trigger

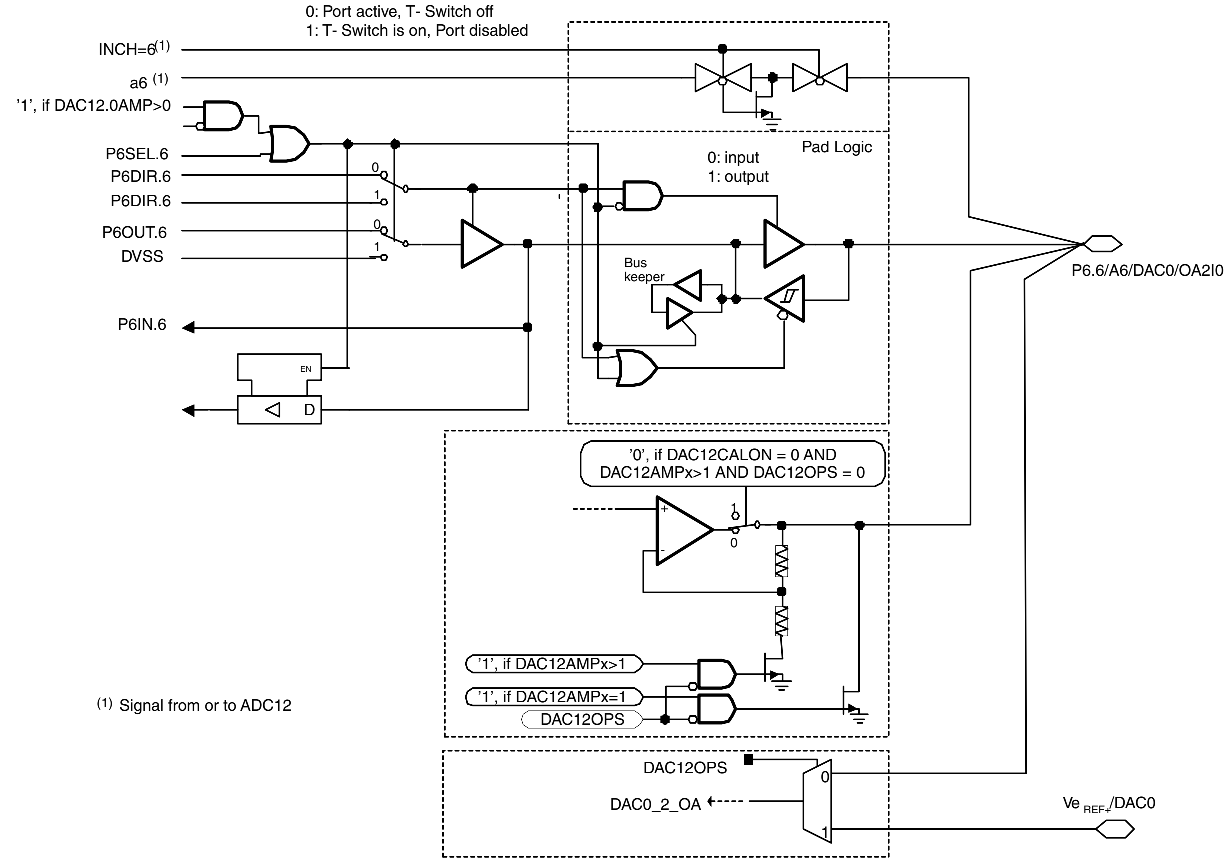


(1) Signal from or to ADC12

PnSel.x(1)	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DVSS	P6IN.5	unused

(1) The signal at pins P6.x/Ax is used by the 12-bit ADC module.

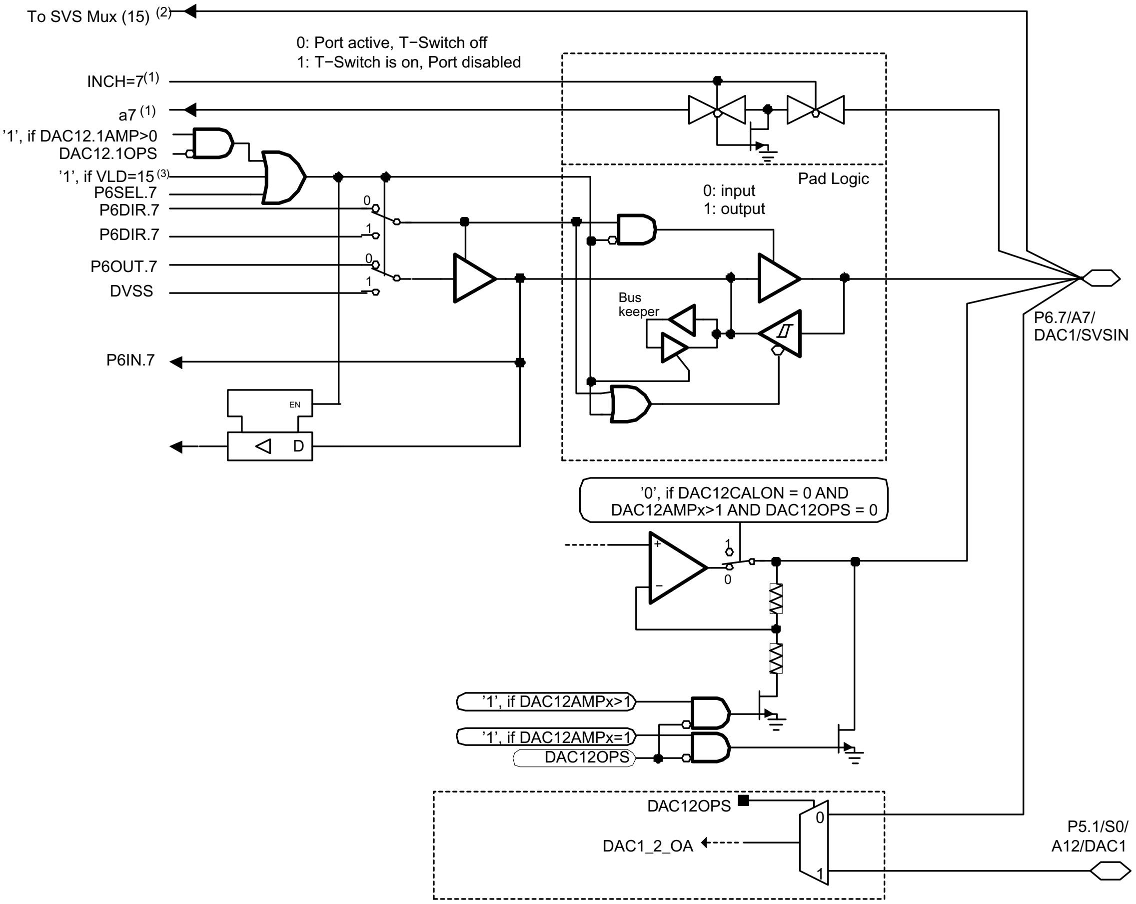
6.10.19 Port P6, P6.6, Input/Output With Schmitt Trigger



PnSel.x(1)	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DVSS	P6IN.6	unused

(1) The signal at pins P6.x/Ax is used by the 12-bit ADC module.

6.10.20 Port P6, P6.7, Input/Output With Schmitt Trigger



(1) Signal from or to ADC12

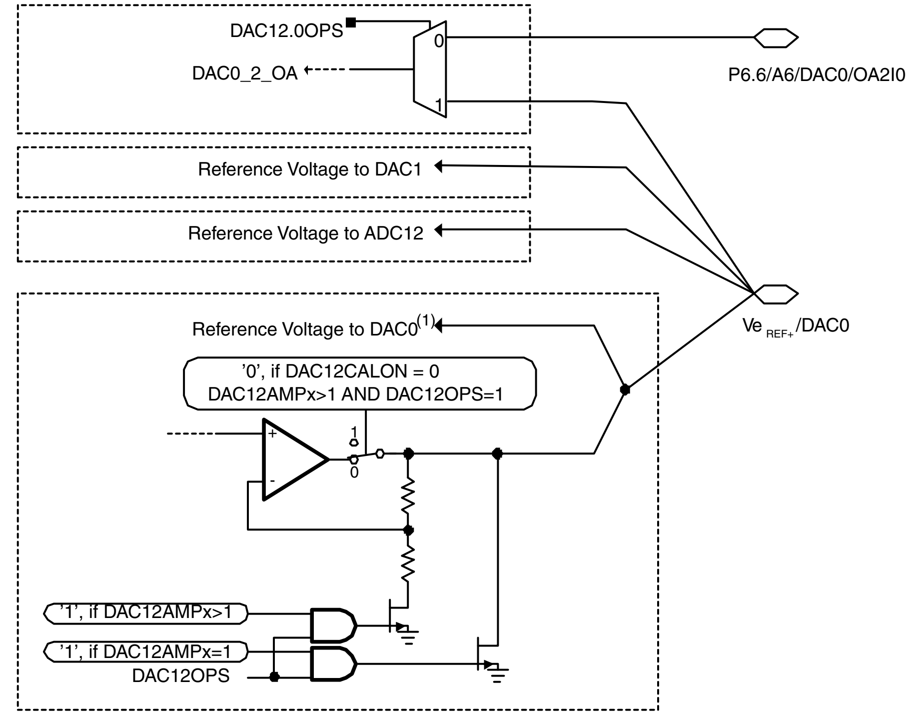
(2) Signal to SVS block, selected if VLD=15

(3) VLD control bits are located in SVS

PnSel.x[1]	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DVSS	P6IN.7	unused

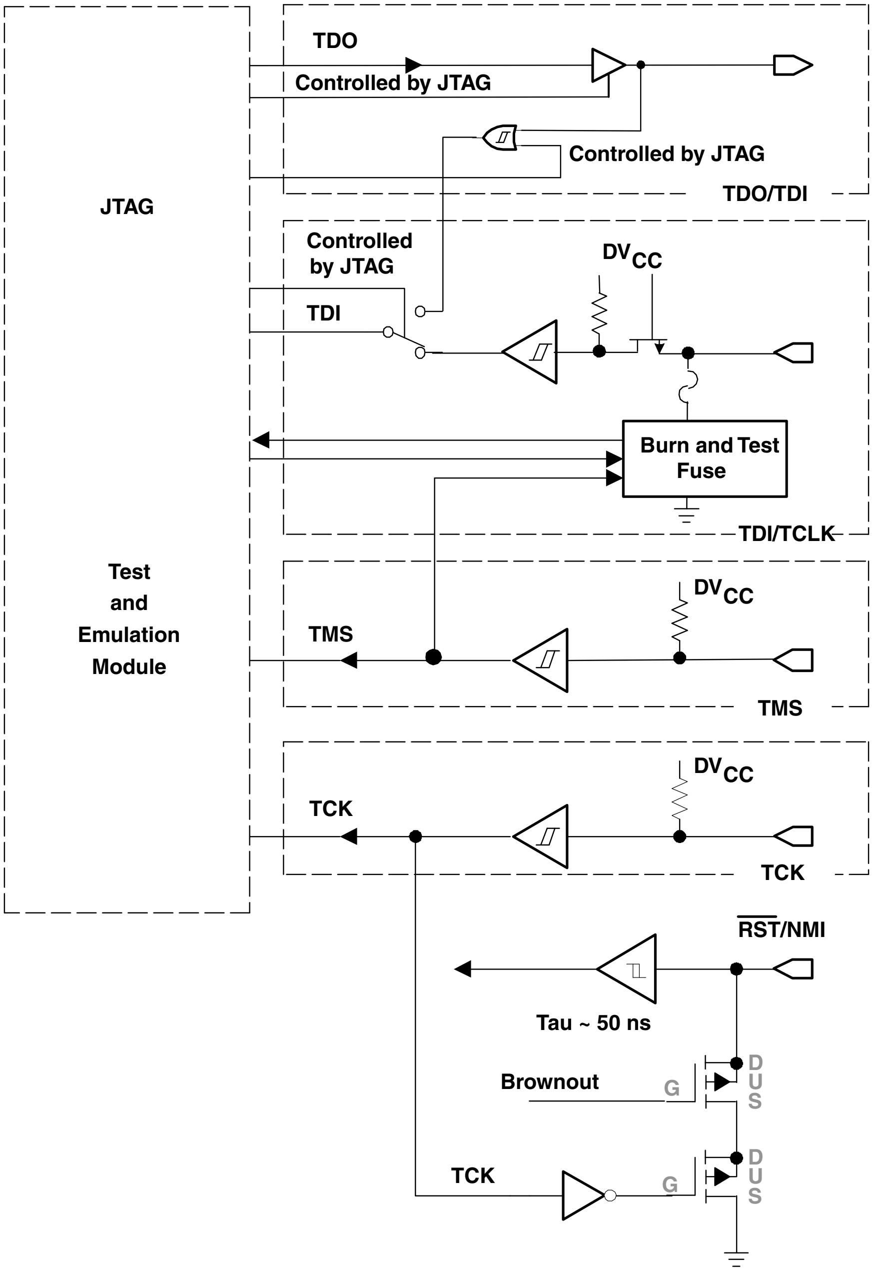
(1) The signal at pins P6.x/Ax is used by the 12-bit ADC module. The signal at pin P6.7/A7/SVSIN is also connected to the input multiplexer in the module brownout/supply voltage supervisor.

6.10.21 VeREF+/DAC0



(1) If the reference of DAC0 is taken from pin $\mathrm{Ve}_{\mathrm{REF+}}$/DAC0, unpredictable voltage levels will be on pin. In this situation, the DAC0 output is fed back to its own reference input.

6.10.22 JTAG Pins TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger or Output



6.10.23 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-8). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

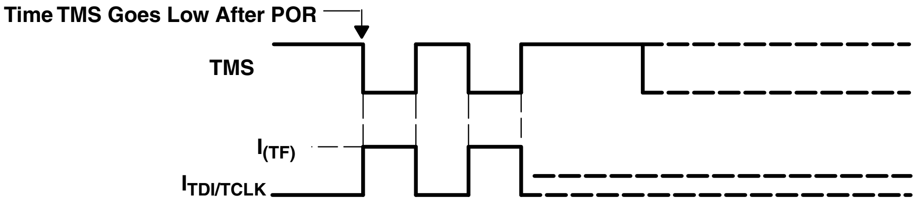


Figure 6-8. Fuse Check Mode Current

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the MSP430FG43x device applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools.

For a complete listing of development-support tools for the MSP430FG43x platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.1.1 Development Kit

The MSP-FET430U80 is a powerful flash emulation tool that includes the hardware and software required to quickly begin application development on the MSP430 MCU. It includes a ZIF socket target board and a USB debugging interface (MSP-FET) used to program and debug the MSP430 in-system through the JTAG interface or the pin saving Spy Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and because the MSP430 flash is ultra-low power, no external power supply is required.

The debugging tool interfaces the MSP430 to the included integrated software environment and includes code to start your design immediately.

7.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5259). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

PMS – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product

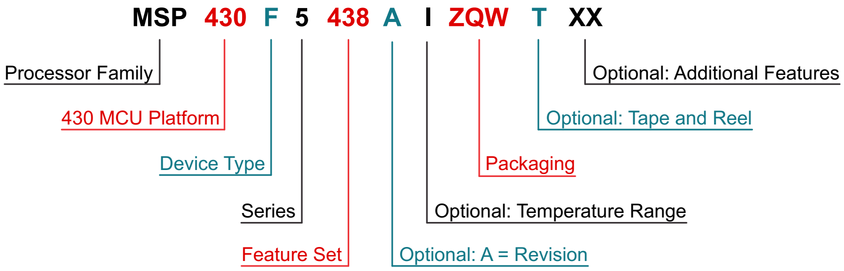
XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). Figure 7-1 provides a legend for reading the complete device name for any family member.



Processor Family	CC = Embedded RF Radio MSP = Mixed Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
430 MCU Platform	TI's Low Power Microcontroller Platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BT = Preprogrammed with *Bluetooth* BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 Series = Up to 8 MHz 2 Series = Up to 16 MHz 3 Series = Legacy 4 Series = Up to 16 MHz w/ LCD	5 Series = Up to 25 MHz 6 Series = Up to 25 MHz w/ LCD 0 = Low Voltage Series
Feature Set	Various Levels of Integration Within a Series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C	
Packaging	www.ti.com/packaging	
Optional: Tape and Reel	T = Small Reel R = Large Reel No Markings = Tube or Tray	
Optional: Additional Features	-EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C) -Q1 = Automotive Q100 Qualified	

Figure 7-1. Device Nomenclature

7.2 Documentation Support

The following documents describe the MSP430FG43x microcontrollers. Copies of these documents are available on the Internet at www.ti.com.

SLAU056	***MSP430x4xx Family User's Guide.*** Detailed description of all modules and peripherals available in this device family.
SLAZ365	***MSP430FG439 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of this device.
SLAZ364	***MSP430FG438 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of this device.
SLAZ363	***MSP430FG437 Device Erratasheet.*** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

7.2.1 Related Links

Table 7-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430FG439	Click here	Click here	Click here	Click here	Click here
MSP430FG438	Click here	Click here	Click here	Click here	Click here
MSP430FG437	Click here	Click here	Click here	Click here	Click here

7.2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.3 Trademarks

MSP430, E2E are trademarks of Texas Instruments.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430A008IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG439	Samples
MSP430A017IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG437	Samples
MSP430A018IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG439	Samples
MSP430A079IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG438	Samples
MSP430A095IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG438	Samples
MSP430FG437IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG437	Samples
MSP430FG437IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG437	Samples
MSP430FG437IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG437	Samples
MSP430FG437IZCAT	ACTIVE	NFBGA	ZCA	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG437	Samples
MSP430FG438IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG438	Samples
MSP430FG438IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG438	Samples
MSP430FG438IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG438	Samples
MSP430FG438IZCAT	ACTIVE	NFBGA	ZCA	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG438	Samples
MSP430FG439IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG439	Samples
MSP430FG439IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430FG439	Samples
MSP430FG439IZCAR	ACTIVE	NFBGA	ZCA	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG439	Samples
MSP430FG439IZCAT	ACTIVE	NFBGA	ZCA	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	FG439	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

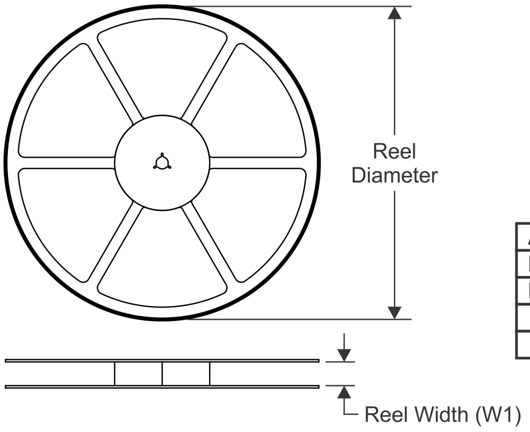
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

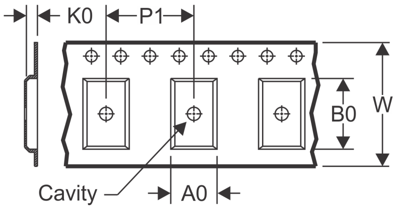
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

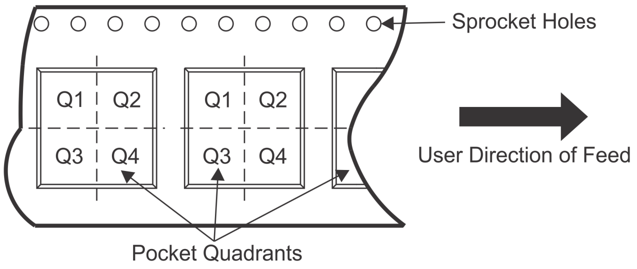


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

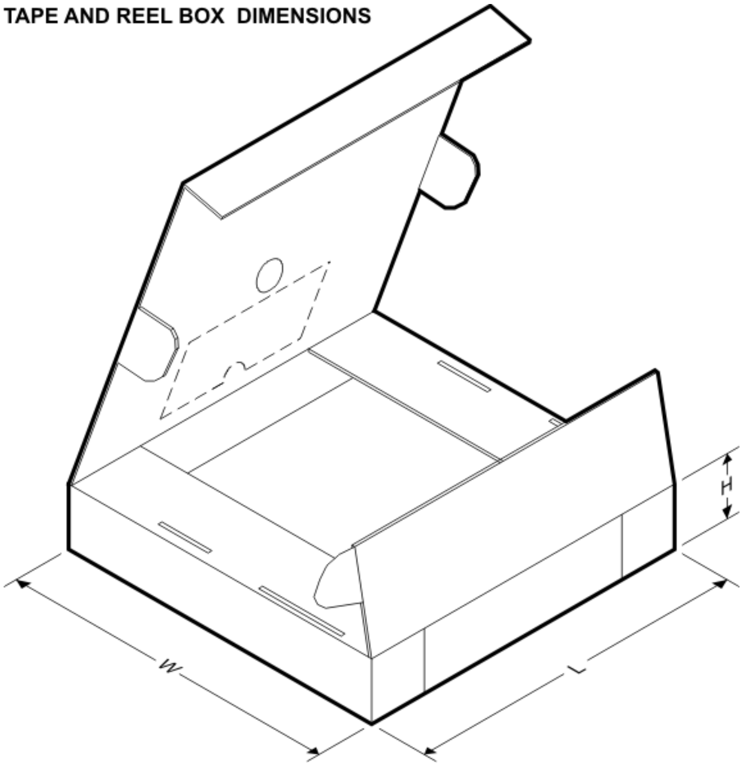
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FG437IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430FG437IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG437IZCAT	NFBGA	ZCA	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG438IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430FG438IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG438IZCAT	NFBGA	ZCA	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG439IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430FG439IZCAR	NFBGA	ZCA	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430FG439IZCAT	NFBGA	ZCA	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

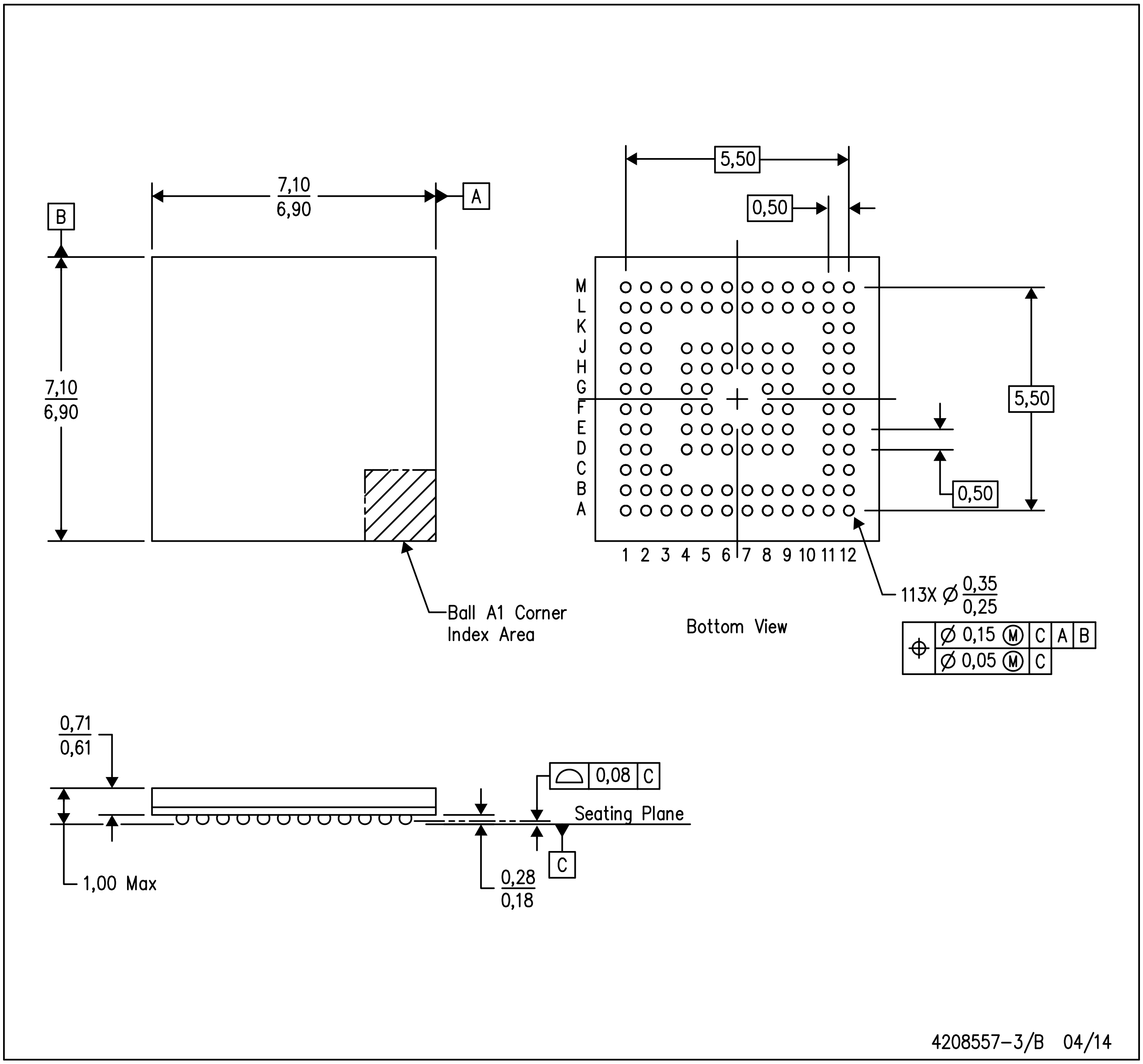
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

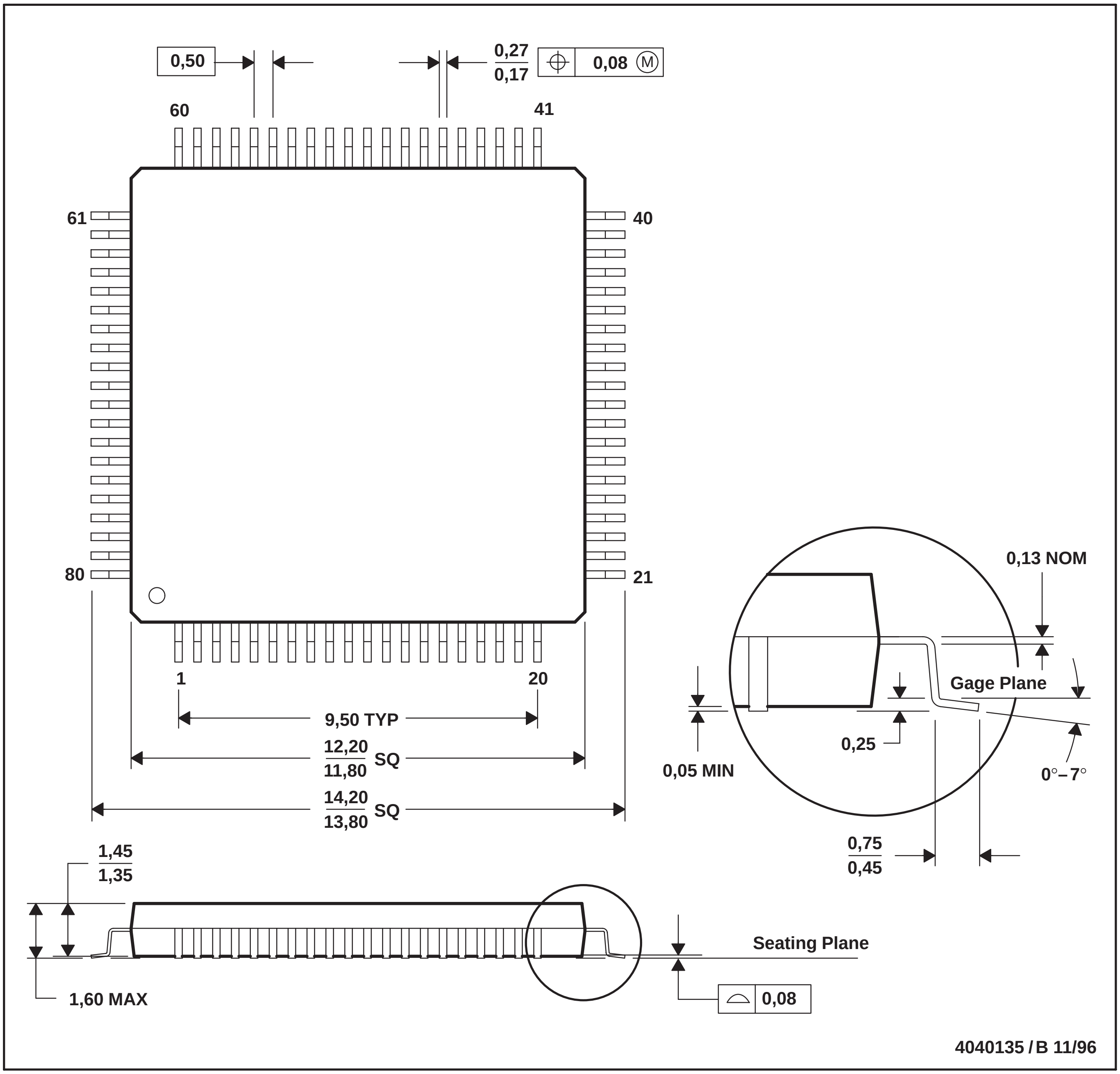
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FG437IPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430FG437IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8
MSP430FG437IZCAT	NFBGA	ZCA	113	250	341.0	336.6	31.8
MSP430FG438IPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430FG438IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8
MSP430FG438IZCAT	NFBGA	ZCA	113	250	341.0	336.6	31.8
MSP430FG439IPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430FG439IZCAR	NFBGA	ZCA	113	2500	341.0	336.6	31.8
MSP430FG439IZCAT	NFBGA	ZCA	113	250	341.0	336.6	31.8

ZCA (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. JEDEC MO–225 registration is pending.
- D. This is a Pb–free solder ball design.

PN (S-PQFP-G80) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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