Innovative Techniques for Extremely Low Power Consumption with 8-bit Microcontrollers

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Summary

With the increasing use of microcontrollers in all sorts off applications, low power has become an very important parameter when choosing microcontrollers. Today's microcontroller designs are often battery or signal wire powered applications replacing passive or mechanical components. Common for them all is the requirement of very low power consumption but with enough power to fill the specification of the product. This white paper will highlight some of the challenges of modern microcontroller design and how the new picoPower™ techniques used in the Atmel® AVR® microcontroller is addressing them.

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Introduction to Power Consumption of MCUs

Why is Low Power Important?

In the same way that fuel consumption is important in everything from scooters to oil tankers, power consumption is a key parameter in most electronics applications. The most obvious applications for which power consumption is critical are battery-powered applications, such as home thermostats and security systems, in which the battery must last for years. Low power also leads to smaller power supplies, less expensive batteries, and enables products to be powered by signal lines (such as fire alarm wires) lowering the cost of the end-product. As a result, low power consumption has become a key parameter of microcontroller designs.

Low Power Parameters

Although power consumption is the product of operating voltage (Vcc) multiplied by the current consumption (Icc), current consumption is usually the only measure considered when describing the power characteristics of a chip. This is a mistake because decreasing the operating voltage directly reduces the current consumption and the overall power drain.

Current consumption increases directly with the system clock frequency so keeping the system clock as low as possible is critical to keeping power consumption down. The clock frequency is affected by a number of factors that include the microcontroller's surroundings and peripheral set as well as the architecture and the instruction set. RISC microcontrollers typically execute in a single clock cycle but some architectures divide the clock down in the same way as CISC architectures do before feeding it to the CPU. This situation leads to confusion about what clock frequency is really required to execute the target application. Designers should pay close attention to the Instruction set architecture when reading the current consumption numbers in a microcontroller's datasheet.

Most datasheets provide power consumption numbers for the microcontroller with no peripherals running. The additional current drawn by the peripherals must be taken into account since all MCUs have peripherals and their contribution to power drain can be significant.

Temperature is another factor. Since higher temperatures lead to higher power consumption, designers should always consider the power numbers for worst-case temperatures.

Active versus Sleep

In many applications, the processor does not run continuously and peripherals may be idle much of the time. The overall power consumption can be lowered by taking advantage of various "sleep" modes available on virtually all processors. The most common sleep modes are Power Down" (PWD), Power Save (PS) and Idle.

In Power Down mode everything is shut down, including the clock source. In Power Save mode everything is turned off except a 32 kHz clock running from a crystal to keep track of

time. Idle mode is a shallow sleep mode where only parts of the device are shut down but the main parts of the microcontroller are running.

The advantage of having multiple sleep modes is the flexibility it provides to shut down any part of the microcontroller that is not absolutely necessary to the function at hand. The amount of power that can be saved depends on the mode being using. For example with a 1.8V supply voltage operating at 1 MHz and 25ºC, Atmel's ATmega165P AVR controller consumes 340 uA in Active mode, 150 uA in Idle mode, 0.65 uA in Power Save mode and a scant 0.1 uA in Power Down mode.
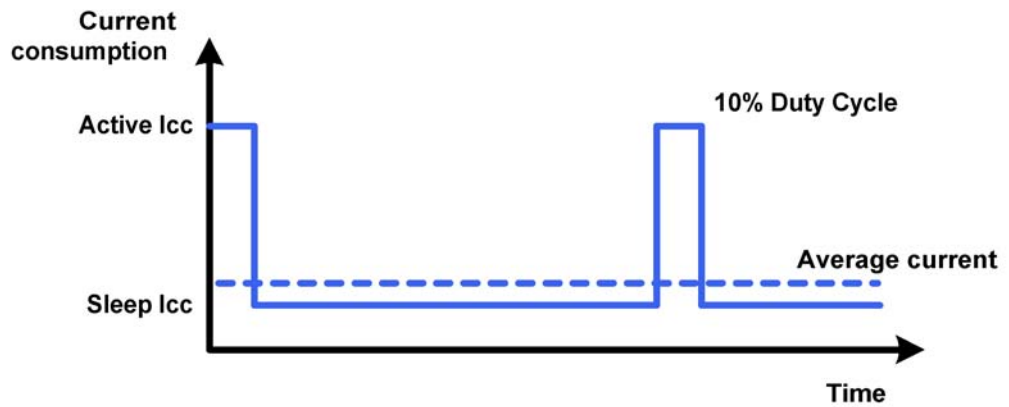

Figure 1: Power budget

Since a microcontroller can spend substantial amounts of time inactive, it is important to consider power consumption in sleep modes as well as active power consumption. Many designers use a power budget to determine the average power consumption and to calculate the battery requirements.

Although a great deal of attention is paid to active power consumption, the most important mode to consider really depends on the duty cycle between the various sleep and active modes. In applications such as thermostats, keyless entry, or security systems the processor spends most of its time idle. For these applications, sleep mode may represent the lion's share of power consumption and will be the most important parameter to consider.

How to Lower Power Consumption in Sleep Mode

Modern microcontrollers are built on digital CMOS logic that is in theory, only consuming power when the logical or clock signals are changing state. A signal is toggled when it has a transition from "0" to "1" or vice versa. Based on this theory, sleep current consumption should be equal to zero. In real life, the picture is a bit more complex. Although sleep mode power consumption approaches zero, current leakage and peripherals that remain active can consume quite a bit of power.

Leakage Current

The temperature, the supply voltage and the process technology affect the leakage current. Some microcontroller manufacturers use proprietary processes specifically developed for low power operation based on years of research and experience. These processes can provide sleep currents down to 100 nA due to the power-optimized process and the ability to operate at a true 1.8V supply voltage. Some microcontrollers that claim 1.8V operation voltage actually must use voltages as high a 2.2V for analog modules or flash writing to work properly. Atmel offers true 1.8V operation in which the memories and analog modules *all* operate at 1.8V. Caution should be used when evaluating a microcontroller's supply voltage specifications to verify that the supply voltage is a "true" 1.8V.

The trend of smaller and smaller process technologies has become very popular in recent years because they allow faster clocks and smaller die sizes. However, current leakage is one of the real disadvantages of aggressive processes with small geometries. The rule of thumb is that the leakage, and thus the sleep current, increase as the process geometries decrease.

Process is also used very loosely. All microcontrollers are not usually made using a single process but with several different processes that are specialized for different sections of the device. The processes used for 8- and 16-bit microcontrollers typically range are from 0.50 down to 0.15 micron.

Active Peripherals

The biggest contributors to sleep mode power consumption are active peripherals. Enabling internal analog or digital modules can cause a significant increase in the overall current consumption but can be difficult to evaluate. While well-documented microcontrollers describe this additional current consumption in their datasheet, others claim that this current consumption equals zero. This is very seldom a correct statement especially when it comes to analog features. When it is correct, the zero power features is likely to have poor performance. The power consumption in digital logic is mainly due to the toggling frequency, the capacitive load, and the supply voltage. The power consumption in analog modules is, on the other hand, static. There is often a trade-off between power consumption and robustness, accuracy, speed and fast start-up time in analog modules. Decreasing power consumption also often decreases the quality of the analog module.

The single-most important analog module in terms of power consumption during a sleep mode is the brown-out detector (BOD). A BOD protects the microcontroller when the supply voltage falls below its operating threshold by resetting the device. This keeps the microcontroller in a defined state when the Vcc is below its operating threshold. The BOD is not important to the microcontroller while it's in sleep mode but it is extremely important when it wakes up. Therefore, as a rule, most microcontrollers keep the BOD active during sleep mode and it contributes substantially to sleep mode power consumption.

There are two ways of getting around BOD power consumption in sleep: making a "zero-power" BOD or turning the BOD off altogether.

Since the BOD must be functional when the controller wakes up, making a zero-power BOD may seem like the most attractive option. However, lowering the power to the analog module can make it very slow and make it respond too slowly to an out-of-range voltage supply. Since the microcontroller is not running any code or writing or erasing the Flash or EEPROM in sleep mode, the BOD is not really necessary. However, it *does* need to be operational the moment the controller wakes up. The solution to this problem is to have the microcontroller shut down the BOD when it enters sleep mode and start it again just before leaving sleep mode. This approach ensures the BOD is functioning when it is needed without any current penalty while in sleep mode.

The 32 kHz Crystal Oscillator

In many applications, the time spent in active mode is insignificant compared to the time spent in power save mode with everything turned off except a real-time clock and the brown-out detector. In these applications, the power consumed in Power Save mode (sum of PWD, BOD and the 32 kHz oscillator) is the most significant contributor to overall power consumption. Therefore, lowering the current consumption of the 32 kHz oscillator can significantly reduce overall system power consumption. Designers should be very thorough in evaluating the current consumed with the crystal oscillator running.

Very Low-power Oscillators versus 32 kHz Oscillators

There are, in general, two ways of timed wake from deep sleep: either by a RTC or by very low power oscillators (VLO). The difference between them is mainly the accuracy. The RTC allows proper timing due to the very accurate 32 kHz oscillator while a VLO is very inaccurate and not suited for time-critical functions.

The AVR picoPower Technology

The increasing use of battery and signal line powered applications mandate low power solutions. Atmel has spent the last decade refining its technologies and architectures to achieve the industry's lowest power consumption. The culmination of this effort is its new picoPower technology which will be implemented in new ultra low-power 8-bit RISC AVR microcontrollers to be introduced during 2006.

Sleep Power Consumption Techniques Incorporated by picoPower Technology

Sleep is often considered the most important low power mode, particularly in applications that spend the majority of their time active. Atmel's picoPower technology employs a number of techniques that result in the lowest sleep mode power consumption of any microcontroller on the market today.

True 1.8V Supply Voltage

The processes used in AVR MCUs support a power supply voltage range from 1.8V to 5.5V. The 1.8V operation is a true 1.8V operation. Which means that all the analog modules, Flash, EEPROM and RAM run at 1.8V. True 1.8V operation ensures less power consumption as the consumption is the sum of current and voltage as well as allowing the battery supply to drop to 1.8V before being out of range.

Minimized Leakage Current

The temperature, the supply voltage and the process affect the leakage current. Atmel has used proprietary processes that have been specifically developed for low power operation based on years of research and experience. The leakage current of picoPower AVRs is less than 100 nA.

Taking the BOD to the Sleeping BOD

Although zero-power brown-out detectors (BOD), such as that used in TI®'s MSP430, can save a lot of power, they are notoriously slow and can require a millisecond to detect a below-threshold voltage. The slow response time could put the controller at risk. Atmel's AVR BOD detects brown-out conditions in 2 microseconds but draws about 20 uA, adding substantially to the Power Down current of 100 nA.

As part of the picoPower technology, Atmel has maintained the high performance and relatively high current of the BOD and saved power by simply turning it off when it is not needed. This approach results in the lowest overall power consumption and the highest possible performance with accurate detection at 1.8V, 2.7V and 4.5V. In addition to the slow response time on the MSP430, there is some concern that its detection level is only 1.4V, substantially lower than the 2.2V required to have all the controller's features available.

Since there is no need for the BOD while the MCU is in the deep sleep mode, the picoPower BOD can be turned off in Extended Standby, Standby, Power Save and Power Down modes.

The picoPower BOD-disable feature is enabled by the application using a two-step secure operation and is fully automatic. When entering sleep, the BOD is disabled *after* the MCU has entered the sleep mode, and enabled to verify that the power supply is sufficient *before* the MCU is allowed to wake from sleep. If the power supply is not sufficient, the MCU will enter a reset mode before any code execution takes place.

While in sleep mode, the only critical parameters to handle are the RAM and register contents. On AVR microcontrollers these contents are valid until ~0.3V Vcc, while the

AVR's Power-on Reset (POR) triggers at ~1.0V. If a power supply voltage drop should occur while in sleep mode with the BOD disabled, the SRAM and register contents will be valid until a POR occurs. A POR will enable the BOD again and set the POR flag to be read by the application firmware.

The BOD disable feature completely eliminates any power consumption penalty for the BOD during sleep mode *and* the MCU has full protection in active mode*.*

Ultra Low Power 32 kHz Crystal Oscillator

Since the time spent in active mode can be insignificant compared to the time spent in Power Save mode, Power Save mode is often the most important power consumption characteristic of a microcontroller. The latest 32 kHz crystal oscillator design utilized in the AVR MCUs reduces the current consumption in Power Save mode to a level comparable to Power Down mode.

Competing microcontrollers offer Power Save current consumption as low as 700 nA, including the oscillator and BOD. With a supply voltage of 1.8 volts, the AVR picoPower technology achieves the industry's lowest Power Save current consumption of 650 nA with the 32 kHz oscillator running and a sleeping BOD.

Active Mode Power Consumption Techniques Incorporated by picoPower Technology

In theory, digital CMOS logic consumes power only when the logical signals or the clock signals are toggling. A signal is toggled when it has a transition from "0" to "1" or a transition from "1" to "0". When all the digital signals are static, like in Power Down mode, only leakage current and current used to enabled analog modules is consumed.

The power consumption in an MCU can be calculated with the following equation:

$$P = \tfrac{1}{2} * F_{Toggle} * C_{Load} * V_{DD}^{2}$$

Where F_{Toggle} is the toggling frequency, C_{Load} is the capacitive load and V_{DD} is the supply voltage. In addition a small adder is made by the digital logic's leakage current and the current consumed by analog modules in idle mode but this minor components in active current consumption.

Toggling Frequency

The toggling frequency for a given device can be seen as the number of gates toggling to achieve a certain task. This can be reduced by minimizing both the number of gates and the number of times each gate needs to toggle.

Clock Gating

Clock gating is used to reduce the toggling frequency. A clock signal can be stopped using a gating element. Any clock distribution or clock domain that is gated is frozen and won't consume any power. A gating element must handle any spike issue on the clock signal. The principle of clock gating is depicted in Figure 2.
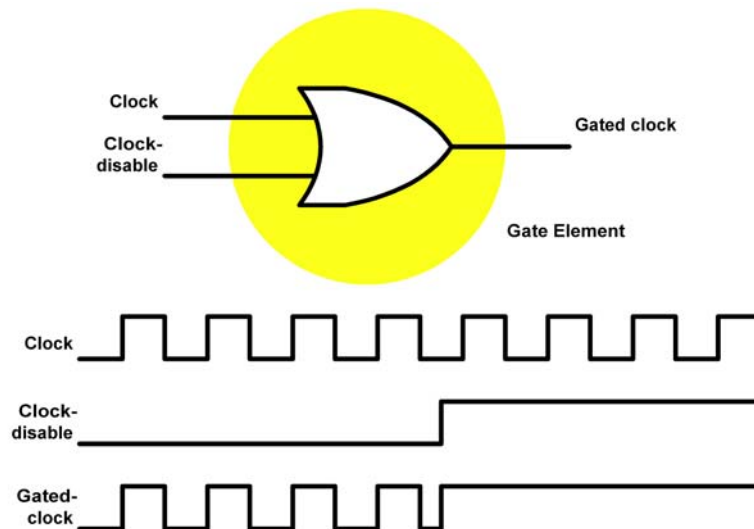

Figure 2: Clock gating principle
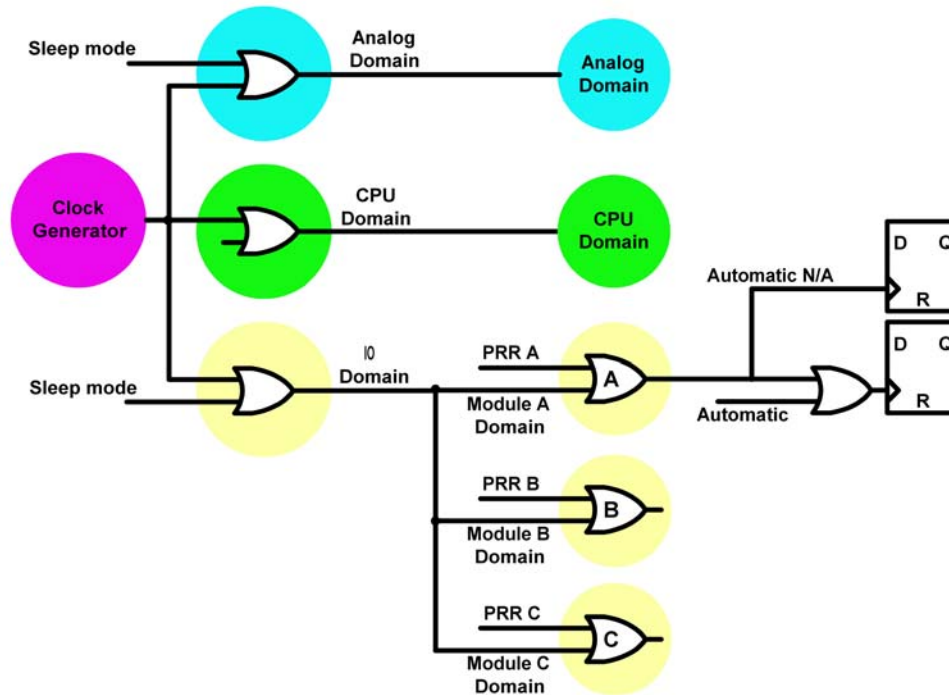
The AVR features three main levels of clock gating.

Figure 3: Three main levels of clock gating

Clock Gating Level One: Sleep Functionality

The first level of clock gating are the sleep modes that have always existed on the AVR. The sleep modes gate the clock distribution to a group of functionality thereby enabling different levels of sleep and functionality.

• Idle mode gates the CPU clock domain and the Flash clock domain while the peripherals and interrupt system continue to operate.

• The ADC noise reduction mode allows the ADC to operate while most of the peripheral clock domains, in addition to the CPU clock domain, and the Flash clock domain are gated.

• The Power Down mode gates all clock domains on the AVR and only enabled asynchronous operation is allowed. The external oscillator is also stopped in Power Down mode.

• The Power Save mode is the same as Power Down mode except that the asynchronous timer can operate when it is enabled.

• The Standby mode is the same as Power Down mode except that the main oscillator is kept running.

- The Extended Standby mode is the same as Power Save mode except that the main oscillator is kept running.

The response time for wake-up from sleep mode is only six clock cycles when the internal RC oscillator or an external clock is selected as the clock source. Power consumption during the wake-up session is less than in Idle mode. This means that the AVR can wake-up from sleep mode and re-enter the sleep mode again with extremely-low energy consumption and spend a very short time during wakeup and active mode.

Clock Gating Level Two: Power Reduction Registers

The second level of clock gating is the Power Reduction Register (PRR). Many peripheral modules are only used for a short period of time or not at all. The Power Reduction Register contains control bits for disabling unused peripheral modules. The entire clock distribution to disabled peripheral modules is gated. This is more powerful than just disabling the module by its enable bit since the modules IO registers are disabled by the PRR.

The Power Reduction Register is controlled by software that allows the user to turn on and off peripheral modules at any time. The current state is frozen and all I/O registers are inaccessible when the peripheral module is disabled by the Power Reduction Register. When re-enabled, the peripheral module continues in the same state as before it was disabled. Disabling one peripheral module results in a reduction of 5 to 10% of the total power consumption in active mode and 10 to 20% of the total power consumption in Idle mode.

Clock Gating Level Three: Automatic Clock Gating

Designs without clock gating update all registers every clock cycle. If no change has taken place, the register is updated with its previous state, unnecessarily consuming power.

Automatic clock gating (or multi-level clock gating) only allows the clock through when an update is required (i.e. when a value has changed). Rather than updating the register with the previous state, the clock to the register is gated.
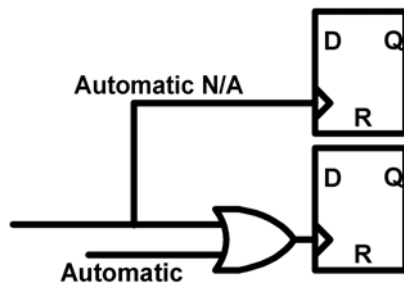

Figure 4: Design with and without automatic clock gating

One-phase Clock System

In many controllers, a significant amount of the overall power consumption is due to power consumption used in the clock distribution. AVR microcontrollers feature a one-phase clock system that reduces power consumption below that of a two-phase clock system.

Capacitive Load and Low Power IC Design Techniques

The AVR design flow is an optimized and power-driven design flow. State-of-the-art CAD tools are used for synthesis, layout and validation.

Hold Time Buffers

It is necessary to infer hold time buffers in the data path between registers to compensate for any clock skew between clock tree branches in a design. Hold time buffers consume power due to capacitive load. The process of hold time buffer implementation in AVR controllers is optimized to keep the amount of hold time buffers to an absolute minimum.

Toggle Information

Toggle information is collected on simulations of actual application code to identify areas of the design that toggle the most. This information is used by the synthesis tool which focuses to optimize those areas that toggle the most to reduce power consumption.

Low Power Processes and Libraries

Atmel Corporation manufactures AVR microcontrollers using proprietary low-leakage flash processes and design libraries that contain many complex cells. Complex cells have shorter wires that give much lower capacitive loading and less toggling due to an optimized structure with fewer transistors. Figure 5 shows a simple example of a complex cell compared to simple cells.
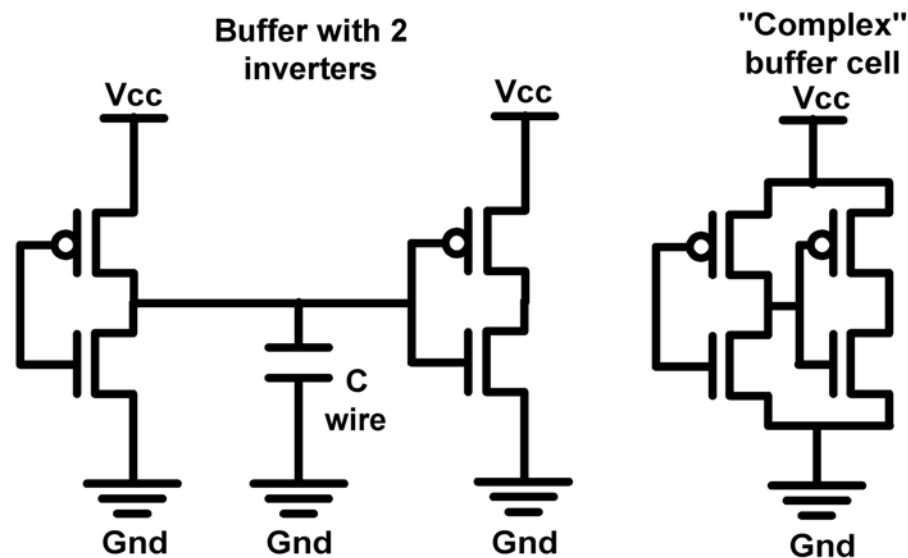

Figure 5: Complex cell example

Ultra Low Power Memory

There is often a trade-off between power consumption and robustness, accuracy, speed and fast start-up time in analog modules. The analog modules therefore require other methods differing from the digital designs to maintain good performance and still achieve low power consumption. AVR MCUs feature high-quality analog modules with more current consumption, but turns them off whenever they are not in use. This approach minimizes current consumption without sacrificing accuracy or performance.

Flash Memory Power Consumption and Flash Sampling

Flash memory is an analog bloc with a static current consumption. Traditional Flash memory designs are always enabled while in active mode. However, at low clock frequencies the Flash read time is less than the clock period so it can be disabled to significantly reduced power consumption. When the clock is running at a few MHz or less, AVR controllers use a technique called "Flash sampling" that enables the Flash for only about 10 nanoseconds to sample the array's contents and then immediately disables it thereby, reducing average power consumption. (Figure 6).
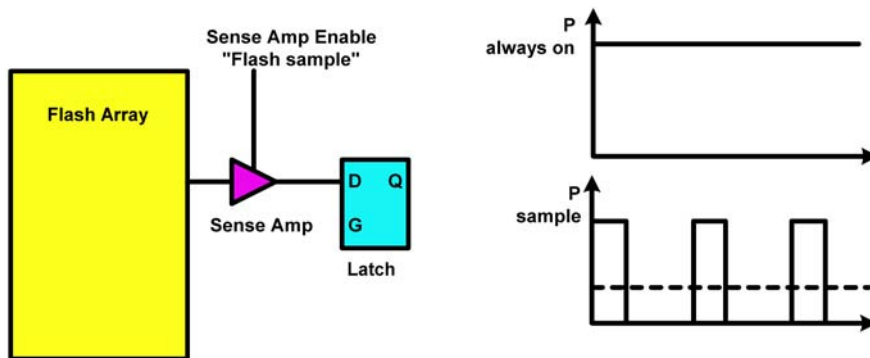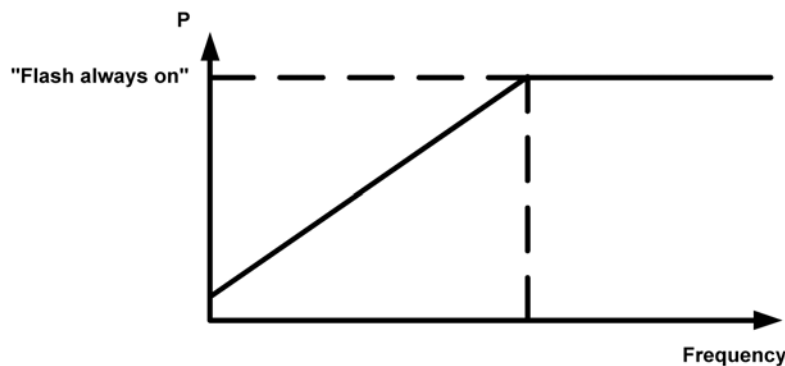

Figure 6: Flash sampling system

Figure 7: Flash Sampling vs Flash Always On

The Flash sampling technique enables a robust, low power Flash design that operates from 1.8 to 5.5V.

True 1.8V Memory Operation

The processes used in AVR MCUs support a power supply voltage range from 1.8 to 5.5V. The 1.8V operation is a true 1.8V operation. This means that all the analog modules, Flash, EEPROM and RAM run at 1.8V enabling really low power applications. The wide power supply range utilizes the complete battery life in a battery-driven application.

Pin Leakage and Digital Input Disable Register

AVR controllers mix ADC and digital I/O on the same pins. Using one ADC and a multiplexed input, the microcontroller scans a number of pins. Multiplexing adds flexibility to low pin-count devices but raises increase power consumption. A digital input is basically built by two transistors, creating an input buffer as shown in Figure 8. As long as valid high or low voltage levels are applied to the buffer, there is no problem. However, applying voltages in the area of Vcc/2 will create a leakage current through the buffer as both transistors will open slightly.
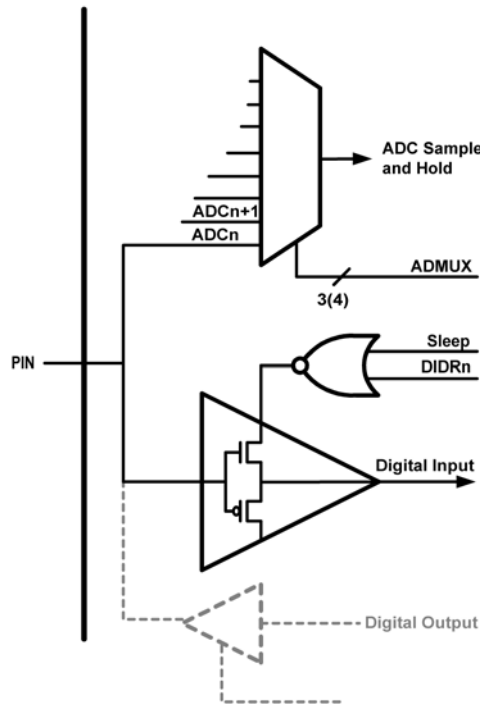

Figure 8: AVR mixed analog and digital I/O

Since the analog voltage level present at the input adds static power consumption, it is important that the microcontroller be able to disable the digital input. Automatic disabling based on the ADC's multiplexer is not possible since the multiplexer is controlled by the microcontroller's firmware and is not predictable by the microcontroller itself. AVR controllers solve this problem with a Dedicated Input Disable Register, DIDR, with one disable bit per analog input.

The digital input buffers are automatically disabled when sleep mode is entered except for those pins used by the input signal to wake the MCU from a sleep mode. The DIDR contributes to decreased overall power consumption.

Conclusion

At the end of the day, power consumption is about numbers and picoPower numbers speak for themselves. The table below compares the leading low-power microcontrollers, TI MSP430Fxxx and Atmel's picoPower AVRs.

Power Save Current Consumption with 32 kHz Running

Device	Typical 2.2V @25°C	Maximum 2.2V @85°C	Comment
MSP430F435	1.1 uA	6 uA	With zero power BOR
MSP430F2131	0.8 uA	2.3 uA	With zero power BOR
ATmega165P	0.65 uA	NA	With Sleeping BOD

Power Down Current Consumption

Device	Typical 3.0V/5.0V @25°C	Maximum 3.0V/5.0V @85°C	Comment
78KO/Kx2 5.0V	NA / 1 uA	NA / 20 uA	3.0V numbers not available
R8C/tiny 3.0/5.0V	0.7 uA/ 0.8 uA	3 uA/ 3 uA	
MSP430F4xxx	0.1 uA / NA	3.5 uA/ NA	Max 3.6V Vcc
MSP430F2xxx	0.1 uA / NA	1.9 uA/ NA	Max 3.6V Vcc
ATmega165P	0.1 uA / 0.6 uA	2 uA/ NA	5.0V numbers not available

Editor's Notes

About Atmel Corporation

Atmel is a worldwide leader in the design and manufacture of microcontrollers, advanced logic, mixed-signal, nonvolatile memory and radio frequency (RF) components. Leveraging one of the industry's broadest intellectual property (IP) technology portfolios, Atmel is able to provide the electronics industry with complete system solutions. Focused on consumer, industrial, security, communications, computing and automotive markets, Atmel ICs can be found Everywhere You Are®

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