

MMBF5460LT1

JFET - General Purpose Transistor

P-Channel

Features

- Pb-Free Package is Available

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|-----------------------------|-----------|-------|------|
| Drain-Gate Voltage | V_{DG} | 40 | Vdc |
| Reverse Gate-Source Voltage | V_{GSR} | 40 | Vdc |
| Forward Gate Current | I_{GF} | 10 | mAdc |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--|-----------------|-------------|----------------------------|
| Total Device Dissipation FR-5 Board, (Note 1) $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 225 1.8 | mW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 556 | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

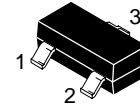
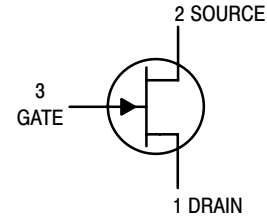
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.062 in.



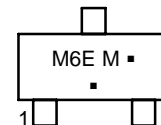
ON Semiconductor®

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SOT-23 (TO-236)
CASE 318
STYLE 10

MARKING DIAGRAM



M6E = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|---------------------|---------------------|
| MMBF5460LT1 | SOT-23 | 3,000 / Tape & Reel |
| MMBF5460LT1G | SOT-23 (Pb-Free) | 3,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MMBF5460LT1

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|---------------|------|-----|------------|-------------------------|
| OFF CHARACTERISTICS | | | | | |
| Gate-Source Breakdown Voltage ($I_G = 10 \mu\text{Adc}$, $V_{DS} = 0$) | $V_{(BR)GSS}$ | 40 | - | - | Vdc |
| Gate Reverse Current ($V_{GS} = 20 \text{Vdc}$, $V_{DS} = 0$) ($V_{GS} = 20 \text{Vdc}$, $V_{DS} = 0$, $T_A = 100^\circ\text{C}$) | I_{GSS} | - | - | 5.0 1.0 | nAdc μAdc |
| Gate Source Cutoff Voltage ($V_{DS} = 15 \text{Vdc}$, $I_D = 1.0 \mu\text{Adc}$) | $V_{GS(off)}$ | 0.75 | - | 6.0 | Vdc |
| Gate Source Voltage ($V_{DS} = 15 \text{Vdc}$, $I_D = 0.1 \text{mAdc}$) | V_{GS} | 0.5 | - | 4.0 | Vdc |
| ON CHARACTERISTICS | | | | | |
| Zero-Gate-Voltage Drain Current ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$) | I_{DSS} | -1.0 | - | -5.0 | mAdc |
| SMALL-SIGNAL CHARACTERISTICS | | | | | |
| Forward Transfer Admittance ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{kHz}$) | $ Y_{fs} $ | 1000 | - | 4000 | μmhos |
| Output Admittance ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{kHz}$) | $ Y_{os} $ | - | - | 75 | μmhos |
| Input Capacitance ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{MHz}$) | C_{iss} | - | 5.0 | 7.0 | pF |
| Reverse Transfer Capacitance ($V_{DS} = 15 \text{Vdc}$, $V_{GS} = 0$, $f = 1.0 \text{MHz}$) | C_{rss} | - | 1.0 | 2.0 | pF |

DRAIN CURRENT versus GATE SOURCE VOLTAGE

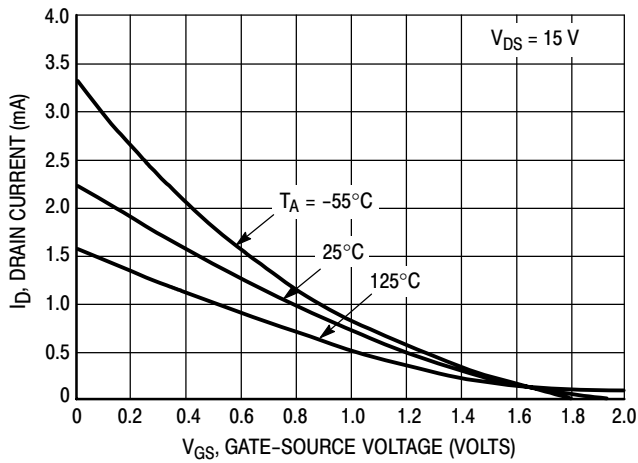


Figure 1. $V_{GS(off)} = 2.0$ Volts

FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

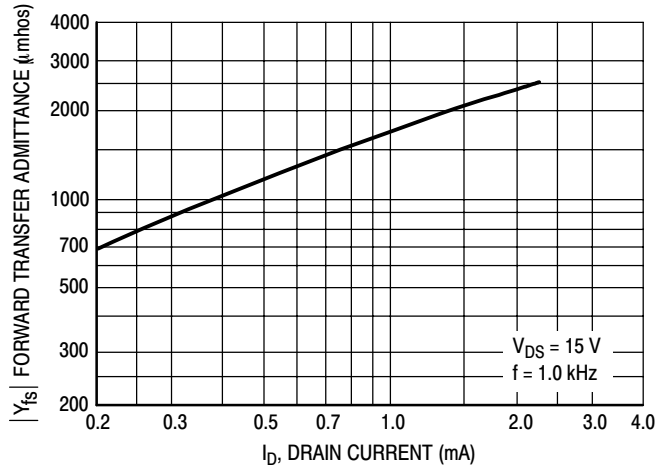


Figure 4. $V_{GS(off)} = 2.0$ Volts

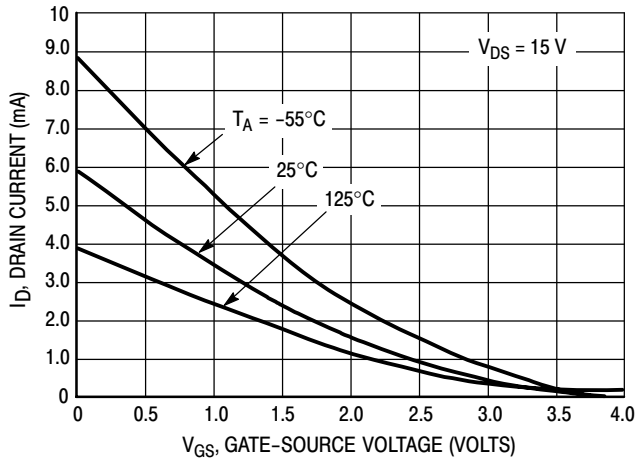


Figure 2. $V_{GS(off)} = 4.0$ Volts

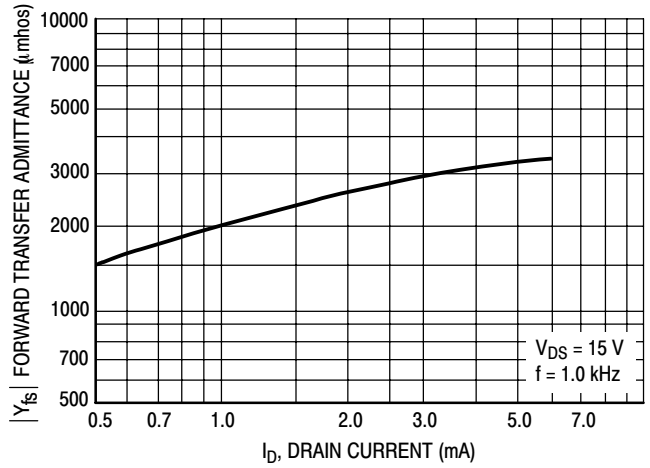


Figure 5. $V_{GS(off)} = 4.0$ Volts

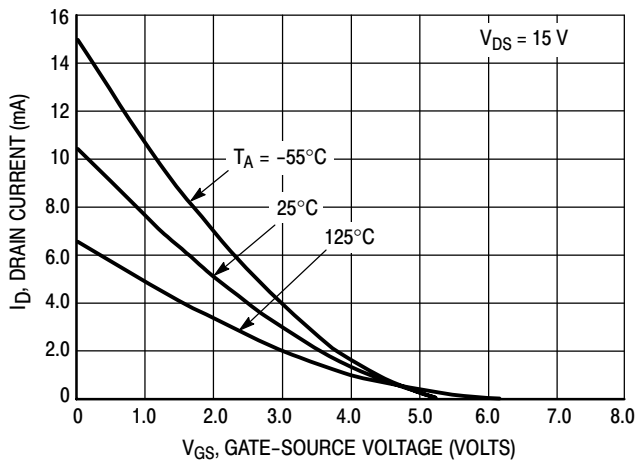


Figure 3. $V_{GS(off)} = 5.0$ Volts

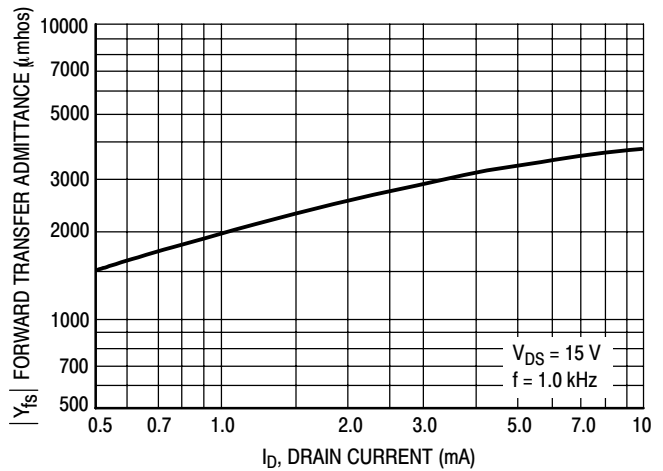


Figure 6. $V_{GS(off)} = 5.0$ Volts

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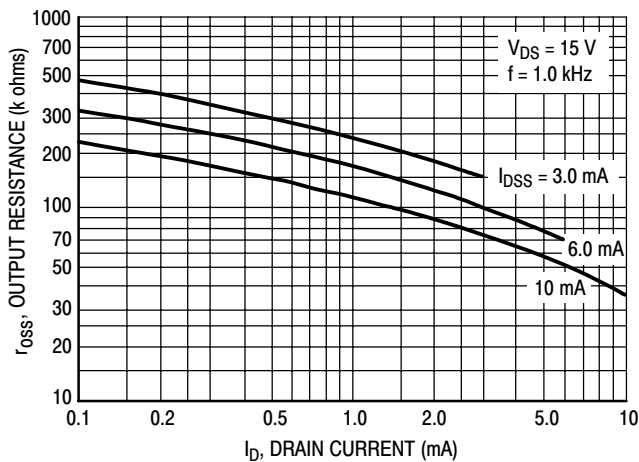


Figure 7. Output Resistance versus Drain Current

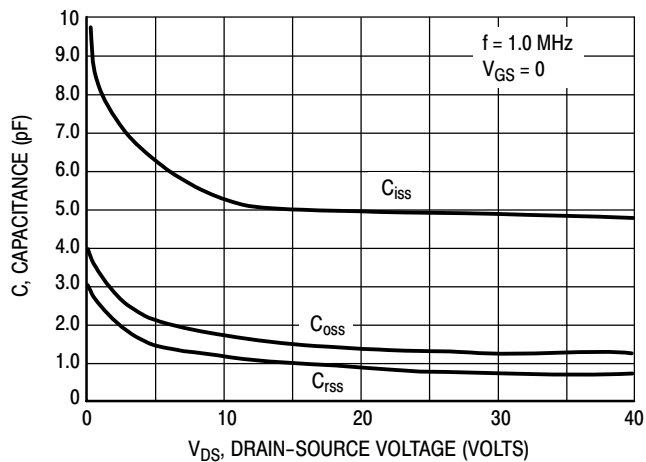


Figure 8. Capacitance versus Drain-Source Voltage

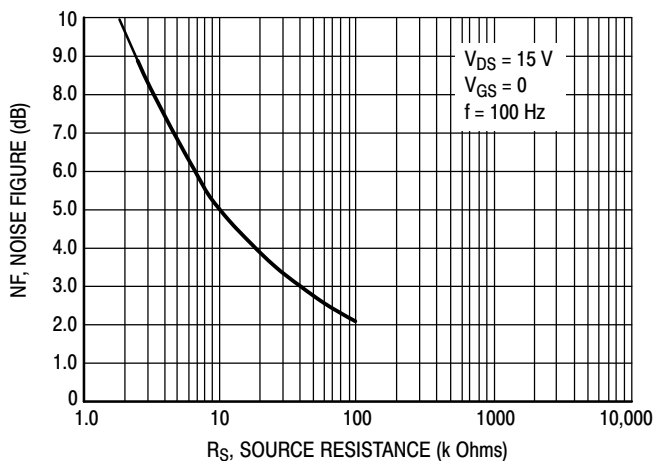
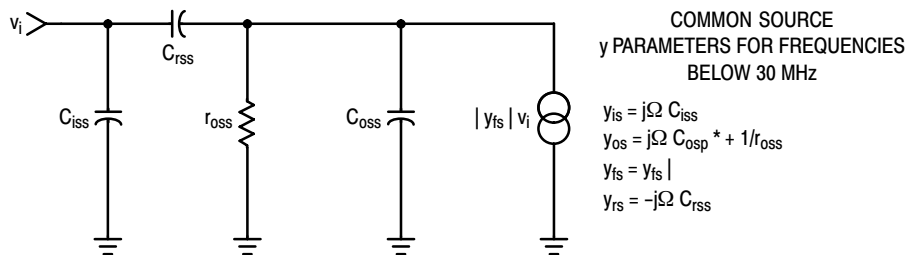


Figure 9. Noise Figure versus Source Resistance



* C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss} .

NOTE:

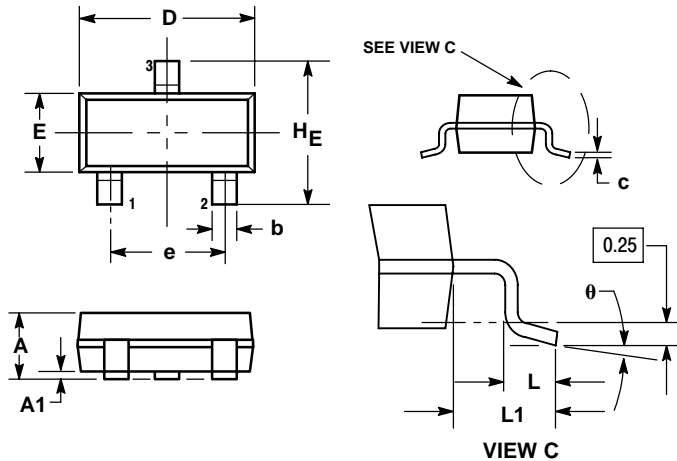
- Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

Figure 10. Equivalent Low Frequency Circuit

MMBF5460LT1

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AN



NOTES:

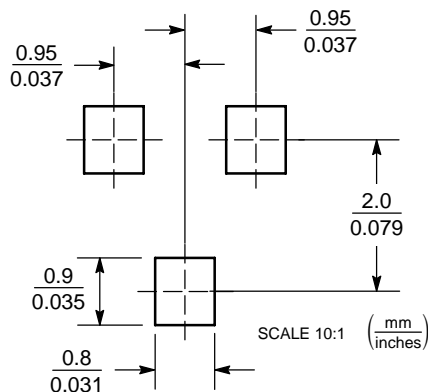
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|--------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.040 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.018 | 0.020 |
| c | 0.09 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.081 |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.029 |
| HE | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |

STYLE 10:

1. DRAIN
2. SOURCE
3. GATE

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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