

High-Side MOSFET Driver

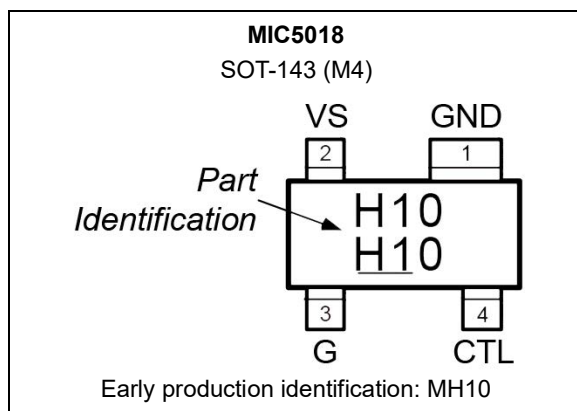
Features

- +2.7V to +9V Operation
- 150 μ A Typical Supply Current at 5V Supply
- ≤ 1 μ A Typical Standby (Off) Current
- Charge Pump for High-Side Low-Voltage Applications
- Internal Zener Diode Gate-to-Ground MOSFET Protection
- Operates in Low- and High-Side Configurations
- TTL Compatible Input
- ESD Protected

Applications

- Battery Conservation
- Power Bus Switching
- Solenoid and Motion Control
- Lamp Control

Package Type



General Description

The MIC5018 high-side MOSFET driver is designed to switch an N-channel enhancement-type MOSFET from a TTL compatible control signal in high- or low-side switch applications. This driver features the tiny 4-lead SOT-143 package.

The MIC5018 is powered from a +2.7V to +9V supply and features extremely low off-state supply current. An internal charge pump drives the gate output higher than the driver supply voltage and can sustain the gate voltage indefinitely. An internal Zener diode limits the gate-to-source voltage to a safe level for standard N-channel MOSFETs.

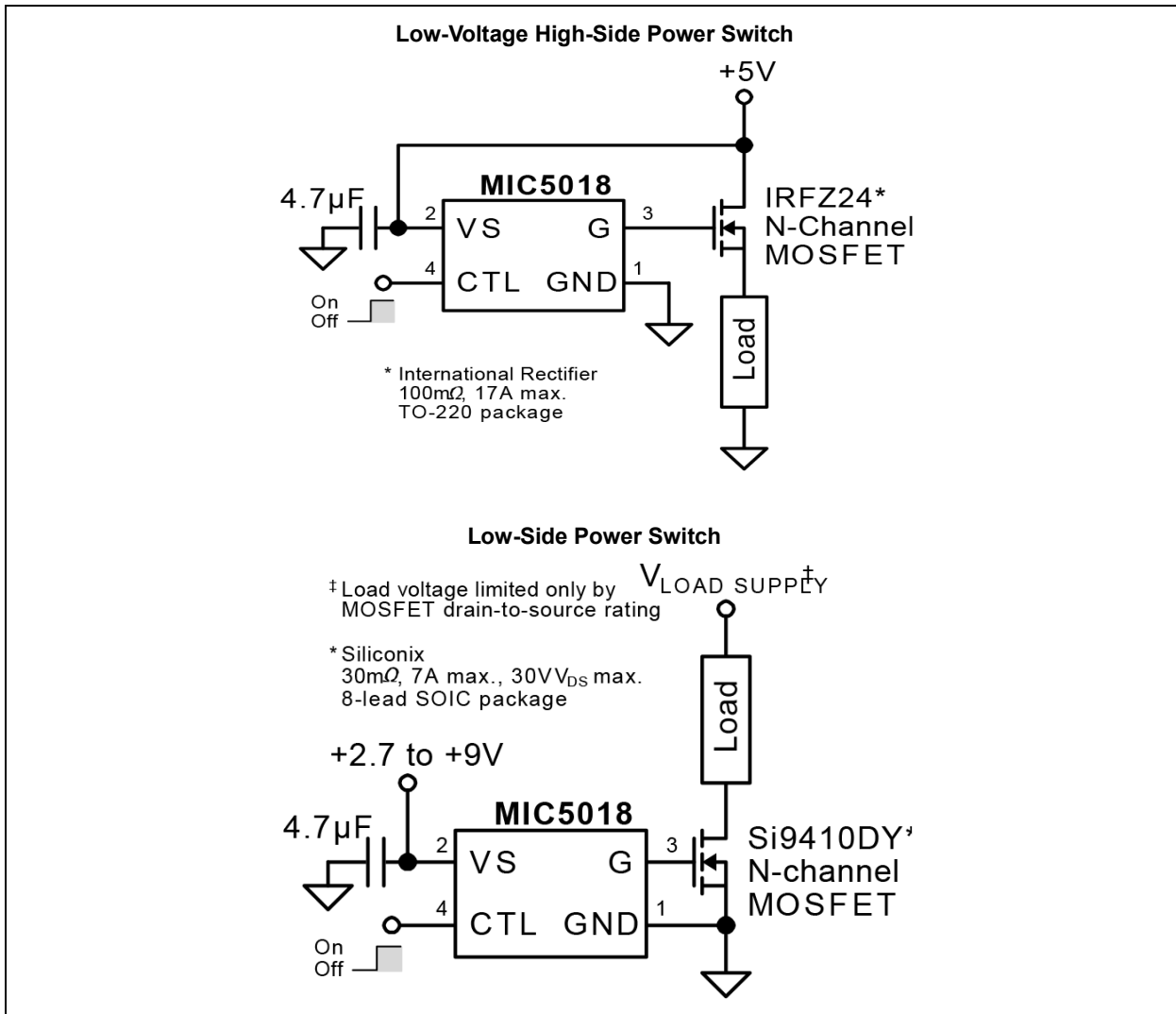
In high-side configurations, the source voltage of the MOSFET approaches the supply voltage when switched on. To keep the MOSFET turned on, the MIC5018's output drives the MOSFET gate voltage higher than the supply voltage. In a typical high-side configuration, the driver is powered from the load supply voltage. Under some conditions, the MIC5018 and MOSFET can switch a load voltage that is slightly higher than the driver supply voltage.

In a low-side configuration, the driver can control a MOSFET that switches any voltage up to the rating of the MOSFET. The gate output voltage is higher than the typical 3.3V or 5V logic supply and can fully enhance a standard MOSFET.

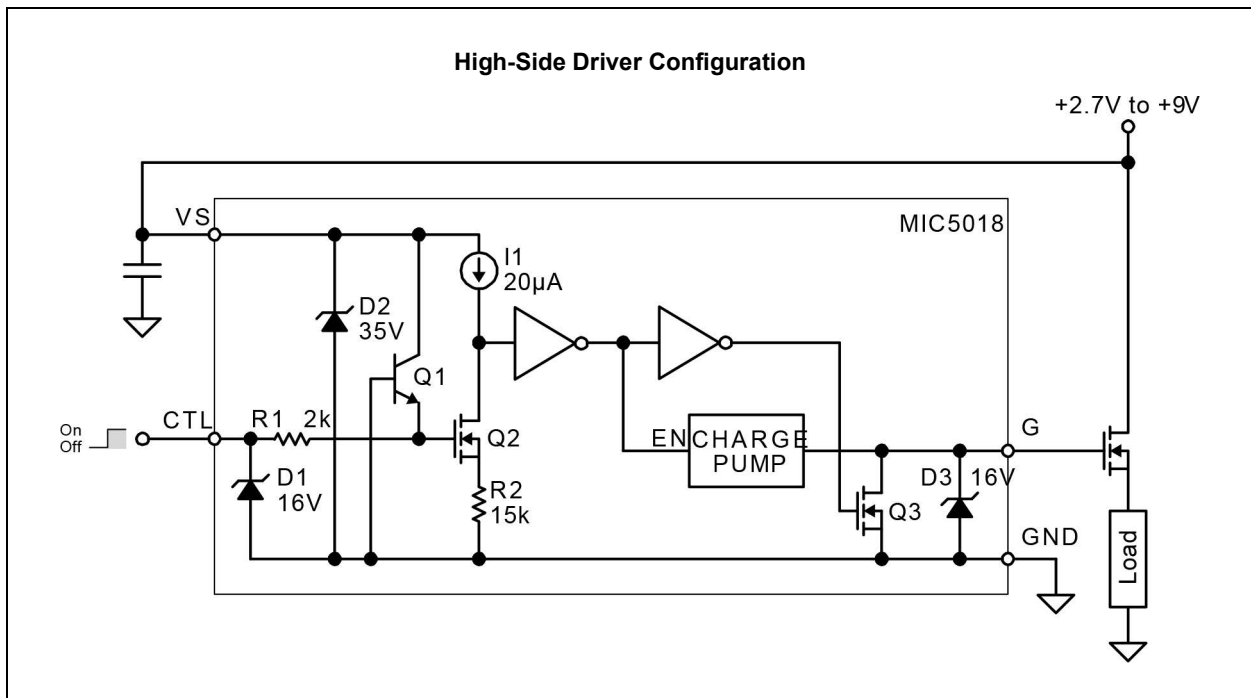
The MIC5018 is available in the SOT-143 package and is rated for -40°C to $+85^{\circ}\text{C}$ ambient temperature range.

MIC5018

Typical Application Circuits



Functional Block Diagram



MIC5018

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Input Voltage (V_{SUPPLY})	+10V
Control Voltage (V_{CTL})	-0.6V to +16V
Gate Voltage (V_G)	+16V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Typical values at $T_A = 25^\circ\text{C}$. Unless otherwise noted, minimum and maximum values indicate performance at $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, with $+2.7\text{V} \leq V_S \leq +9\text{V}$. Parts production tested at 25°C .

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions (Note 1)
Supply Current	I_{SUPPLY}	—	0.01	1	μA	$V_{SUPPLY} = 3.3\text{V}, V_{CTL} = 0\text{V}$
		—	70	140		$V_{SUPPLY} = 3.3\text{V}, V_{CTL} = 3.3\text{V}$
		—	0	1		$V_{SUPPLY} = 5, V_{CTL} = 0\text{V}$
		—	150	300		$V_{SUPPLY} = 5, V_{CTL} = 5\text{V}$
Control Input Voltage	V_{CTL}	0	—	0.8	V	$2.7\text{V} \leq V_{SUPPLY} \leq 9\text{V}, V_{CTL}$ for logic 0 input
		2.0	—	V_{SUPPLY}	V	$2.7\text{V} \leq V_{SUPPLY} \leq 5\text{V}, V_{CTL}$ for logic 1 input
		2.4	—	V_{SUPPLY}	V	$5\text{V} \leq V_{SUPPLY} \leq 9, V_{CTL}$ for logic 1 input
Control Input Current	I_{CTL}	—	0.01	1	μA	$2.7\text{V} \leq V_{SUPPLY} \leq 9\text{V}$
Control Input Capacitance	—	—	5	—	pF	Note 1
Zener Diode Output Clamp	—	13	16	19	V	$V_{SUPPLY} = 9\text{V}$
Gate Output Voltage	V_G	6.3	7.1	—	V	$V_{SUPPLY} = 2.7\text{V}$
		7.1	8.2	—	V	$V_{SUPPLY} = 3.0\text{V}$
		11.4	13.4	—	V	$V_{SUPPLY} = 4.5\text{V}$
Gate Output Current	I_G	—	9.5	—	μA	$V_{SUPPLY} = 5\text{V}, V_{OUT} = 10\text{V}$ (Note 2)
Gate Turn-On Time	—	—	0.75	1.5	ms	$V_{SUPPLY} = 4.5\text{V}, C_L = 1000\text{ pF}$ (Note 3)
	—	—	2.1	4.2	ms	$V_{SUPPLY} = 4.5\text{V}, C_L = 3000\text{ pF}$ (Note 3)
Gate Turn-Off Time	—	—	10	20	μs	$V_{SUPPLY} = 4.5\text{V}, C_L = 1000\text{ pF}$ (Note 4)
	—	—	30	60	μs	$V_{SUPPLY} = 4.5\text{V}, C_L = 3000\text{ pF}$ (Note 4)

Note 1: Guaranteed by design.

2: Resistive load selected for $V_{OUT} = 10\text{V}$.

3: Turn-on time is the time required for gate voltage to rise to 4V greater than the supply voltage. This represents a typical MOSFET gate threshold voltage.

4: Turn-off time is the time required for the gate voltage to fall to 4V above the supply voltage. This represents a typical MOSFET gate threshold voltage.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	-40	—	+85	°C	—
Lead Temperature	—	—	—	+300	°C	Soldering, 10 seconds
Package Thermal Resistance						
Thermal Resistance, SOT-143	θ_{JA}	—	+220	—	°C/W	—
	θ_{JA}	—	+130	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum rating. Sustained junction temperatures above that maximum can impact device reliability.

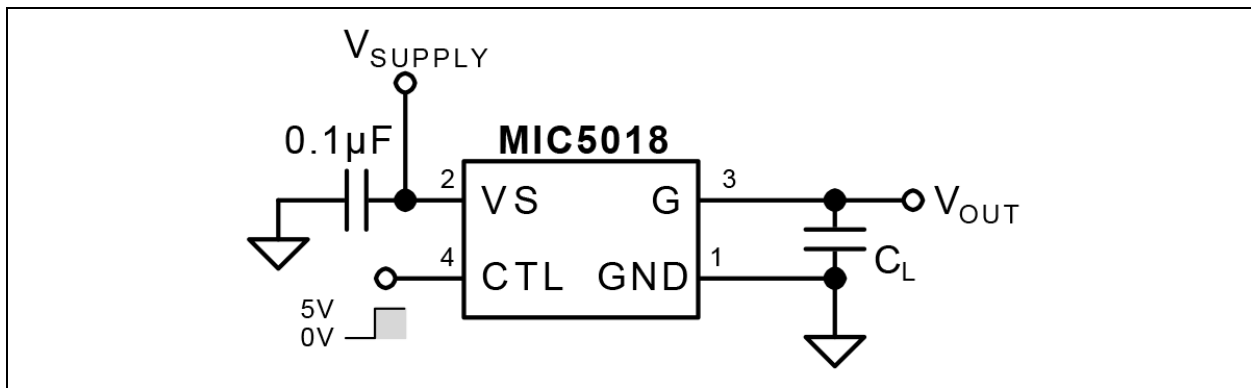


FIGURE 1-1: Test Circuit.

MIC5018

2.0 TYPICAL PERFORMANCE CURVES (Note 1)

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

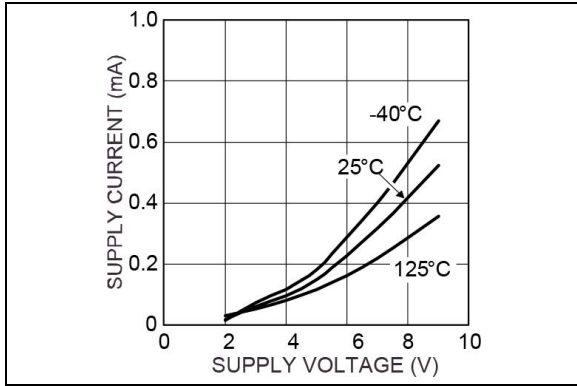


FIGURE 2-1: Supply Current vs. Supply Voltage.

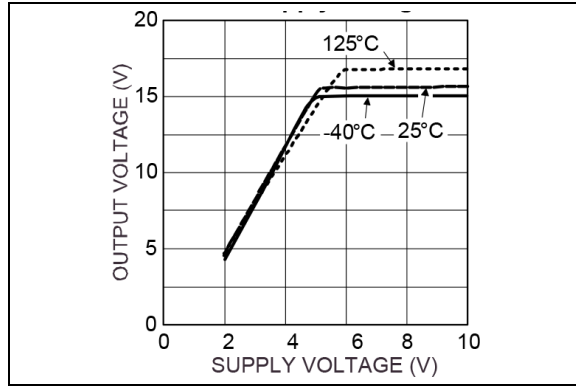


FIGURE 2-4: Gate Output Voltage vs. Supply Voltage.

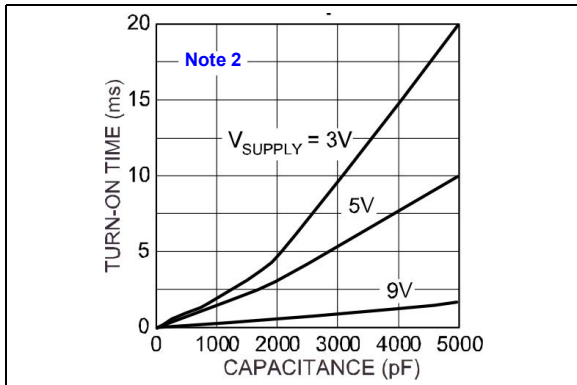


FIGURE 2-2: Full Turn-On Time vs. Load Capacitance.

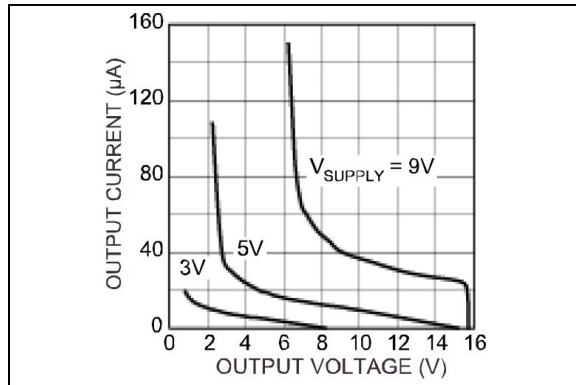


FIGURE 2-5: Gate Output Current vs. Output Voltage.

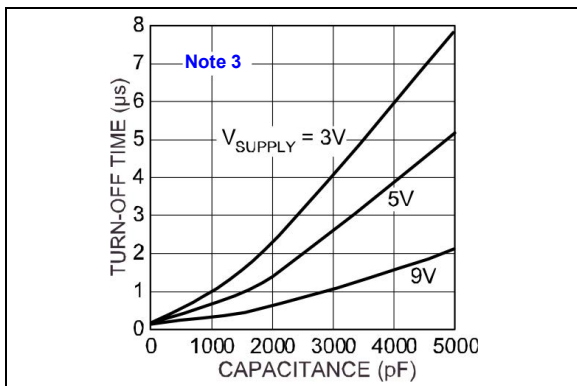


FIGURE 2-3: Full Turn-Off Time vs. Load Capacitance.

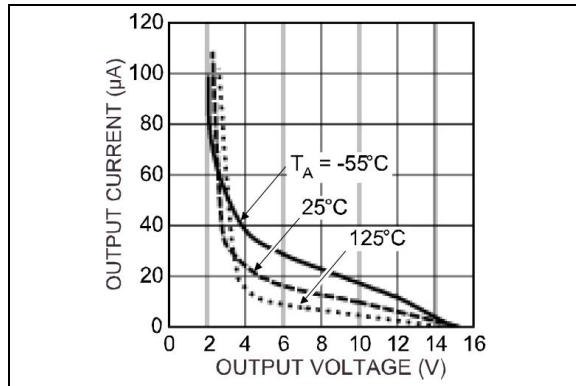


FIGURE 2-6: Gate Output Current vs. Output Voltage.

2.1 Typical Performance Curve Notes

- 1: $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = 5\text{V}$ unless noted.
- 2: Full turn-on time is the time between V_{CTL} rising to 2.5V and the V_G rising to 90% of its steady on-state value.
- 3: Full turn-off time is the time between V_{CTL} falling to 0.5V and the V_G falling to 10% of its steady on-state value.

MIC5018

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number 5-Lead SOT-143	Pin Name	Description
1	GND	Ground: Power return.
2	VS	Supply (Input): +2.7V to +9V supply.
3	G	Gate (Output): Gate connection to external MOSFET.
4	CTL	Control (Input): TTL compatible on/off control input. Logic high drives the gate output above the supply voltage. Logic low forces the gate output near ground.

3.1 Functional Description

Refer to the “**Functional Block Diagram**”.

The MIC5018 is a noninverting device. Applying a logic high signal to CTL (control input) produces gate drive output. The G (gate) output is used to turn on an external N-channel MOSFET.

3.1.1 SUPPLY

VS (supply) is rated for +2.7V to +9V. An external capacitor is recommended to decouple noise.

3.1.2 CONTROL

CTL (control) is a TTL compatible input. CTL must be forced high or low by an external signal. A floating input may cause unpredictable operation.

A high input turns on Q2, which sinks the output of current source I1, making the input of the first inverter low. The inverter output becomes high enabling the charge pump.

3.1.3 CHARGE PUMP

The charge pump is enabled when CTL is logic high. The charge pump consists of an oscillator and voltage quadrupler (4×). Output voltage is limited to 16V by a Zener diode. The charge pump output voltage will be approximately:

EQUATION 3-1:

$$V_G = 4 \times V_{SUPPLY} - 2.8V$$

But not exceeding 16V.

The oscillator operates from approximately 70 kHz to approximately 100 kHz depending upon the supply voltage and temperature.

3.1.4 GATE OUTPUT

The charge pump output is connected directly to the G (gate) output. The charge pump is active only when CTL is high. When CTL is low, Q3 is turned on by the second inverter and discharges the gate of the external MOSFET to force it off.

If CTL is high, and the voltage applied to VS drops to zero, the gate output will be floating (unpredictable).

3.1.5 ESD PROTECTION

D1 and D2 clamp positive and negative ESD voltages. R1 isolates the gate of Q2 from sudden changes on the CTL input. Q1 turns on if the emitter (CTL input) is forced below ground to provide additional input protection. Zener D3 also clamps ESD voltages for the gate (G) output.

4.0 APPLICATION INFORMATION

4.1 Supply Bypass

A capacitor from VS to GND is recommended to control switching and supply transients. Load current and supply lead length are some of the factors that affect capacitor size requirements.

A 4.7 μF or 10 μF aluminum electrolytic or tantalum capacitor is suitable for many applications. The low ESR (equivalent series resistance) of tantalum capacitors makes them especially effective, but also makes them susceptible to uncontrolled inrush current from low impedance voltage sources (such as NiCd batteries or automatic test equipment). Avoid instantaneously applying voltage, capable of high peak current, directly to or near tantalum capacitors without additional current limiting. Normal power supply turn-on (slow rise time) or printed circuit trace resistance is usually adequate for normal product usage.

4.2 MOSFET Selection

The MIC5018 is designed to drive N-channel enhancement type MOSFETs. The gate output (G) of the MIC5018 provides a voltage, referenced to ground, that is greater than the supply voltage. Refer to Figure 2-4.

The supply voltage and the MOSFET drain-to-source voltage drop determine the gate-to-source voltage.

EQUATION 4-1:

$$V_{GS} = V_G - (V_{SUPPLY} - V_{DS})$$

Where:

V_{GS} = gate-to-source voltage (enhancement)

V_G = gate voltage (from graph)

V_{SUPPLY} = supply voltage

V_{DS} = drain-to-source voltage (approx. 0V at low current, or when fully enhanced)

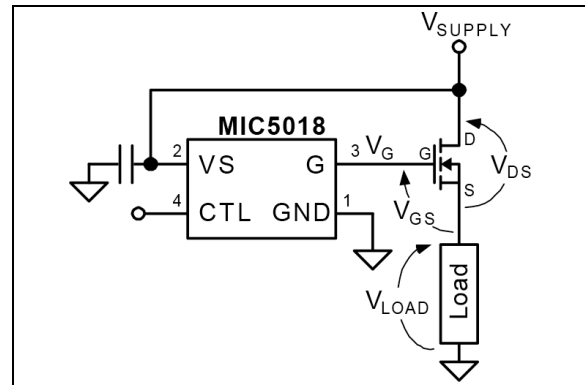


FIGURE 4-1: Voltages

The performance of the MOSFET is determined by the gate-to-source voltage. Choose the type of MOSFET according to the calculated gate-to-source voltage.

4.3 Standard MOSFET

Standard MOSFETs are fully enhanced with a gate-to-source voltage of about 10V. Their absolute maximum gate-to-source voltage is ±20V.

With a 5V supply, the MIC5018 produces a gate output of approximately 15V. Figure 4-2 shows how the remaining voltages conform. The actual drain-to-source voltage drop across an IRFZ24 is less than 0.1V with a 1A load and 10V enhancement. Higher current increases the drain-to-source voltage drop, increasing the gate-to-source voltage.

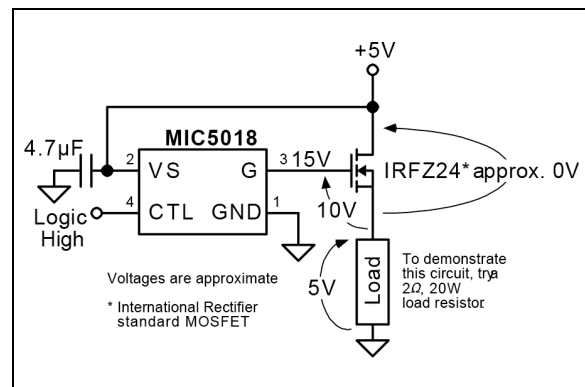


FIGURE 4-2: Using a Standard MOSFET.

The MIC5018 has an internal Zener diode that limits the gate-to-ground voltage to approximately 16V. Lower supply voltages, such as 3.3V, produce lower gate output voltages which will not fully enhance standard MOSFETs. This significantly reduces the maximum current that can be switched. Always refer to the MOSFET data sheet to predict the MOSFET's performance in specific applications.

MIC5018

4.4 Logic-Level MOSFET

Logic-level N-channel MOSFETs are fully enhanced with a gate-to-source voltage of approximately 5V and generally have an absolute maximum gate-to-source voltage of $\pm 10V$.

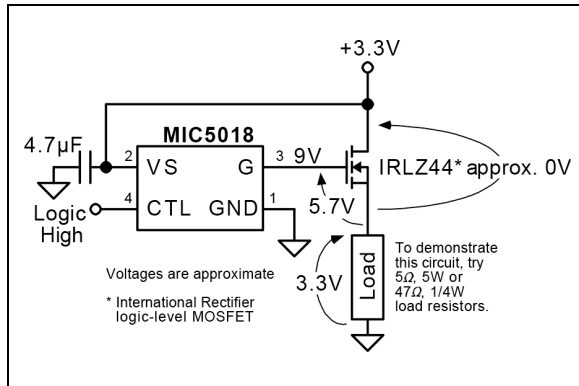


FIGURE 4-3: Using a Logic-Level MOSFET.

Refer to Figure 4-3 for an example showing nominal voltages. The maximum gate-to-source voltage rating of a logic-level MOSFET can be exceeded if a higher supply voltage is used. An external Zener diode can clamp the gate-to-source voltage as shown in Figure 4-4. The Zener voltage, plus its tolerance, must not exceed the absolute maximum gate voltage of the MOSFET.

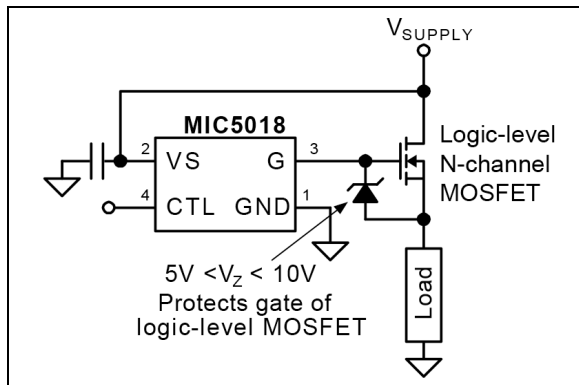


FIGURE 4-4: Gate-to-Source Protection.

A gate-to-source Zener may also be required when the maximum gate-to-source voltage could be exceeded due to normal part-to-part variation in gate output voltage.

Other conditions can momentarily increase the gate-to-source voltage, such as turning on a capacitive load or shorting a load.

4.5 Inductive Loads

Inductive loads include relays, and solenoids. Long leads may also have enough inductance to cause adverse effects in some circuits.

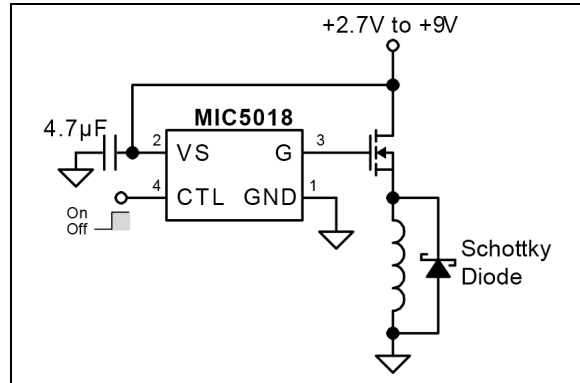


FIGURE 4-5: Switching an Inductive Load.

Switching off an inductive load in a high-side application momentarily forces the MOSFET source negative (as the inductor opposes changes to current). This voltage spike can be very large and can exceed a MOSFET's gate-to-source and drain-to-source ratings. A Schottky diode across the inductive load provides a discharge current path to minimize the voltage spike. The peak current rating of the diode should be greater than the load current.

In a low-side application, switching off an inductive load will momentarily force the MOSFET drain higher than the supply voltage. The same precaution applies.

4.6 Split Power Supply

Refer to Figure 4-6. The MIC5018 can be used to control a 12V load by separating the driver supply from the load supply.

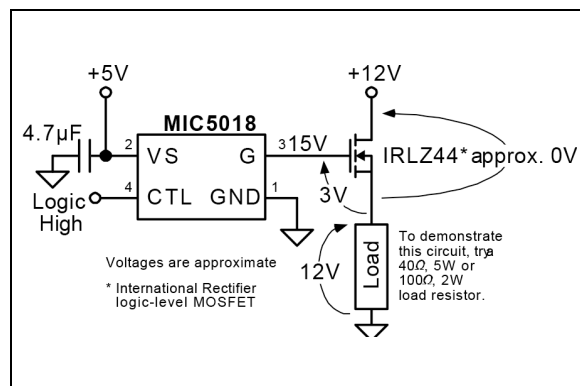


FIGURE 4-6: 12V High-Side Switch.

A logic-level MOSFET is required. The MOSFET's maximum current is limited slightly because the gate is not fully enhanced. To predict the MOSFET's performance for any pair of supply voltages, calculate the gate-to-source voltage and refer to the MOSFET data sheet.

EQUATION 4-2:

$$V_{GS} = V_G - (V_{LDSUPPLY} - V_{DS})$$

V_G is determined from the driver supply voltage using [Figure 2-4](#).

4.7 Low-Side Switch Configuration

The low-side configuration makes it possible to switch a voltage much higher than the MIC5018's maximum supply voltage.

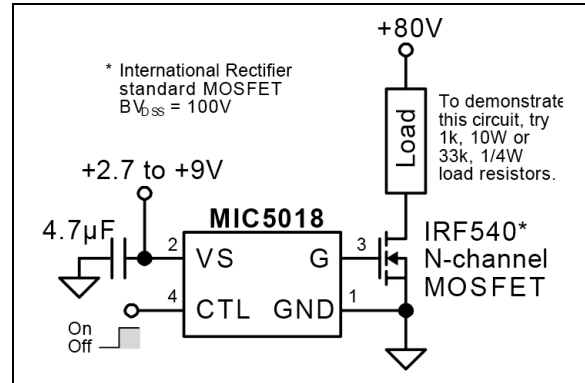


FIGURE 4-7: Low-Side Switch Configuration.

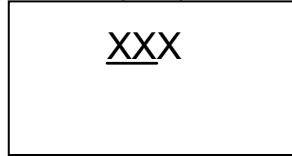
The maximum switched voltage is limited only by the MOSFET's maximum drain-to-source ratings.

MIC5018

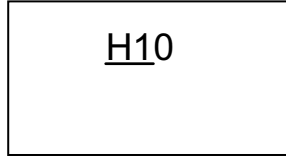
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

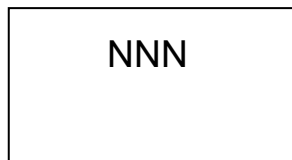
4-Lead SOT-143*
(front)



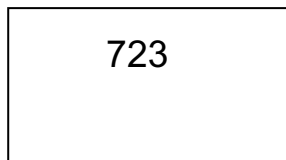
Example



4-Lead SOT-143*
(back)



Example

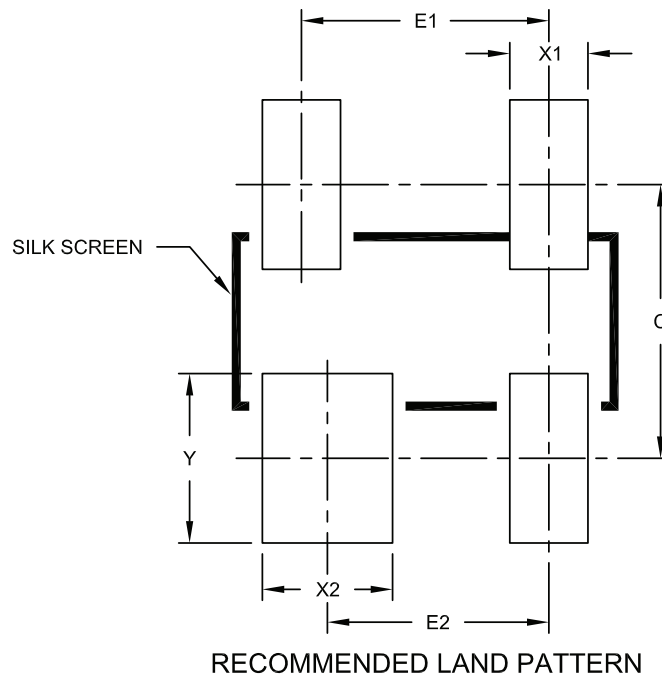


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (˘) symbol may not be to scale.	

4-Lead SOT-143 Package Outline and Recommended Land Pattern

4-Lead Plastic Small Outline Transistor (RC) [SOT-143]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E1	1.90 BSC		
Contact Pitch	E2	1.60 BSC		
Contact Width	X1			0.60
Contact Width	X2			1.00
Contact Length	Y			1.30
Contact Pad Spacing	C		2.10	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

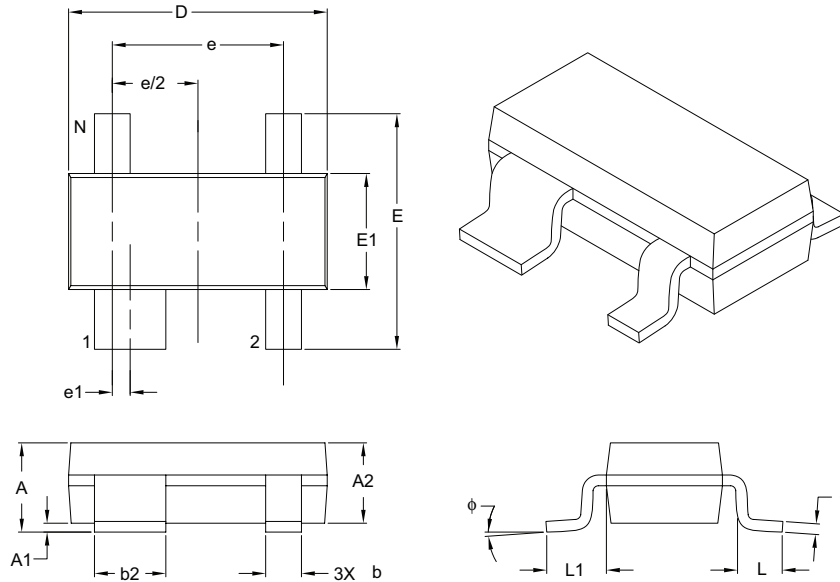
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2031A

MIC5018

4-Lead Plastic Small Outline Transistor (RC) [SOT-143]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	4		
Pitch	e	1.92 BSC		
Lead 1 Offset	e1	0.20 BSC		
Overall Height	A	0.80	–	1.22
Molded Package Thickness	A2	0.75	0.90	1.07
Standoff §	A1	0.01	–	0.15
Overall Width	E	2.10	–	2.64
Molded Package Width	E1	1.20	1.30	1.40
Overall Length	D	2.67	2.90	3.05
Foot Length	L	0.13	0.50	0.60
Footprint	L1	0.54 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.20
Lead 1 Width	b1	0.76	–	0.94
Leads 2, 3 & 4 Width	b	0.30	–	0.54

Notes:

- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-031B

APPENDIX A: REVISION HISTORY

Revision A (December 2021)

- Converted Micrel document MIC5018 to Microchip data sheet DS20006631A.
- Minor text changes throughout.

MIC5018

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART No.</u>	<u>X</u>	<u>XX</u>	<u>-XX</u>	Examples:
Device	Junction Temp. Range	Package	Media Type	a) MIC5018YM4-TR: MIC5018, -40°C to +85°C Temp. Range, 4-Lead SOT-143, 3000/Reel.
Device:	MIC5018:	150mA Low Voltage μ Cap Linear Regulator		
Junction Temperature Range:	Y =	-40°C to +85°C		
Package:	M4 =	4-Lead SOT-143		
Media Type:	-TR =	3000/Reel		Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MIC5018

NOTES:

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- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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