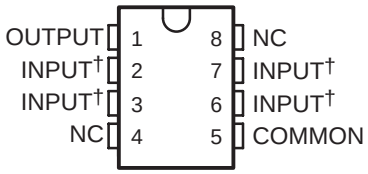
SLVS011D − OCTOBER 1982 − REVISED AUGUST 2003

- **3-Terminal Regulators**
- **Output Current Up To 100 mA**
- **No External Components Required**
- **Internal Thermal-Overload Protection**
- **Internal Short-Circuit Current Limiting**
- **Direct Replacement for Industry-Standard MC79L00 Series**
- **Available in 5% or 10% Selections**

D PACKAGE
(TOP VIEW)



† Internally connected
NC − No internal connection

LP PACKAGE
(TOP VIEW)

description/ordering information

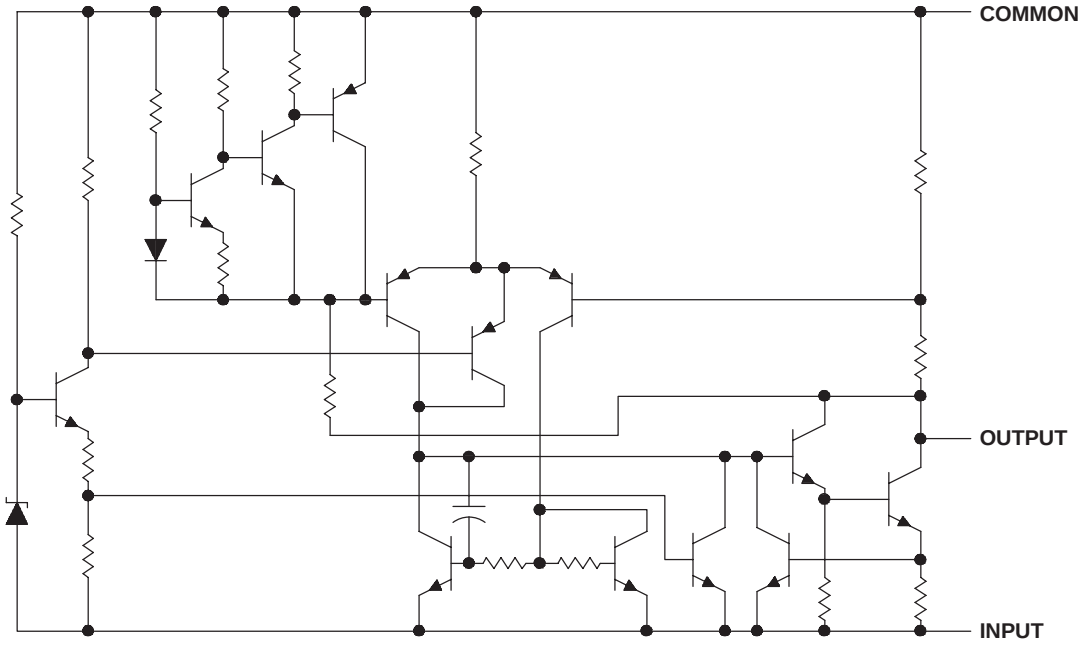
This series of fixed negative-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used to control series pass elements to make high-current voltage-regulator circuits. One of these regulators can deliver up to 100 mA of output current. The internal current-limiting and thermal-shutdown features essentially make the regulators immune to overload. When used as a replacement for a Zener-diode and resistor combination, these devices can provide an effective improvement in output impedance of two orders of magnitude, with lower bias current.

ORDERING INFORMATION

T_J	OUTPUT VOLTAGE TOLERANCE	NOMINAL OUTPUT VOLTAGE (V)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5%	−5	SOIC (D)	Tube of 75	MC79L05ACD	79L05A
				Reel of 2500	MC79L05ACDR	
			TO-226 / TO-92 (LP)	Bulk of 1000	MC79L05ACLP	79L05AC
				Reel of 2000	MC79L05ACLPR	
		−12	SOIC (D)	Tube of 75	MC79L12ACD	79L12A
				Reel of 2500	MC79L12ACDR	
			TO-226 / TO-92 (LP)	Bulk of 1000	MC79L12ACLP	79L12AC
				Reel of 2000	MC79L12ACLPR	
		−15	TO-226 / TO-92 (LP)	Bulk of 1000	MC79L15ACLP	79L15AC
				Ammo of 2000	MC79L15ACLPM	
				Reel of 2000	MC79L15ACLPR	
	10%	−12	TO-226 / TO-92 (LP)	Bulk of 1000	MC79L12CLP	79L12C
		−15	SOIC (D)	Tube of 75	MC79L15CD	79L15C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

equivalent schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage: MC79L05 . . . . . −30 V
MC79L12, MC79L15 . . . . . −35 V
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package . . . . . 97°C/W
LP package . . . . . 140°C/W
Operating free-air, case, or virtual junction temperature . . . . . 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V_I	Input voltage	MC79L05	−7	−20	V
		MC79L12	−14.5	−27	
		MC79L15	−17.5	−30	
I_O	Output current			100	mA
T_J	Operating virtual junction temperature		0	125	°C

electrical characteristics at specified virtual junction temperature, V_I = −10 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J	MC79L05C			MC79L05AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−4.6	−5	−5.4	−4.8	−5	−5.2	V
	V_I = −7 V to −20 V, I_O = 1 mA to 40 mA	0°C to 125°C	−4.5		−5.5	−4.75		−5.25	
	V_I = −10 V, I_O = 1 mA to 70 mA	0°C to 125°C	−4.5		−5.5	−4.75		−5.25	
Input regulation	V_I = −7 V to −20 V	25°C			200			150	mV
	V_I = −8 V to −20 V				150			100	
Ripple rejection	V_I = −8 V to −18 V, f = 120 Hz	25°C	40	49		41	49		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			60			60	mV
	I_O = 1 mA to 40 mA				30			30	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40			40		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6			6	mA
		125°C			5.5			5.5	
Bias current change	V_I = −8 V to −20 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −19 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J	MC79L12C			MC79L12AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−11.1	−12	−12.9	−11.5	−12	−12.5	V
	V_I = −14.5 V to −27 V, I_O = 1 mA to 40 mA	0°C to 125°C	−10.8		−13.2	−11.4		−12.6	
	V_I = −19 V, I_O = 1 mA to 70 mA	0°C to 125°C	−10.8		−13.2	−11.4		−12.6	
Input regulation	V_I = −14.5 V to −27 V	25°C			250			250	mV
	V_I = −16 V to −27 V				200			200	
Ripple rejection	V_I = −15 V to −25 V, f = 120 Hz	25°C	36	42		37	42		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			100			100	mV
	I_O = 1 mA to 40 mA				50			50	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		80			80		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −16 V to −27 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

electrical characteristics at specified virtual junction temperature, V_I = −23 V, I_O = 40 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_J	MC79L15C			MC79L15AC			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage‡		25°C	−13.8	−15	−16.2	−14.4	−15	−15.6	V
	V_I = −17.5 V to −30 V, I_O = 1 mA to 40 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
	V_I = −23 V, I_O = 1 mA to 70 mA	0°C to 125°C	−13.5		−16.5	−14.25		−15.75	
Input regulation	V_I = −17.5 V to −30 V	25°C			300			300	mV
	V_I = −17.5 V to −30 V				250			250	
Ripple rejection	V_I = −18.5 V to −28.5 V, f = 120 Hz	25°C	33	39		34	39		dB
Output regulation	I_O = 1 mA to 100 mA	25°C			150			150	mV
	I_O = 1 mA to 40 mA				75			75	
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90			90		μV
Dropout voltage	I_O = 40 mA	25°C		1.7			1.7		V
Bias current		25°C			6.5			6.5	mA
		125°C			6			6	
Bias current change	V_I = −20 V to −30 V	0°C to 125°C			1.5			1.5	mA
	I_O = 1 mA to 40 mA				0.2			0.1	

† All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output. Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately.
‡ This specification applies only for dc power dissipation permitted by absolute maximum ratings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC79L05ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	Samples
MC79L05ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	Samples
MC79L05ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	Samples
MC79L05ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	Samples
MC79L05ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	Samples
MC79L05ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L05A	Samples
MC79L05ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L05AC	Samples
MC79L05ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L05AC	Samples
MC79L05ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L05AC	Samples
MC79L05ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L05AC	Samples
MC79L12ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	Samples
MC79L12ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	Samples
MC79L12ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	Samples
MC79L12ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	Samples
MC79L12ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 125	79L12A	Samples
MC79L12ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L12AC	Samples
MC79L12ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L12AC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC79L12ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L12AC	Samples
MC79L12ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L12AC	Samples
MC79L12CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L12C	Samples
MC79L15ACLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L15AC	Samples
MC79L15ACLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L15AC	Samples
MC79L15ACLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L15AC	Samples
MC79L15ACLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	79L15AC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

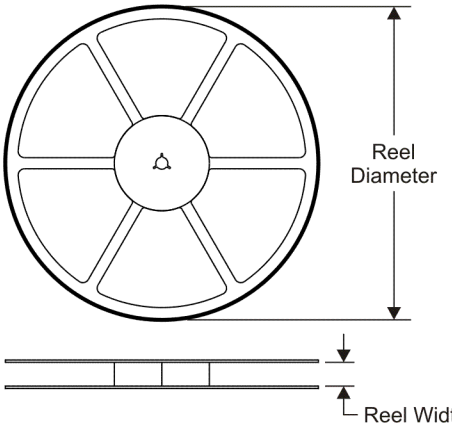
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

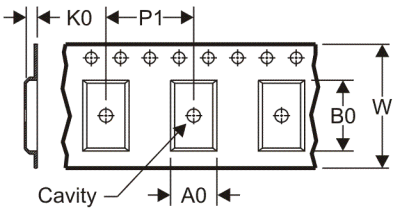
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

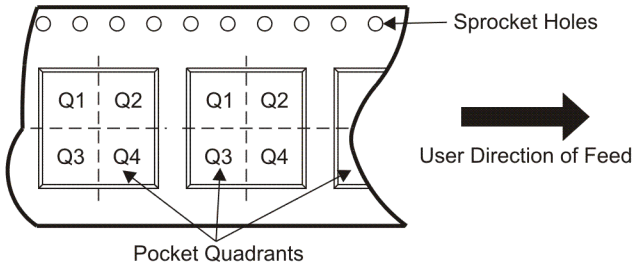


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

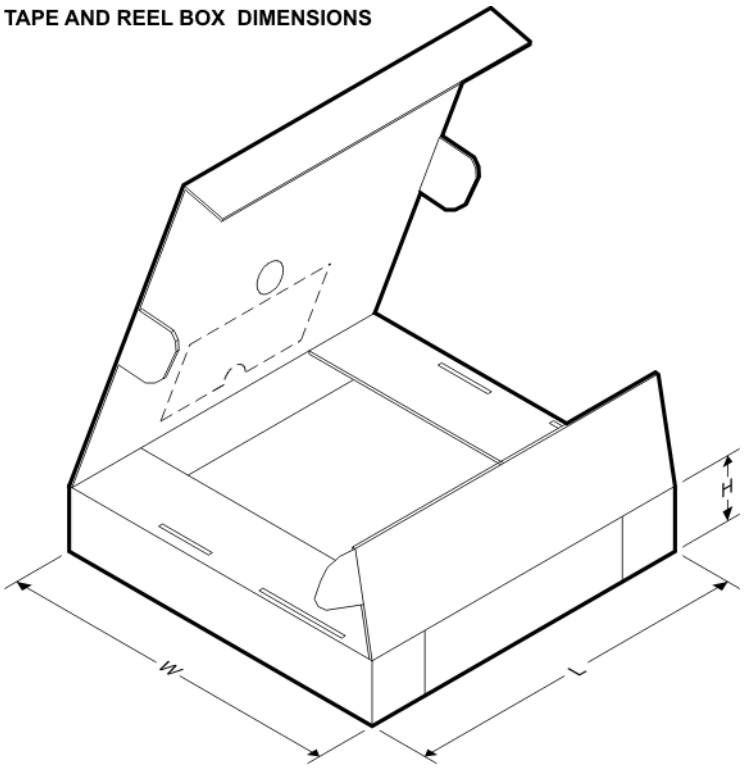
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC79L05ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC79L12ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

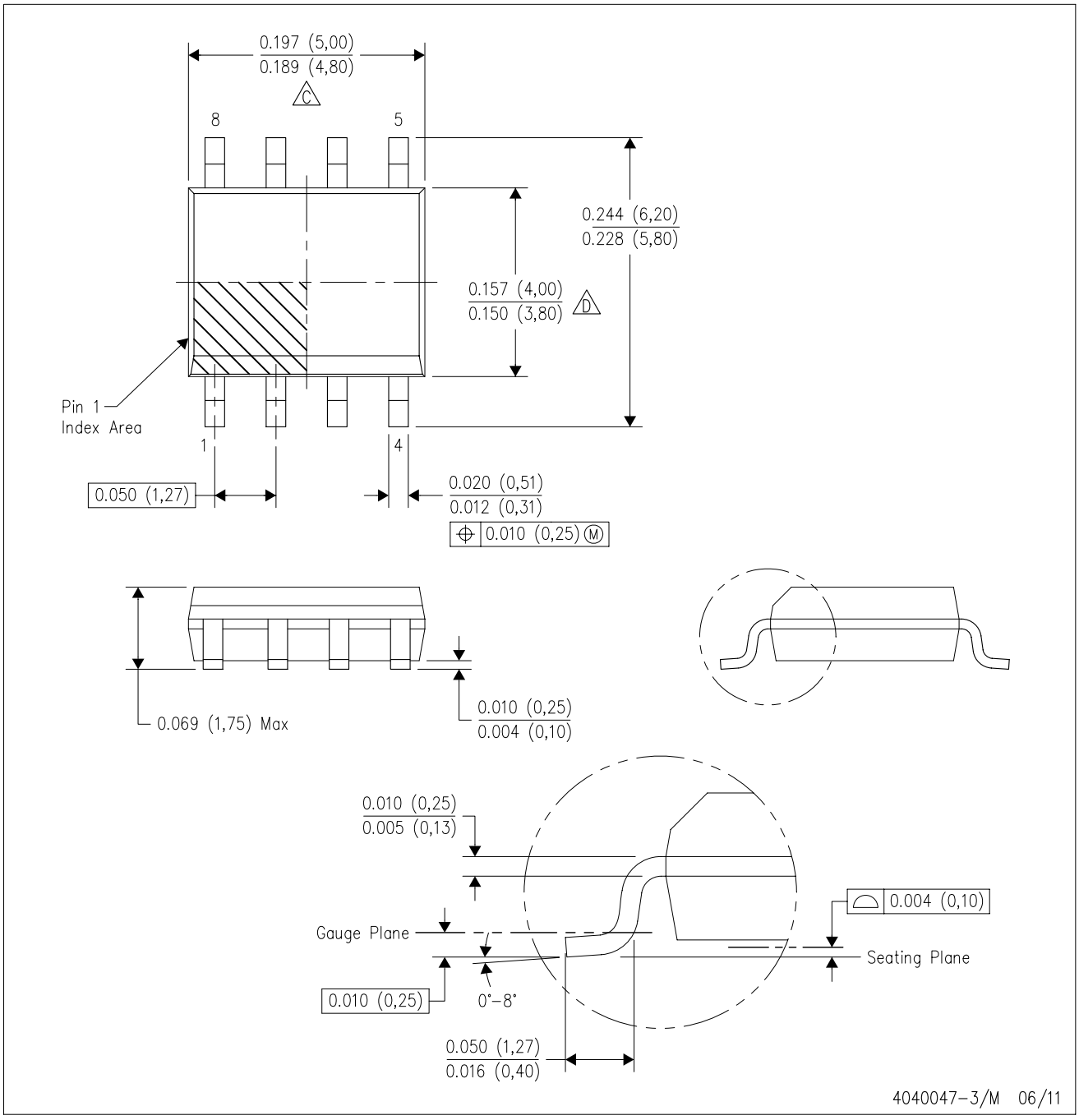
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

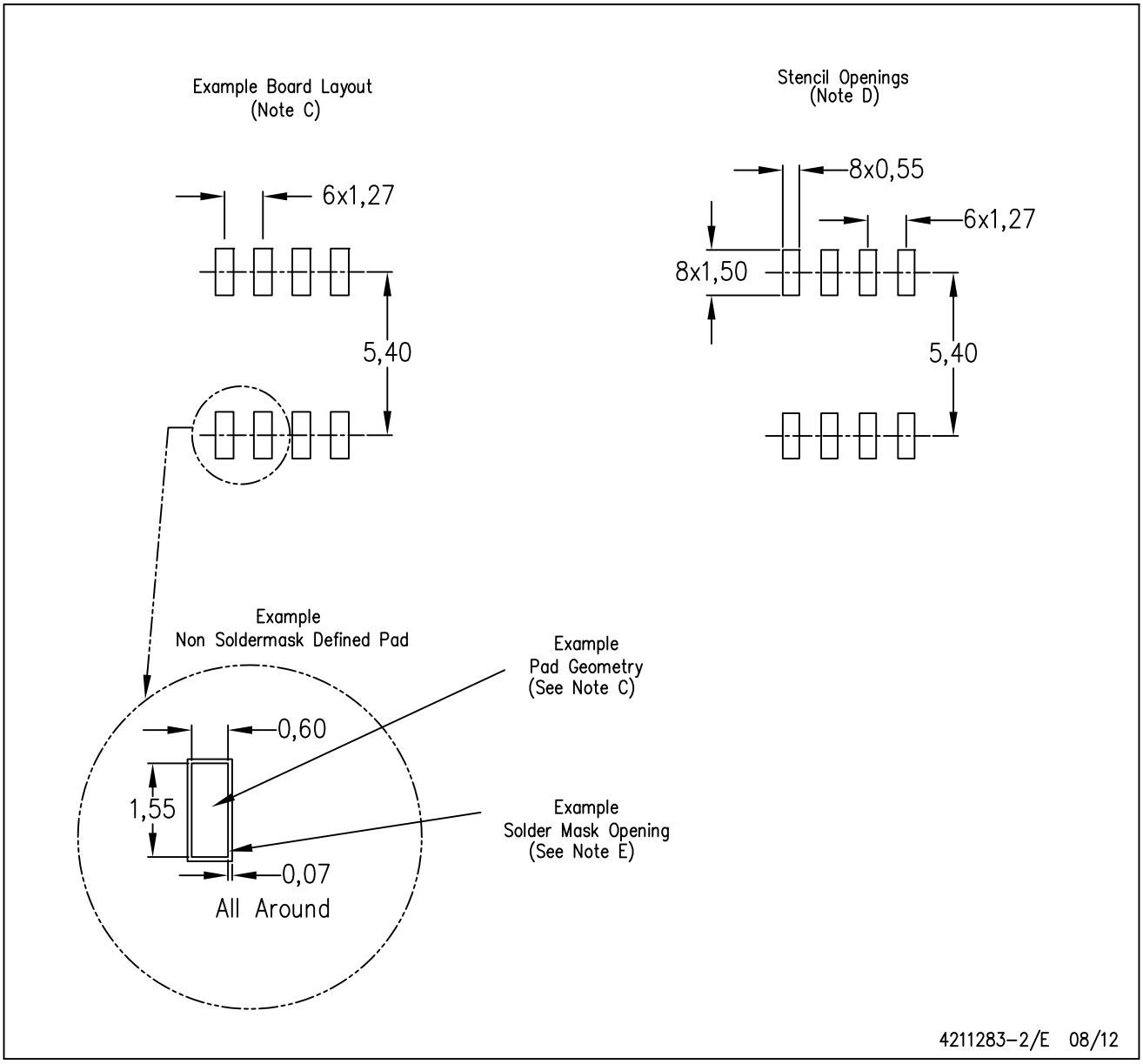
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC79L05ACDR	SOIC	D	8	2500	340.5	338.1	20.6
MC79L12ACDR	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

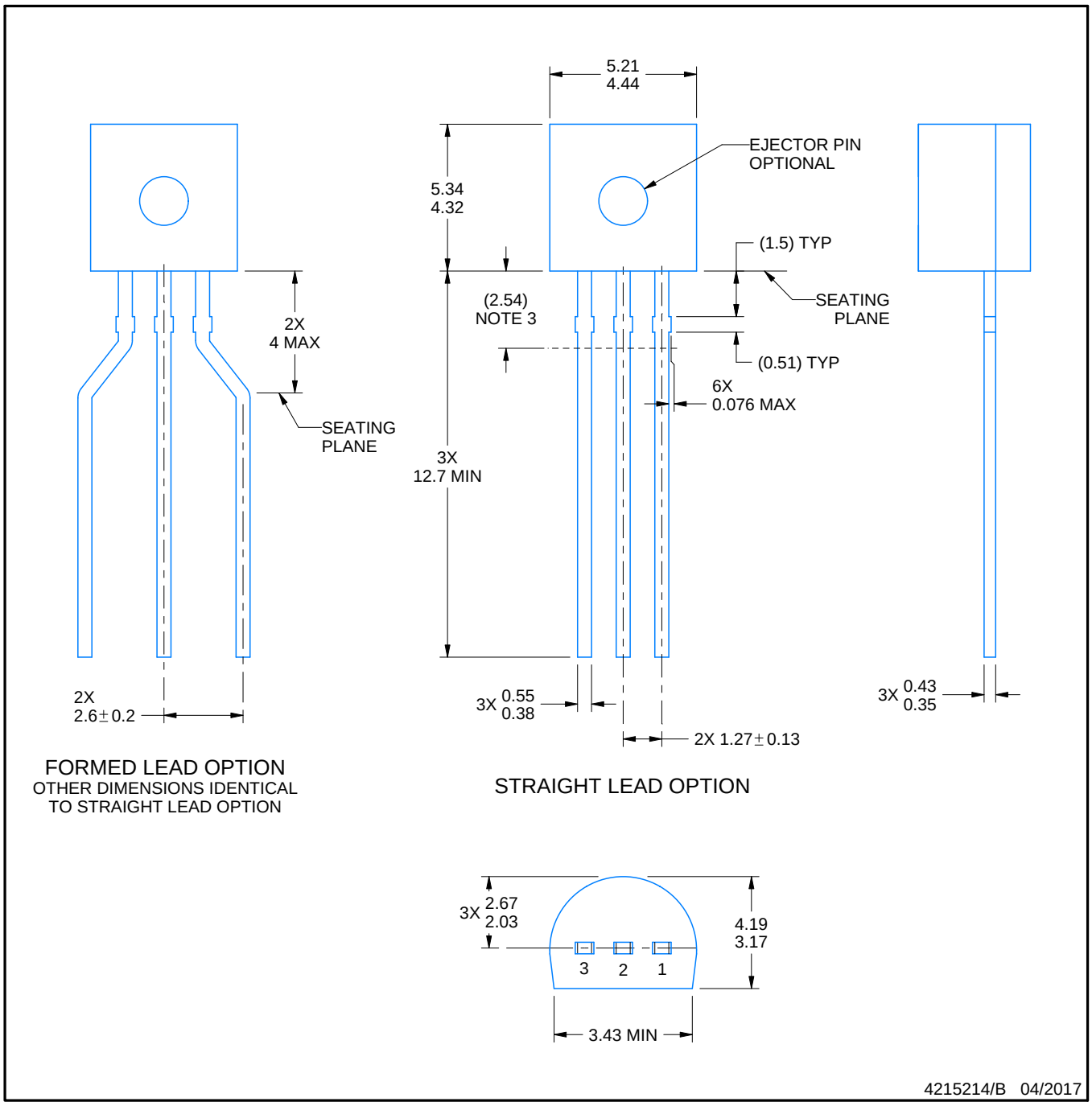
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

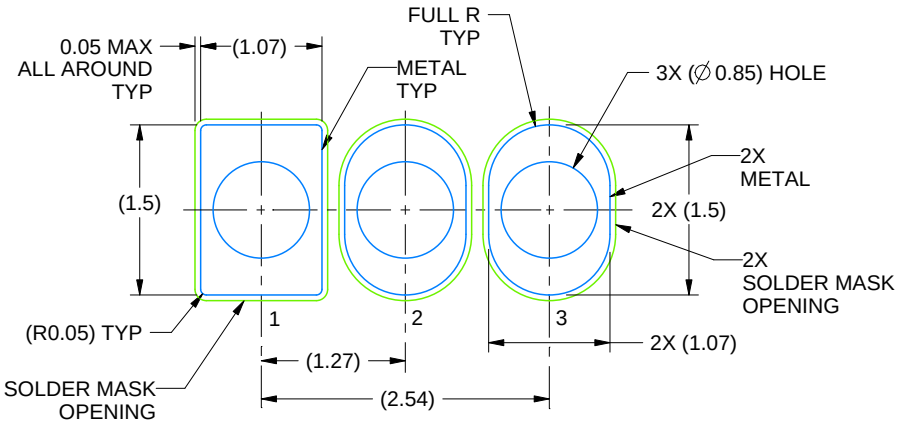
TO-92 - 5.34 mm max height

TO-92

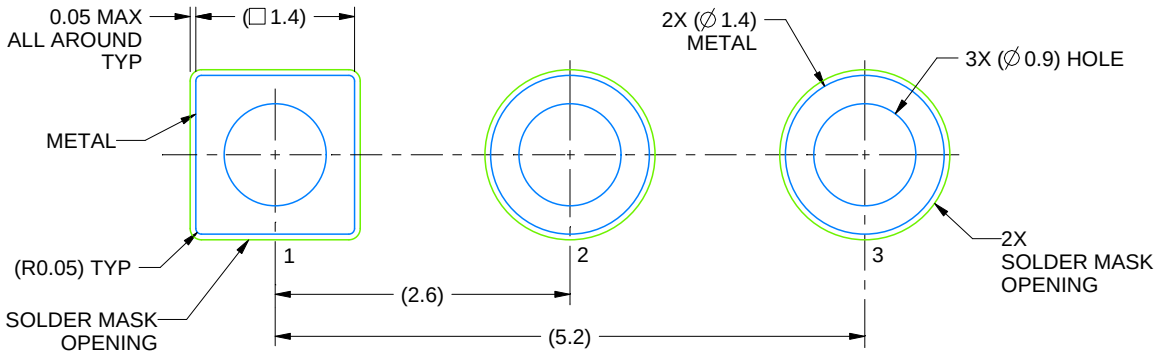


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



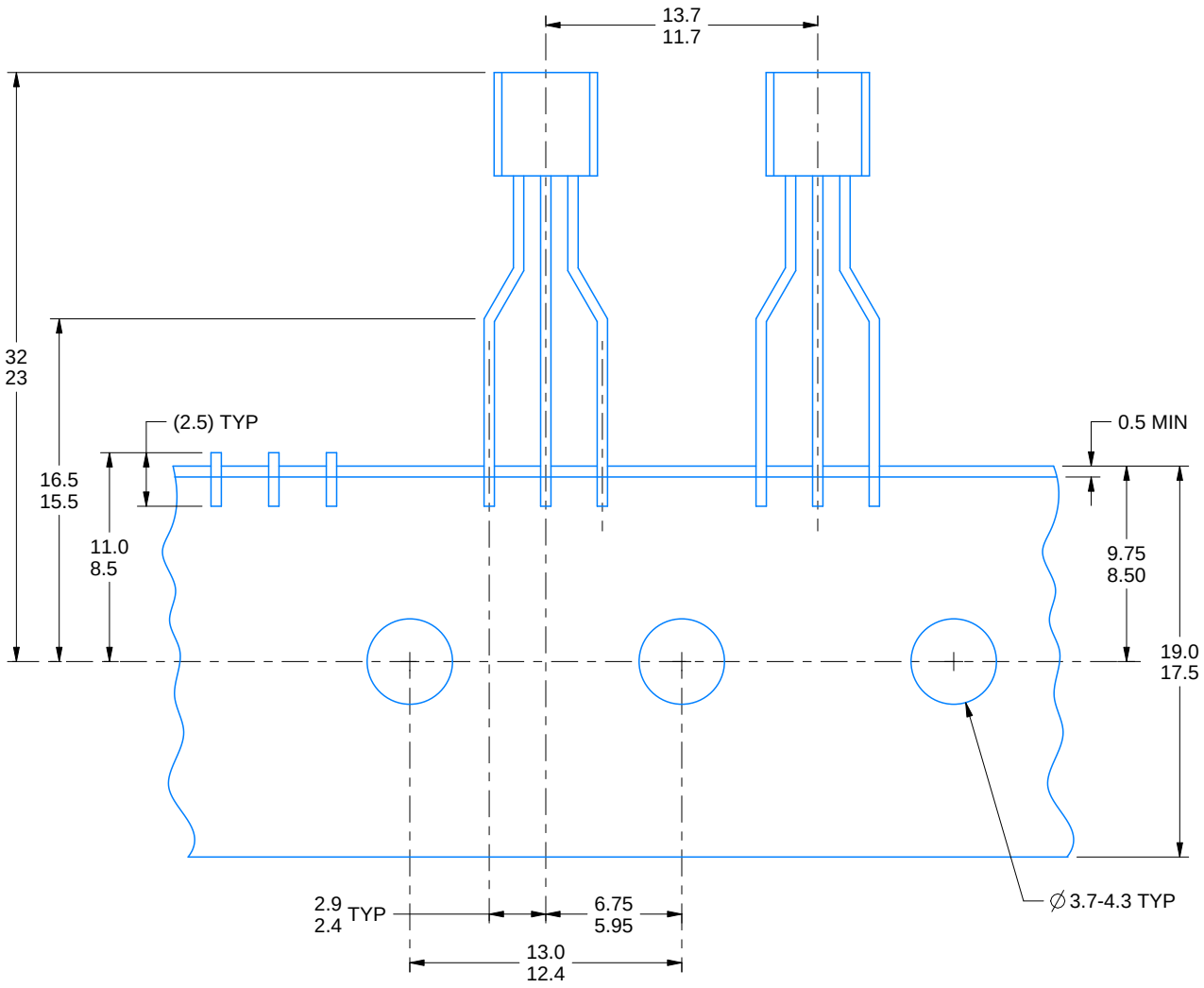
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

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