

Single Non-Inverting Buffer with Open Drain Output

NLV74VHC1G07, NLV74VHC1GT07

The NLV74VHC1G07 / NLV74VHC1GT07 is a single non-inverting buffer with open drain output in tiny footprint packages. The NLV74VHC1G07 has CMOS-level input thresholds while the NLV74VHC1GT07 has TTL-level input thresholds.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits. Some output structures also provide protection when $V_{CC} = 0$ V and when the output voltage exceeds V_{CC} . These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 3.5 ns t_{PD} at 5 V (typ)
- Inputs/Outputs Over-Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 8 mA at 3.0 V
- Available in SC-88A and TSOP-5 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

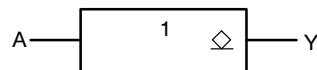
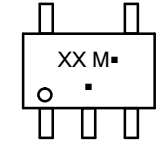


Figure 1. Logic Symbol

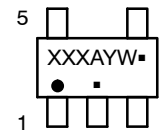
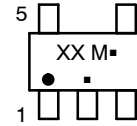


SC-88A
DF SUFFIX
CASE 419A

MARKING DIAGRAMS



TSOP-5
DT SUFFIX
CASE 483



- XX = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

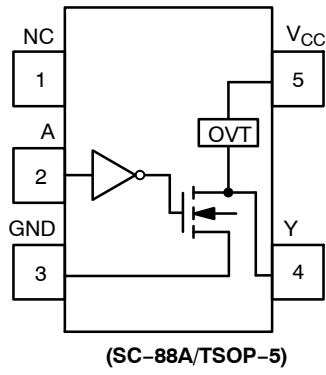


Figure 2. Pinout (Top View)

PIN ASSIGNMENT
 (SC-88A/TSOP-5)

| Pin | Function |
|-----|-----------------|
| 1 | NC |
| 2 | A |
| 3 | GND |
| 4 | Y |
| 5 | V _{CC} |

FUNCTION TABLE

| A Input | Y Output |
|---------|----------|
| L | L |
| H | Z |

MAXIMUM RATINGS

| Symbol | Characteristics | | Value | Unit |
|-------------------------------------|--|-------|---|------|
| V _{CC} | DC Supply Voltage | | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage | | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage | 1Gxx | -0.5 to V _{CC} + 0.5 | V |
| | | 1GTxx | Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V) | |
| I _{IK} | DC Input Diode Current V _{IN} < GND | | -20 | mA |
| I _{OK} | DC Output Diode Current | 1Gxx | V _{OUT} > V _{CC} , V _{OUT} < GND | mA |
| | | 1GTxx | V _{OUT} < GND | |
| I _{OUT} | DC Output Source/Sink Current | | ±25 | mA |
| I _{CC} or I _{GND} | DC Supply Current per Supply Pin or Ground Pin | | ±50 | mA |
| T _{STG} | Storage Temperature Range | | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 secs | | 260 | °C |
| T _J | Junction Temperature Under Bias | | +150 | °C |
| θ _{JA} | Thermal Resistance (Note 2) | | SC-88A | °C/W |
| | | | TSOP-5 | |
| P _D | Power Dissipation in Still Air | | SC-88A | mW |
| | | | TSOP-5 | |
| MSL | Moisture Sensitivity | | Level 1 | - |
| F _R | Flammability Rating Oxygen Index: 28 to 34 | | UL 94 V-0 @ 0.125 in | - |
| V _{ESD} | ESD Withstand Voltage (Note 3) | | Human Body Model | V |
| | | | Charged Device Model | |
| I _{Latchup} | Latchup Performance (Note 4) | | ± 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | | Min | Max | Unit | |
|---------------------------------|-----------------------------|---|---------------------------------|-----------------|------|-----------------|
| V _{CC} | Positive DC Supply Voltage | | 2.0 | 5.5 | V | |
| V _{IN} | DC Input Voltage | | 0 | 5.5 | V | |
| V _{OUT} | DC Output Voltage | 1Gxx | 0 | V _{CC} | V | |
| | | 1GTxx | Active-Mode (High or Low State) | 0 | | V _{CC} |
| | | | Tri-State Mode (Note 1) | 0 | | 5.5 |
| | | Power-Down Mode (V _{CC} = 0 V) | 0 | 5.5 | | |
| T _A | Operating Temperature Range | | -55 | +125 | °C | |
| t _r , t _f | Input Rise and Fall Time | | | | ns/V | |
| | | V _{CC} = 3.0 V to 3.6 V | 0 | 100 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0 | 20 | | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (NLV74VHC1G07)

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|------------------|--------------------------------|---|---------------------|-----------------------|-----|-------|-------------------------------|------|--------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | High-Level Input Voltage | | 2.0 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | 3.0 | 2.1 | - | - | 2.1 | - | 2.1 | - | |
| | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | |
| | | | 5.5 | 3.85 | - | - | 3.85 | - | 3.85 | - | |
| V _{IL} | Low-Level Input Voltage | | 2.0 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | 3.0 | - | - | 0.9 | - | 0.9 | - | 0.9 | |
| | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | |
| | | | 5.5 | - | - | 1.65 | - | 1.65 | - | 1.65 | |
| V _{OL} | Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA I _{OL} = 8 mA | 2.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 3.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | | 4.5 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | | 3.0 | - | - | 0.36 | - | 0.44 | - | 0.52 | |
| | | | 4.5 | - | - | 0.36 | - | 0.44 | - | 0.52 | |
| I _{IN} | Input Leakage Current | V _{IN} = 5.5 V or GND | 2.0 to 5.5 | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | 3-State Output Leakage Current | V _{OUT} = 0 V to 5.5 V | 5.5 | - | - | ±0.25 | - | ±2.5 | - | ±2.5 | μA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = 5.5 V | 0.0 | - | - | 1.0 | - | 10 | - | 10 | μA |
| I _{CC} | Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | - | - | 1.0 | - | 20 | - | 40 | μA |

DC ELECTRICAL CHARACTERISTICS (NLV74VHC1GT07)

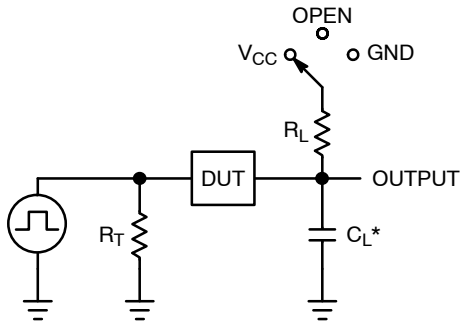
| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|--------------------|--|---|---------------------|-----------------------|-----|-------|-------------------------------|------|--------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | High-Level Input Voltage | | 2.0 | 1.0 | - | | 1.0 | - | 1.0 | - | V |
| | | | 3.0 | 1.4 | - | | 1.4 | - | 1.4 | - | |
| | | | 4.5 | 2.0 | - | | 2.0 | - | 2.0 | - | |
| | | | 5.5 | 2.0 | - | | 2.0 | - | 2.0 | - | |
| V _{IL} | Low-Level Input Voltage | | 2.0 | - | - | 0.28 | - | 0.28 | - | 0.28 | V |
| | | | 3.0 | - | - | 0.45 | - | 0.45 | - | 0.45 | |
| | | | 4.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | |
| | | | 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | |
| V _{OL} | Low-Level Output Voltage | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA I _{OL} = 8 mA | 2.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 3.0 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | | 4.5 | - | 0.0 | 0.1 | - | 0.1 | - | 0.1 | |
| | | | 3.0 | - | - | 0.36 | - | 0.44 | - | 0.52 | |
| | | | 4.5 | - | - | 0.36 | - | 0.44 | - | 0.52 | |
| I _{IN} | Input Leakage Current | V _{IN} = 5.5 V or GND | 2.0 to 5.5 | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | 3-State Output Leakage Current | V _{OUT} = 0 V to 5.5 V | 5.5 | - | - | ±0.25 | - | ±2.5 | - | ±2.5 | μA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = 5.5 V or V _{OUT} = 5.5 V | 0 | - | - | 1.0 | - | 10 | - | 10 | μA |
| I _{CC} | Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | - | - | 1.0 | - | 20 | - | 40 | μA |
| I _{CC(T)} | Increase in Quiescent Supply Current per Input Pin | One Input: V _{IN} = 3.4 V; Other Input at V _{CC} or GND | 5.5 | - | - | 1.35 | - | 1.5 | - | 1.65 | mA |

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | -55°C ≤ T _A ≤ 125°C | | Unit |
|------------------|---|--------------------------------|---------------------|-----------------------|-----|------|-------------------------------|------|--------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PZL} | Propagation Delay, A to Y (Figures 3 and 4) | C _L = 15 pF | 3.0 to 3.6 | - | 5.0 | 7.1 | - | 8.5 | - | 10.0 | ns |
| | | | | - | 7.5 | 10.6 | - | 12.0 | - | 14.5 | |
| | | C _L = 50 pF | 4.5 to 5.5 | - | 3.8 | 5.5 | - | 6.5 | - | 8.0 | |
| | | | | - | 5.3 | 7.5 | - | 8.5 | - | 10.0 | |
| t _{PLZ} | Propagation Delay, A to Y (Figures 3 and 4) | C _L = 15 pF | 3.0 to 3.6 | - | 6.5 | 9.7 | - | 11.5 | - | 12.5 | ns |
| | | | | - | 7.5 | 10.6 | - | 12.0 | - | 14.5 | |
| | | C _L = 50 pF | 4.5 to 5.5 | - | 4.8 | 6.8 | - | 8.0 | - | 9.0 | |
| | | | | - | 5.3 | 7.5 | - | 10.0 | - | 12.0 | |
| C _{IN} | Input Capacitance | | | - | 4.0 | 10 | - | 10 | - | 10 | pF |
| C _{OUT} | Output Capacitance | Output in High Impedance State | | - | 6.0 | - | - | - | - | - | pF |

| | | | |
|-----------------|--|---|----|
| C _{PD} | Power Dissipation Capacitance (Note 5) | Typical @ 25°C, V _{CC} = 5.0 V | pF |
| | | 8.0 | |

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 3. Test Circuit

| Test | Switch Position | C_L , pF | R_L , Ω |
|---------------------|-----------------|------------------------------|------------------|
| t_{PLH} / t_{PHL} | Open | See AC Characteristics Table | X |
| t_{PLZ} / t_{PZL} | V_{CC} | | 1 k |
| t_{PHZ} / t_{PZH} | GND | | 1 k |

X = Don't Care

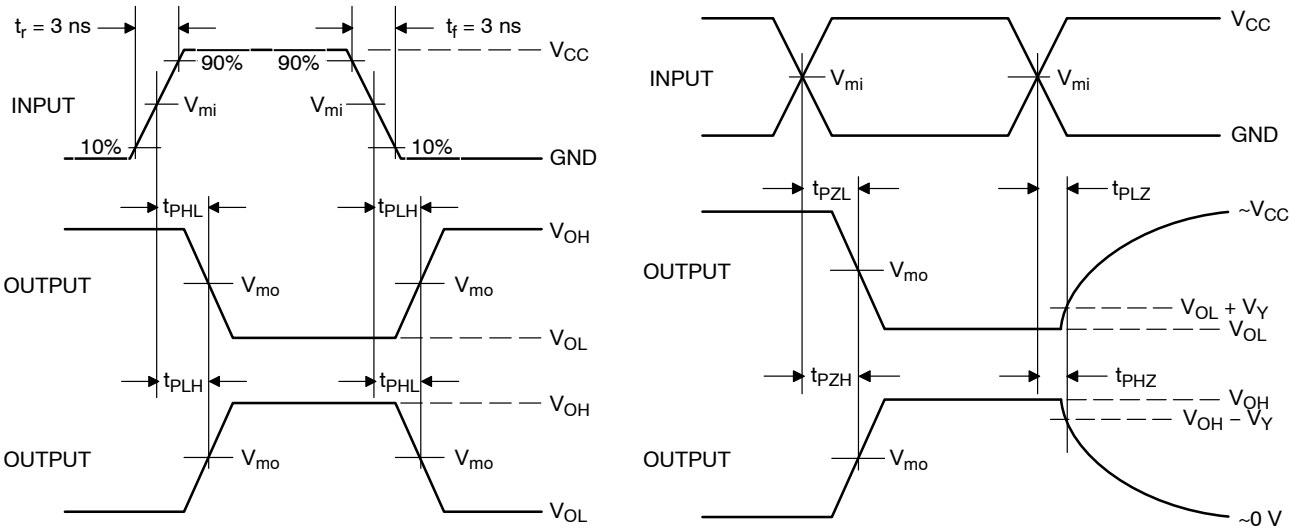


Figure 4. Switching Waveforms

| V_{CC} , V | V_{mi} , V | V_{mo} , V | | V_Y , V |
|--------------|--------------|--------------------|--------------------------------------|-----------|
| | | t_{PLH}, t_{PHL} | $t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$ | |
| 3.0 to 3.6 | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | 0.3 |
| 4.5 to 5.5 | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | 0.3 |

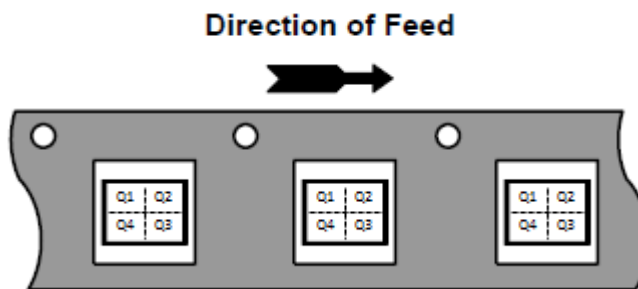
ORDERING INFORMATION

| Device | Packages | Specific Device Code | Pin 1 Orientation (See below) | Shipping [†] |
|-------------------------|----------|----------------------|----------------------------------|-----------------------|
| MC74VHC1G07DFT1G-L22038 | SC-88A | V7 | Q2 | 3000 / Tape & Reel |
| NLVVHC1G07DFT1G* | SC-88A | V7 | Q2 | 3000 / Tape & Reel |
| NLVVHC1G07DFT2G* | SC-88A | V7 | Q4 | 3000 / Tape & Reel |
| MC74VHC1G07DTT1G | TSOP-5 | V7 | Q4 | 3000 / Tape & Reel |
| NLV74VHC1G07DTT1G* | TSOP-5 | V7 | Q4 | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PIN 1 ORIENTATION IN TAPE AND REEL



MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE M

DATE 11 APR 2023



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.95 | 1.10 |
| A1 | --- | --- | 0.10 |
| A3 | 0.20 REF | | |
| b | 0.10 | 0.20 | 0.30 |
| c | 0.10 | --- | 0.25 |
| D | 1.80 | 2.00 | 2.20 |
| E | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| e | 0.65 BSC | | |
| L | 0.10 | 0.15 | 0.30 |

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

STYLE 2:

- PIN 1. ANODE
- EMITTER
- BASE
- COLLECTOR
- CATHODE

STYLE 3:

- PIN 1. ANODE 1
- N/C
- ANODE 2
- CATHODE 2
- CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- DRAIN 1/2
- SOURCE 1
- GATE 1
- GATE 2

STYLE 5:

- PIN 1. CATHODE
- COMMON ANODE
- CATHODE 2
- CATHODE 3
- CATHODE 4

STYLE 6:

- PIN 1. EMITTER 2
- BASE 2
- EMITTER 1
- COLLECTOR
- COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- COLLECTOR
- N/C
- BASE
- EMITTER

STYLE 9:

- PIN 1. ANODE
- CATHODE
- ANODE
- ANODE
- ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | |
|-------------------------|---------------------------------|---|
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| DESCRIPTION: | SC-88A (SC-70-5/SOT-353) | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 2.85 | 3.15 |
| B | 1.35 | 1.65 |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| M | 0° | 10° |
| S | 2.50 | 3.00 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code XXX = Specific Device Code
 A = Assembly Location M = Date Code
 Y = Year ■ = Pb-Free Package
 W = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

| | | |
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