Low-Voltage CMOS Dual D-Type Flip-Flop

With 5 V-Tolerant Inputs

The MC74LCX74 is a high performance, dual D-type flip-flop with asynchronous clear and set inputs and complementary (O, \overline{O}) outputs. It operates from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX74 inputs to be safely driven from 5.0 V devices.

The MC74LCX74 consists of 2 edge-triggered flip-flops with individual D-type inputs. The flip-flop will store the state of individual D inputs, that meet the setup and hold time requirements, on the LOW-to-HIGH Clock (CP) transition.

Features

- Designed for 2.3 V to 3.6 V V_{CC} Operation
- 5.0 V Tolerant Inputs Interface Capability With 5.0 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

1



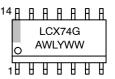
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http://onsemi.com

MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



A = Assembly Location

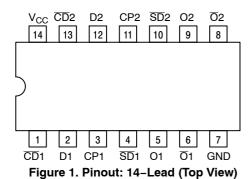
L, WL = Wafer Lot Y, YY = Year

W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.



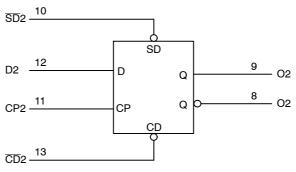


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
CP1, CP2	Clock Pulse Inputs
D1-D2	Data Inputs
CD1, CD2	Direct Clear Inputs
SD1, SD2	Direct Set Inputs
On– O n	Outputs

TRUTH TABLE

	Inp	uts		Outputs		
SDn	CDn	CPn	Dn	On On		Operating Mode
L	Н	Х	Х	Н	L	Asynchronous Set
Н	L	Х	Х	L	Н	Asynchronous Clear
L	L	Х	×	Н	Н	Undetermined
Н	Н	1	h	Н	L	
Н	Н	\uparrow	ı	L	Н	Load and Read Register
Н	Н	1	Х	NC	NC	Hold

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

L = Low Voltage Level

I = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition

NC = No Change

X = High or Low Voltage Level and Transitions are Acceptable

= Low-to-High Transition

1 = Not a Low-to-High Transition

For I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	$-0.5 \le V_1 \le +7.0$		V
Vo	DC Output Voltage	$-0.5 \le V_O \le V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
lok	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
Io	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Type	Max	Units
V _{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
VI	Input Voltage	0		5.5	V
V _O	Output Voltage (HIGH or LOW State)	0		V _{CC}	V
I _{OH}	$ \begin{array}{l} \text{HIGH Level Output Current} \\ \text{$V_{CC} = 3.0 \ V - 3.6 \ V$} \\ \text{$V_{CC} = 2.7 \ V - 3.0 \ V$} \\ \text{$V_{CC} = 2.3 \ V - 2.7 \ V$} \end{array} $			-24 -12 -8	mA
l _{OL}	LOW Level Output Current $V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			+24 +12 +8	mA
T _A	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0		10	ns/V

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LCX74DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LCX74DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCX74DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LCX74DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DC ELECTRICAL CHARACTERISTICS

			T _A = -40°C	to +85°C	
Symbol	Characteristic	Condition	Min	Max	Units
V _{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		8.0	
V _{OH}	HIGH Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OH} = -100 \mu\text{A}$	V _{CC} - 0.2		V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OL} = 100 \mu\text{A}$		0.2	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _{OFF}	Power Off Leakage Current	V _{CC} = 0, V _{IN} = 3.6 V or V _{OUT} = 3.6 V		10	μΑ
I _{IN}	Input Leakage Current	V _{CC} = 0 to 3.6 V, V _{IN} = 3.6 V or GND		±5	μΑ
I _{CC}	Quiescent Supply Current	V _{CC} = 3.6 V, V _{IN} = 3.6 V or V _{OUT} = 3.6 V		10	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_{IH} = V_{CC} - 0.6 \text{ V}$		500	μΑ

^{2.} These values of $V_{\rm I}$ are used to test DC electrical characteristics only.

AC CHARACTERISTICS t_R = t_F = 2.5 ns; R_L = 500 Ω

					Lir	nits			
					T _A = -40°	C to +85°C	;		
			V _{CC} = 3.3	3 V ± 0.3 V	V _{CC} :	= 2.7 V	V _{CC} = 2.5	5 V ± 0.2 V	
			C _L =	50 pF	C _L =	50 pF	C _L =	30 pF	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Units
f _{max}	Clock Pulse Frequency	1	150		150		150		MHz
t _{PLH} t _{PHL}	Propagation Delay CPn to On or On	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	1.5 1.5	8.4 8.4	ns
t _{PLH} t _{PHL}	Propagation Delay SDn or CDn to On or On	2	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0	1.5 1.5	8.4 8.4	ns
t _s	Setup Time, HIGH or LOW Dn to CPn	1	2.5		2.5		4.0		ns
t _h	Hold Time, HIGH or LOW Dn to CPn	1	1.5		1.5		2.0		ns
t _w	CPn Pulse Width, HIGH or LOW SDn or CDn Pulse Width, LOW	4	3.3 3.3		3.3 3.6		4.0 4.0		ns
t _{rec}	Recovery Time SDn or CDn to CPn	3	2.5		3.0		4.5		ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0					ns

^{3.} Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (toshl) or LOW-to-HIGH (toslh); parameter guaranteed by design.

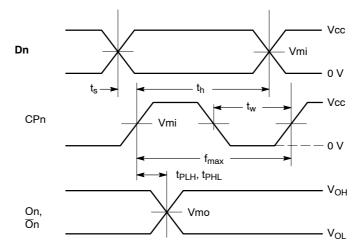
DYNAMIC SWITCHING CHARACTERISTICS

			T _A = +25°C			
Symbol	Characteristic	Condition	Min	Тур	Max	Units
V _{OLP}	Dynamic LOW Peak Voltage (Note 4)	$V_{CC} = 3.3 \text{ V}, C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V} $ $V_{CC} = 2.5 \text{ V}, C_L = 30 \text{ pF}, V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$		0.8 0.6		V V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4)	$\begin{array}{c} V_{CC} = 3.3 \text{ V, } C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{ V, } V_{IL} = 0 \text{ V} \\ V_{CC} = 2.5 \text{ V, } C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{ V, } V_{IL} = 0 \text{ V} \end{array}$		-0.8 -0.6		V

^{4.} Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	7	pF
C _{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_{I} = 0 V or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	25	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES $t_{R}=t_{F}=2.5~\text{ns},~10\%~\text{to}~90\%;~f=1~\text{MHz};~t_{W}=500~\text{ns}$

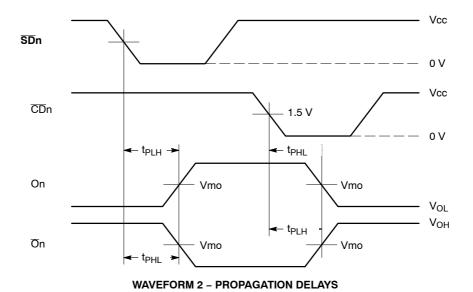
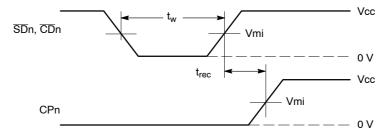


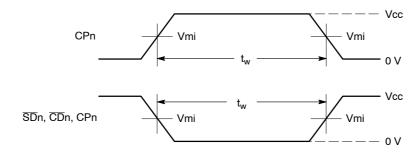
Figure 3. AC Waveforms

 t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 - RECOVERY TIME

 t_R = t_F = 2.5 ns from 10% to 90%; f = 1 MHz; t_w = 500 ns

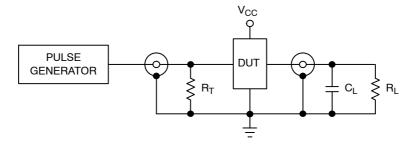


WAVEFORM 4 - PULSE WIDTH

 $t_R = t_F = 2.5$ ns (or fast as required) from 10% to 90%; Output requirements: $V_{OL} \le 0.8 \text{ V}, V_{OH} \ge 2.0 \text{ V}$

	Vcc					
Symbol	3.3 V <u>+</u> 0.3 V	2.7 V	2.5 V <u>+</u> 0.2 V			
Vmi	1.5 V	1.5 V	Vcc/2			
Vmo	1.5 V	1.5 V	Vcc/2			

Figure 3. AC Waveforms (Continued)



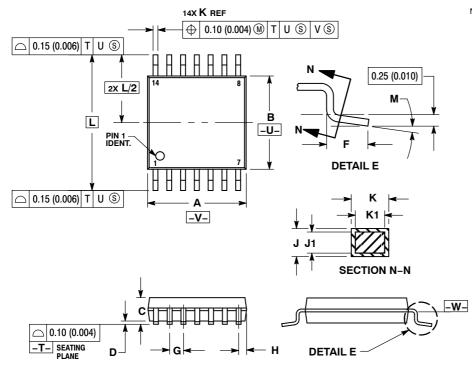
 $C_L=50$ pF at $V_{CC}=3.3\pm0.3$ V or equivalent (includes jig and probe capacitance) $C_L=30$ pF at $V_{CC}=2.5\pm0.2$ V or equivalent (includes jig and probe capacitance) $R_L=R_1=500~\Omega$ or equivalent

 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G-01 **ISSUE B**



NOTES:

- OTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

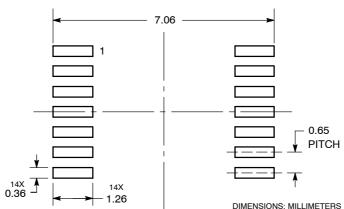
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.08
- DAMBAR PHOTRUSION, ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08
 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
 CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

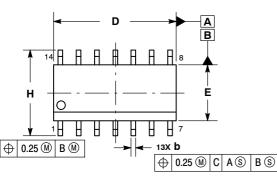
	MILLIN	IETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40		0.252 BSC	
М	0 °	8 °	0 °	8 °

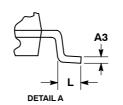
SOLDERING FOOTPRINT

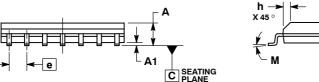


PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 **ISSUE K**







NOTES:

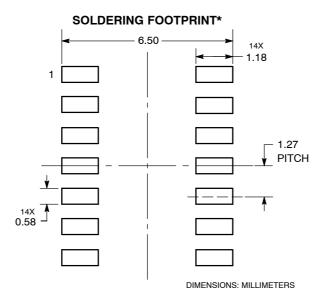
DETAIL A

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR
- PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.

 4. DIMENSIONS D AND E DO NOT INCLUDE
- MOLD PROTRUSIONS.

 MAXIMUM MOLD PROTRUSION 0.15 PER

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
А3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
е	1.27	BSC	0.050	BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7°



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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