

# MC100LVEL17

## 3.3 V ECL Quad Differential Receiver

### Description

The MC100LVEL17 is a 3.3 V ECL, quad differential receiver. The device is functionally equivalent to the E116 device with the capability of operation from either a  $-3.3$  V or  $+3.3$  V supply voltage.

Under open input conditions, the  $\bar{D}$  input will be biased at  $V_{CC}/2$  and the D input will be pulled down to  $V_{EE}$ . This operation will force the Q output LOW and ensure stability.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a  $0.01$   $\mu$ F capacitor and limit current sourcing or sinking to  $0.5$  mA. When not used,  $V_{BB}$  should be left open.

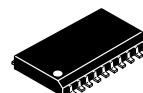
### Features

- 325 ps Propagation Delay
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to  $3.8$  V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Internal Input Pulldown Resistors D Inputs; Pullup and Pulldown on  $\bar{D}$  Inputs
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



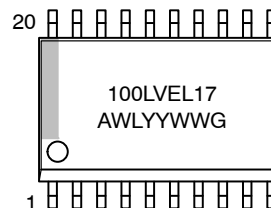
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SOIC-20 WB  
DW SUFFIX  
CASE 751D-05

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

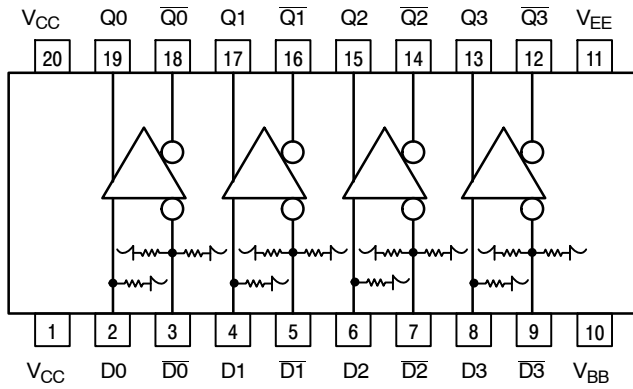
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device           | Package              | Shipping†        |
|------------------|----------------------|------------------|
| MC100LVEL17DWG   | SOIC-20 WB (Pb-Free) | 38 Units / Tube  |
| MC100LVEL17DWR2G | SOIC-20 WB (Pb-Free) | 1000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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**Table 1. PIN DESCRIPTION**

| PIN                          | FUNCTION                      |
|------------------------------|-------------------------------|
| D <sub>n</sub> , $\bar{D}_n$ | ECL Differential Data Inputs  |
| Q <sub>n</sub> , $\bar{Q}_n$ | ECL Differential Data Outputs |
| V <sub>BB</sub>              | Reference Voltage Output      |
| V <sub>CC</sub>              | Positive Supply               |
| V <sub>EE</sub>              | Negative Supply               |

\* All V<sub>CC</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Logic Diagram and Pinout: (Top View)**

**Table 2. ATTRIBUTES**

| Characteristics   | Value                       |
|---|-----------------------------|
| Internal Input Pulldown Resistor  | 75 kΩ                       |
| Internal Input Pullup Resistor  | 75 kΩ                       |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 200 V<br>> 4 kV |
| Moisture Sensitivity, (Note 1)<br>Pb-Free                                   | Level 3                     |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL 94 V-0 @ 0.125 in        |
| Transistor Count  | 141                         |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                             |

1. For additional information, see Application Note [AND8003/D](#).

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**Table 3. MAXIMUM RATINGS**

| Symbol        | Parameter  | Condition 1                                    | Condition 2                            | Rating            | Unit                        |
|---------------|--|--|--|-------------------|-----------------------------|
| $V_{CC}$      | PECL Mode Power Supply                             | $V_{EE} = 0\text{ V}$                          |  | 8 to 0            | V                           |
| $V_{EE}$      | NECL Mode Power Supply                             | $V_{CC} = 0\text{ V}$                          |  | -8 to 0           | V                           |
| $V_I$         | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$<br>$V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>-6 to 0 | V                           |
| $I_{out}$     | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100         | mA                          |
| $I_{BB}$      | $V_{BB}$ Sink/Source                               |  |  | $\pm 0.5$         | mA                          |
| $T_A$         | Operating Temperature Range                        |  |  | -40 to +85        | $^{\circ}\text{C}$          |
| $T_{stg}$     | Storage Temperature Range                          |  |  | -65 to +150       | $^{\circ}\text{C}$          |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-20 WB<br>SOIC-20 WB               | 90<br>60          | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-20 WB                             | 30 to 35          | $^{\circ}\text{C}/\text{W}$ |
| $T_{sol}$     | Wave Solder (Pb-Free)                              | < 2 to 3 sec @ 260 $^{\circ}\text{C}$          |  | 265               | $^{\circ}\text{C}$          |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. LVPECL DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1))

| Symbol      | Characteristic  | -40 $^{\circ}\text{C}$ |      |      | 25 $^{\circ}\text{C}$ |      |      | 85 $^{\circ}\text{C}$ |      |      | Unit          |
|-------------|---|------------------------|------|------|-----------------------|------|------|-----------------------|------|------|---------------|
|             |   | Min                    | Typ  | Max  | Min                   | Typ  | Max  | Min                   | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current  |                        | 26   | 31   |                       | 26   | 31   |                       | 27   | 33   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)  | 2215                   | 2295 | 2420 | 2275                  | 2345 | 2420 | 2275                  | 2345 | 2420 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)   | 1470                   | 1605 | 1745 | 1490                  | 1595 | 1680 | 1490                  | 1595 | 1680 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 2135                   |      | 2420 | 2135                  |      | 2420 | 2135                  |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 1490                   |      | 1825 | 1490                  |      | 1825 | 1490                  |      | 1825 | mV            |
| $V_{BB}$    | Output Voltage Reference  | 1.92                   |      | 2.04 | 1.92                  |      | 2.04 | 1.92                  |      | 2.04 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3)<br>$V_{pp} < 500\text{ mV}$<br>$V_{pp} \geq 500\text{ mV}$ |                        |      |      |                       |      |      |                       |      |      | V             |
|             |   | 1.3                    |      | 2.9  | 1.2                   |      | 2.9  | 1.2                   |      | 2.9  |               |
|             |   | 1.5                    |      | 2.9  | 1.4                   |      | 2.9  | 1.4                   |      | 2.9  |               |
| $I_{IH}$    | Input HIGH Current  |                        |      | 150  |                       |      | 150  |                       |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>Dn<br>$\overline{\text{Dn}}$   | 0.5<br>-300            |      |      | 0.5<br>-300           |      |      | 0.5<br>-300           |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

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**Table 5. LVNECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol      | Characteristic   | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |  | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current   |       | 26    | 31    |       | 26    | 31    |       | 27    | 33    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 2)                                 | -1085 | -1005 | -880  | -1025 | -955  | -880  | -1025 | -955  | -880  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 2)                                  | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                            | -1165 |       | -880  | -1165 |       | -880  | -1165 |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                             | -1810 |       | -1475 | -1810 |       | -1475 | -1810 |       | -1475 | mV            |
| $V_{BB}$    | Output Voltage Reference                                     | -1.38 |       | -1.26 | -1.38 |       | -1.26 | -1.38 |       | -1.26 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) |       |       |       |       |       |       |       |       |       | V             |
|             | $V_{pp} < 500\text{ mV}$                                     | -2.0  |       | -0.4  | -2.1  |       | -0.4  | -2.1  |       | -0.4  |               |
|             | $V_{pp} \geq 500\text{ mV}$                                  | -1.8  |       | -0.4  | -1.9  |       | -0.4  | -1.9  |       | -0.4  |               |
| $I_{IH}$    | Input HIGH Current   |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  |       |       |       |       |       |       |       |       |       | $\mu\text{A}$ |
|             | $D_n$  | 0.5   |       |       | 0.5   |       |       | 0.5   |       |       |               |
|             | $\overline{D}_n$   | -300  |       |       | -300  |       |       | -300  |       |       |               |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

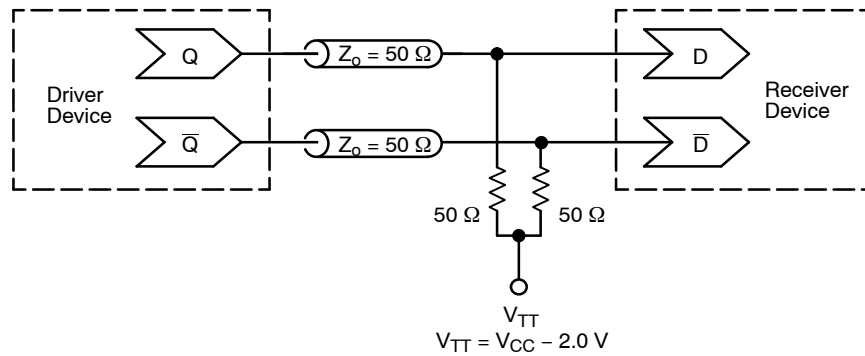
**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 1))

| Symbol       | Characteristic                     | -40°C |     |     | 25°C |      |      | 85°C |     |      | Unit |
|--------------|------------------------------------|-------|-----|-----|------|------|------|------|-----|------|------|
|              |                                    | Min   | Typ | Max | Min  | Typ  | Max  | Min  | Typ | Max  |      |
| $f_{max}$    | Maximum Toggle Frequency           |       |     |     |      | 1.75 |      |      |     |      | GHz  |
| $t_{PLH}$    | Propagation Delay                  |       |     |     |      |      |      |      |     |      | ps   |
| $t_{PHL}$    | D to Q                             | Diff  | 330 |     | 530  |      | 550  | 360  |     | 560  |      |
|              |                                    | S.E.  | 280 |     | 580  |      | 600  | 310  |     | 610  |      |
| $t_{SKEW}$   | Skew                               |       |     |     |      |      |      |      |     |      | ps   |
|              | Output-to-Output (Note 2)          |       |     |     | 75   |      | 75   |      |     | 75   |      |
|              | Part-to-Part (Diff) (Note 2)       |       |     |     | 200  |      | 200  |      |     | 200  |      |
|              | Duty Cycle (Diff) (Note 3)         |       |     |     | 25   |      | 25   |      |     | 25   |      |
| $t_{JITTER}$ | Random Clock Jitter (RMS)          |       |     |     |      | 0.7  |      |      |     |      | ps   |
| $V_{PP}$     | Input Swing (Note 4)               |       | 150 |     | 1000 |      | 1000 | 150  |     | 1000 | mV   |
| $t_r$        | Output Rise/Fall Times Q (20%–80%) |       | 280 |     | 550  |      | 550  | 280  |     | 550  | ps   |
| $t_f$        |                                    |       |     |     |      |      |      |      |     |      |      |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
3. Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.
4.  $V_{PP(min)}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

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**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

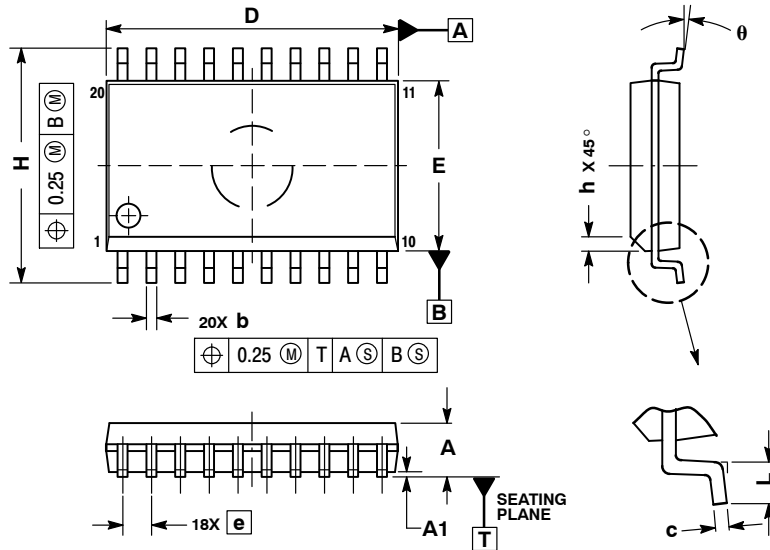
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## PACKAGE DIMENSIONS

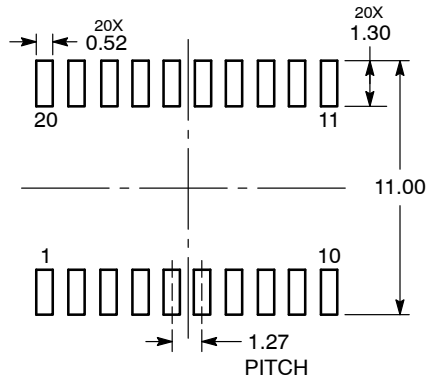
SOIC-20 WB  
DW SUFFIX  
CASE 751D-05  
ISSUE H



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM   | MILLIMETERS |       |
|-------|-------------|-------|
|       | MIN         | MAX   |
| A     | 2.35        | 2.65  |
| A1    | 0.10        | 0.25  |
| b     | 0.35        | 0.49  |
| c     | 0.23        | 0.32  |
| D     | 12.65       | 12.95 |
| E     | 7.40        | 7.60  |
| e     | 1.27 BSC    |       |
| H     | 10.05       | 10.55 |
| h     | 0.25        | 0.75  |
| L     | 0.50        | 0.90  |
| theta | 0°          | 7°    |


### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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