



# Single LVDS/Anything-to-LVPECL Translator

MAX9375

## General Description

The MAX9375 is a fully differential, high-speed, anything-to-LVPECL translator designed for signal rates up to 2GHz. The MAX9375's extremely low propagation delay and high speed make it ideal for various high-speed network routing and backplane applications.

The MAX9375 accepts any differential input signal within the supply rails and with minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. Outputs are LVPECL and have sufficient current to drive 50Ω transmission lines.

The MAX9375 is available in an 8-pin  $\mu$ MAX package and operates from a single +3.3V supply over the -40°C to +85°C temperature range.

## Features

- ◆ Guaranteed 2GHz Switching Frequency
- ◆ Accepts LVDS/LVPECL/Anything Inputs
- ◆ 421ps (typ) Propagation Delays
- ◆ 30ps (max) Pulse Skew
- ◆ 2ps<sub>RMS</sub> (max) Random Jitter
- ◆ Minimum 100mV Differential Input to Guarantee AC Specifications
- ◆ Temperature-Compensated LVPECL Output
- ◆ +3.0V to +3.6V Power-Supply Operating Range
- ◆ >2kV ESD Protection (Human Body Model)

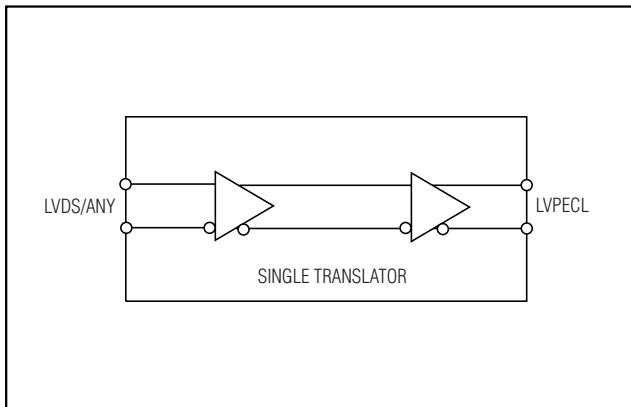
## Applications

Backplane Logic Standard Translation  
 LAN  
 WAN  
 DSLAM  
 DLC

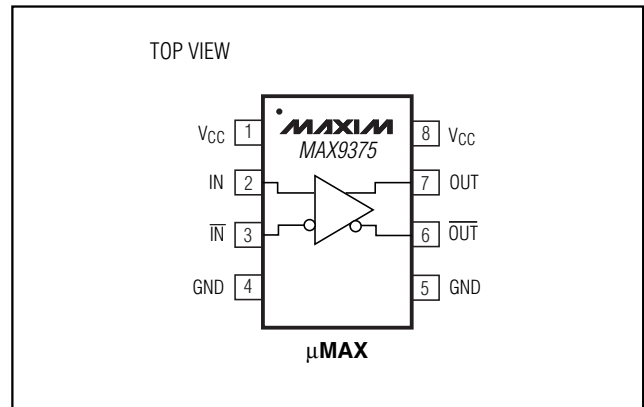
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9375EUA	-40°C to +85°C	8 $\mu$ MAX

## Functional Diagram



## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	-0.3V to +4.1V	Junction Temperature	+150°C
Inputs (IN, $\overline{\text{IN}}$ )	-0.3V to (V <sub>CC</sub> + 0.3V)	Storage Temperature Range	-65°C to +150°C
IN to $\overline{\text{IN}}$	±3.0V	ESD Protection	
Continuous Output Current	50mA	Human Body Model (IN, $\overline{\text{IN}}$ , OUT, $\overline{\text{OUT}}$ )	≥ 2kV
Surge Output Current	100mA	Soldering Temperature (10s)	+300°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)			
8-Pin $\mu$ MAX (derate 5.9mW/°C above +70°C)	470.6mW		
$\theta_{\text{JA}}$ in Still Air	+170°C/W		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, differential input voltage |V<sub>ID1</sub>| = 0.1V to 3.0V, input voltage (V<sub>IN</sub>, V $\overline{\text{IN}}$ ) = 0 to V<sub>CC</sub>, input common-mode voltage V<sub>CM</sub> = 0.05V to (V<sub>CC</sub> - 0.05V), LVPECL outputs terminated with 50 $\Omega$  ±1% to V<sub>CC</sub> - 2.0V, T<sub>A</sub> = -40°C to +85°C. Typical values are at V<sub>CC</sub> = +3.3V, |V<sub>ID1</sub>| = 0.2V, input common-mode voltage V<sub>CM</sub> = 1.2V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>DIFFERENTIAL INPUTS (IN, <math>\overline{\text{IN}}</math>)</b>												
Differential Input Threshold	V <sub>THD</sub>		-100		+100	-100		+100	-100		+100	mV
Input Current	I <sub>IN</sub> , I $\overline{\text{IN}}$	V <sub>IN</sub> , V $\overline{\text{IN}}$ = V <sub>CC</sub> or 0V	-20		+20	-20		+20	-20		+20	$\mu$ A
Input Common-Mode Voltage	V <sub>CM</sub>	Figure 1	0.05		V <sub>CC</sub> - 0.05	0.05		V <sub>CC</sub> - 0.05	0.05		V <sub>CC</sub> - 0.05	V
<b>LVPECL OUTPUTS (OUT, <math>\overline{\text{OUT}}</math>)</b>												
Single-Ended Output High Voltage	V <sub>OH</sub>		V <sub>CC</sub> - 1.085	V <sub>CC</sub> - 1.017	V <sub>CC</sub> - 0.880	V <sub>CC</sub> - 1.025	V <sub>CC</sub> - 0.983	V <sub>CC</sub> - 0.880	V <sub>CC</sub> - 1.025	V <sub>CC</sub> - 0.966	V <sub>CC</sub> - 0.880	V
Single-Ended Output Low Voltage	V <sub>OL</sub>		V <sub>CC</sub> - 1.830	V <sub>CC</sub> - 1.753	V <sub>CC</sub> - 1.620	V <sub>CC</sub> - 1.810	V <sub>CC</sub> - 1.710	V <sub>CC</sub> - 1.620	V <sub>CC</sub> - 1.810	V <sub>CC</sub> - 1.692	V <sub>CC</sub> - 1.620	V
Differential Output Voltage	V <sub>OH</sub> - V <sub>OL</sub>		595	725		595	725		595	725		mV
<b>POWER SUPPLY</b>												
Supply Current	I <sub>CC</sub>	All pins open except V <sub>CC</sub> , GND	10	18		12	18		14	18		mA

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## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ , differential input voltage  $|V_{ID}| = 0.1V$  to  $1.2V$ , input frequency  $\leq 1.34GHz$ , differential input transition time =  $125ps$  (20% to 80%), input voltage ( $V_{IN}, \overline{V_{IN}}$ ) =  $0$  to  $V_{CC}$ , input common-mode voltage  $V_{CM} = 0.05V$  to  $(V_{CC} - 0.05V)$ , outputs terminated with  $50\Omega \pm 1\%$  to  $V_{CC} - 2.0V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{CC} = +3.3V$ ,  $|V_{ID}| = 0.2V$ , input common-mode voltage  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	$f_{MAX}$	$V_{OH} - V_{OL} \geq 250mV$	2.0	2.5		GHz
Propagation Delay Low to High	$t_{PLH}$	Figure 2	250	421	600	ps
Propagation Delay High to Low	$t_{PHL}$	Figure 2	250	421	600	ps
Pulse Skew $ t_{PLH} - t_{PHL} $	$t_{SKEW}$	Figure 2 (Note 5)		6	30	ps
Output Low-to-High Transition Time (20% to 80%)	$t_R$	Figure 2		116	220	ps
Output High-to-Low Transition Time (20% to 80%)	$t_F$	Figure 2		116	220	ps
Added Random Jitter	$t_{RJ}$	$f_{IN} = 1.34GHz$ (Note 6)		0.7	2	ps(RMS)

**Note 1:** Measurements are made with the device in thermal equilibrium. All voltages are referenced to ground except  $V_{THD}$  and  $V_{ID}$ .

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.

**Note 3:** DC parameters production tested at  $T_A = +25^\circ C$  and guaranteed by design and characterization over the full operating temperature range.

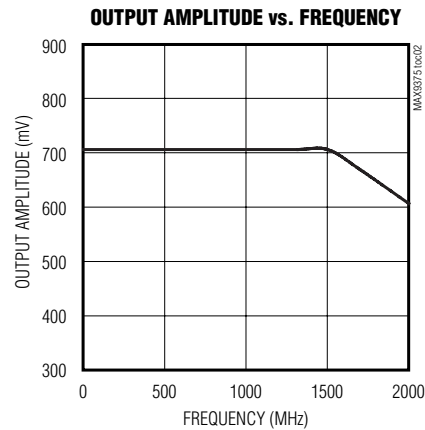
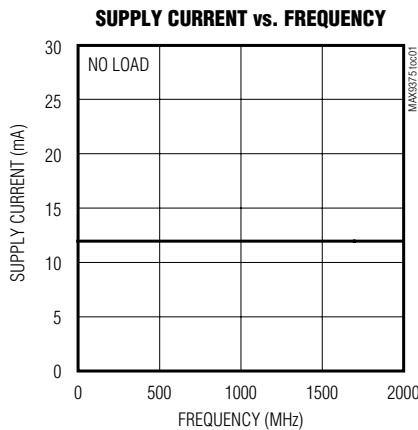
**Note 4:** Guaranteed by design and characterization, not production tested. Limits are set at  $\pm 6$  sigma.

**Note 5:**  $t_{SKEW}$  is the magnitude difference of differential propagation delays for the same output under the same conditions;  $t_{SKEW} = |t_{PHL} - t_{PLH}|$ .

**Note 6:** Device jitter added to the input signal.

## Typical Operating Characteristics

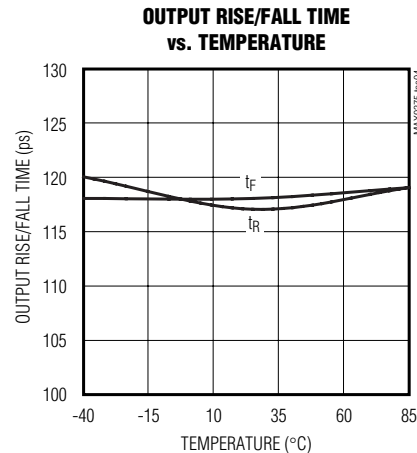
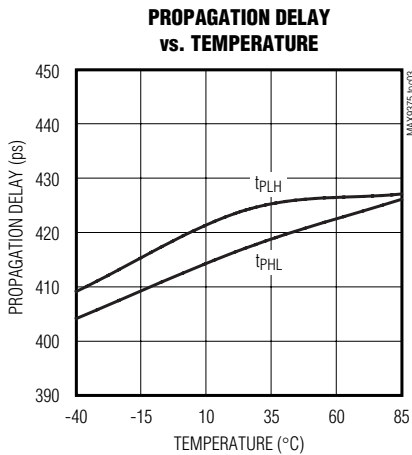
( $V_{CC} = +3.3V$ , differential input voltage  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ , input frequency =  $500MHz$ , outputs terminated with  $50\Omega \pm 1\%$  to  $V_{CC} - 2.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Single LVDS/Anything-to-LVPECL Translator

## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ , differential input voltage  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ , input frequency = 500MHz, outputs terminated with  $50\Omega \pm 1\%$  to  $V_{CC} - 2.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Detailed Description

The MAX9375 is a fully differential, high-speed, anything-to-LVPECL translator designed for signal rates up to 2GHz. The MAX9375's extremely low propagation delay and high speed make it ideal for various high-speed network routing and backplane applications.

The MAX9375 accepts any differential input signals within the supply rails and with a minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. Outputs are LVPECL and have sufficient current to drive  $50\Omega$  transmission lines.

### Inputs

Inputs have a wide common-mode range of 0.05V to ( $V_{CC} - 0.05V$ ), which accommodates any differential signals within rails, and requires a minimum of 100mV to switch the outputs. This allows the MAX9375 inputs to support virtually any differential signaling standard.

### LVPECL Outputs

The MAX9375 outputs are emitter followers that require external resistive paths to a voltage source ( $V_T = V_{CC} - 2.0V$  typ) more negative than worst-case  $V_{OL}$  for proper

## Pin Description

PIN	NAME	FUNCTION
1, 8	$V_{CC}$	Positive Supply. Bypass from $V_{CC}$ to GND with 0.1 $\mu F$ and 0.01 $\mu F$ ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	IN	LVDS/Anything Noninverting Input
3	$\overline{IN}$	LVDS/Anything Inverting Input
4, 5	GND	Power Supply Ground Connection
6	$\overline{OUT}$	Differential LVPECL Inverting Output. Terminate with $50\Omega \pm 1\%$ to $V_{CC} - 2V$ .
7	OUT	Differential LVPECL Noninverting Output. Terminate with $50\Omega \pm 1\%$ to $V_{CC} - 2V$ .

static and dynamic operation. When properly terminated, the outputs generate steady-state voltage levels,  $V_{OL}$  or  $V_{OH}$  with fast transition edges between state levels. Output current always flows into the termination during proper operation.

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## Applications Information

### Output Termination

Terminate the outputs with  $50\Omega$  to  $(V_{CC} - 2V)$  or use equivalent Thevenin terminations. Terminate  $\overline{\text{OUT}}$  and  $\text{OUT}$  with identical termination on each for low-output distortion. When a single-ended signal is taken from the differential output, terminate both  $\text{OUT}$  and  $\overline{\text{OUT}}$ . Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

### Supply Bypassing

Bypass  $V_{CC}$  to ground with high-frequency surface-mount ceramic  $0.1\mu\text{F}$  and  $0.01\mu\text{F}$  capacitors. Place the capacitors as close to the device as possible with the  $0.01\mu\text{F}$  capacitor closest to the device pins.

### Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the  $50\Omega$  characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

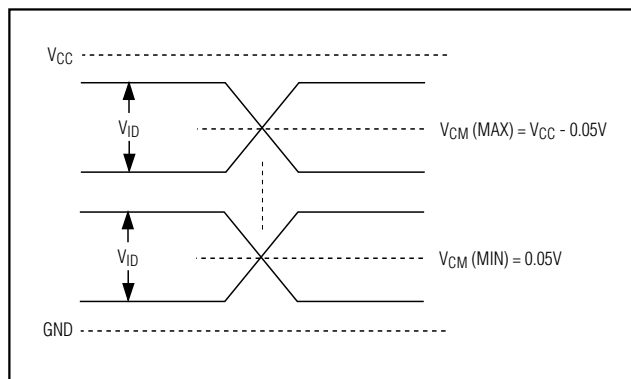


Figure 1. Input Definitions

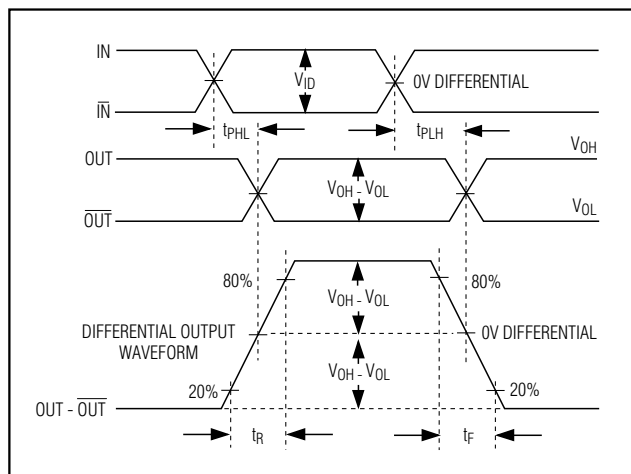


Figure 2. Differential Input-to-Output Propagation Delay Timing Diagram

## Chip Information

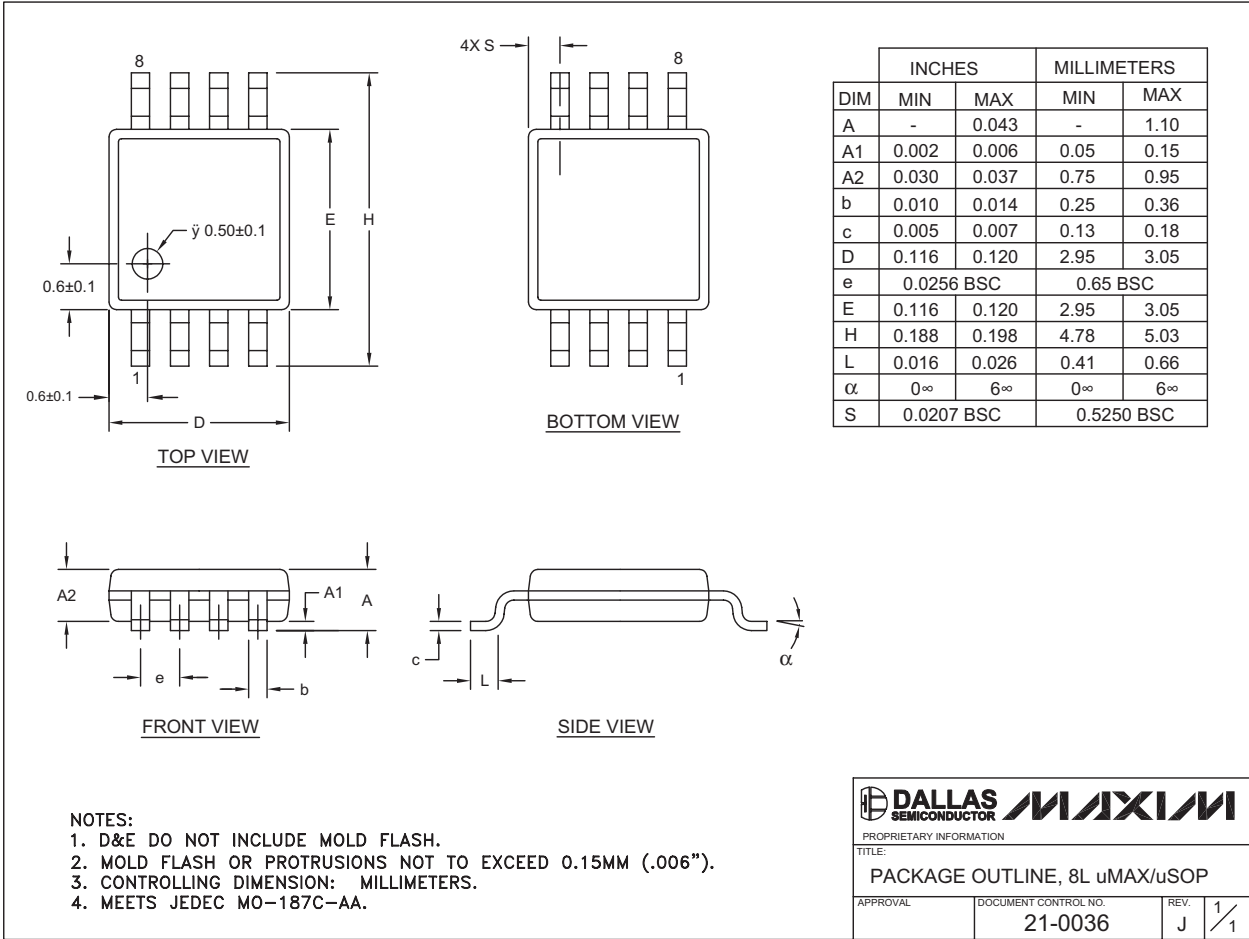
TRANSISTOR COUNT: 614

PROCESS: Bipolar

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## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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