MAX8557ETE
Rev. A

RELIABILITY REPORT

FOR

MAX8557ETE

PLASTIC ENCAPSULATED DEVICES

July 19, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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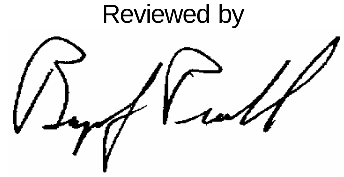
Reviewed by



Bryan J. Preeshl
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Conclusion

The MAX8557 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX8557 low-dropout linear regulator operates from input voltages as low as 1.425V and is able to deliver up to 4A of continuous output current with a typical dropout voltage of only 100mV. The output voltage is adjustable from 0.5V to V_{IN} - 0.2V.

Designed with an internal p-channel MOSFET pass transistor, the MAX8557 maintains a low 800µA typical supply current, independent of the load current and dropout voltage. Using a p-channel MOSFET eliminates the need for an additional external supply or a noisy internal charge pump. Other features include a logic-controlled shutdown mode, built-in soft-start, short-circuit protection with foldback current limit, and thermal-overload protection. The MAX8557 offers a power-on reset output that transitions high 140ms after the output has achieved 90% of its nominal output voltage.

The MAX8557 is available in a 16-pin thin QFN 5mm x 5mm package with exposed paddle.

B. Absolute Maximum Ratings

Item	Rating
IN, EN, POK, POR to GND	-0.3V to +4V
FB, OUT to GND	-0.3V to (VIN + 0.3V)
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin Thin QFN (5mm x 5mm)	2666.7mW
Derates above +70°C (Note 1)	
16-Pin Thin QFN (5mm x 5mm)	33.3mW/°C

Note 1: Maximum power dissipation is obtained using JEDEC JESD51-5 and JESD51-7 standards.

II. Manufacturing Information

A. Description/Function: 4A Ultra-Low-Input-Voltage LDO Regulators

B. Process: S4

C. Number of Device Transistors: 3137

D. Fabrication Location: California, USA

E. Assembly Location: Thailand, Hong Kong or Thailand

F. Date of Initial Production: April, 2004

III. Packaging Information

A. Package Type: **16-Pin QFN (5x5)**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Conductive Epoxy

E. Bondwire: Gold (2.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-9000-0801

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A: Level 1

IV. Die Information

A. Dimensions: 110 x 90 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)

F. Minimum Metal Spacing: Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 14.28 \times 10^{-9}$

λ = 14.28 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6240) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PN29 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX8557ETE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		77	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

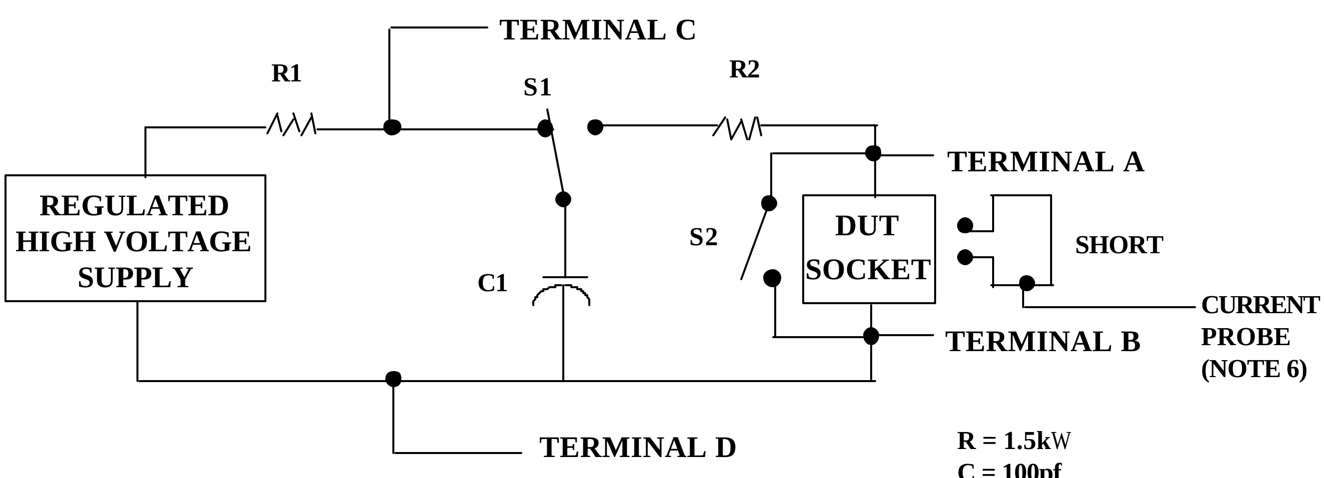
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

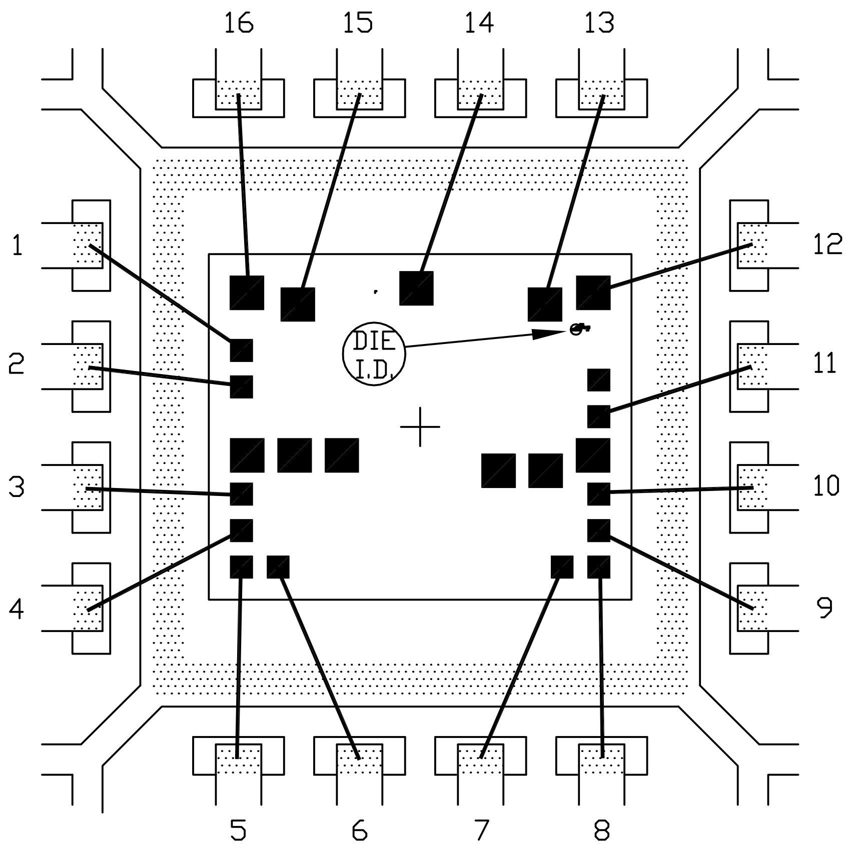
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



5x5x0.8mm THIN QFN PKG.

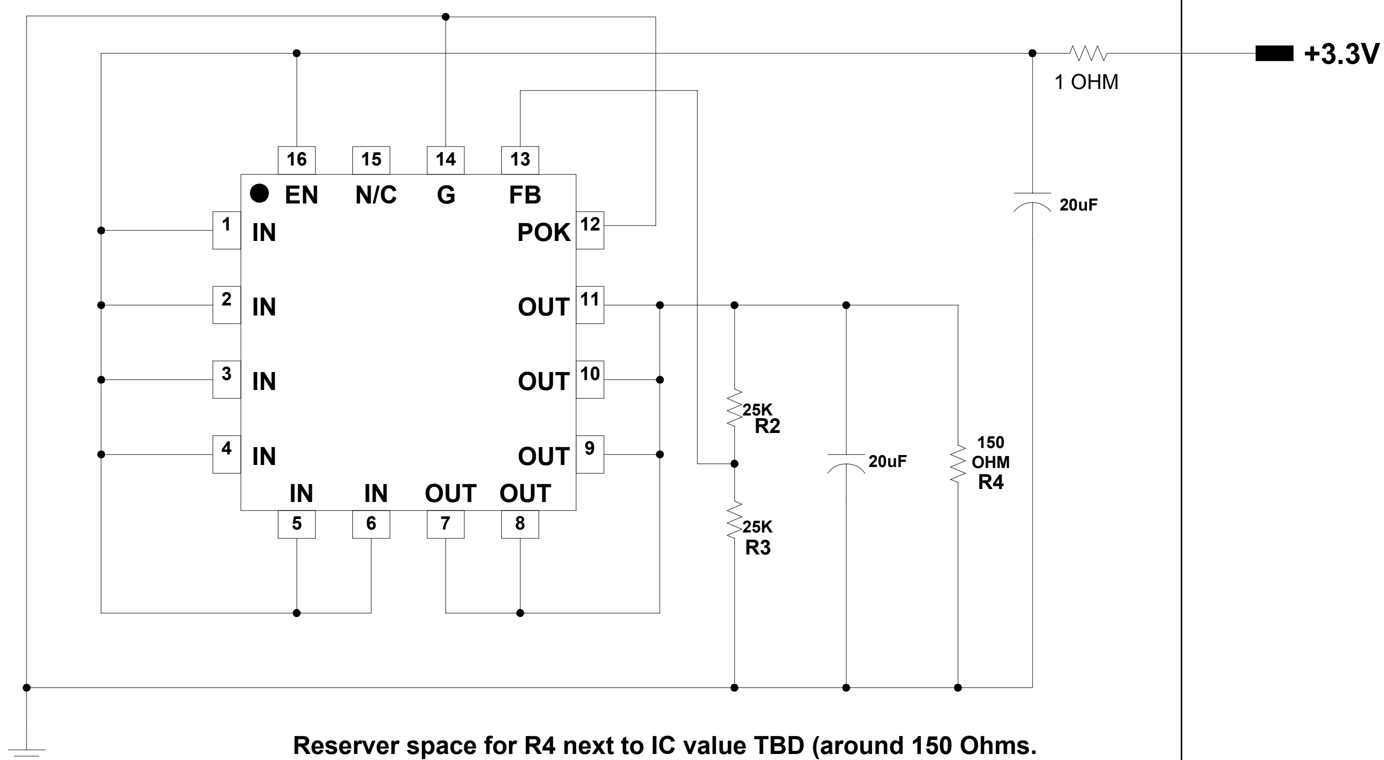
EXPOSED PAD PKG.



BONDABLE AREA

PKG. CODE: T1655-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 146x146	PKG.			BOND DIAGRAM #: 05-9000-0801	REV: C
	DESIGN				

ONCE PER SOCKET **ONCE PER BOARD**



Reserver space for R4 next to IC value TBD (around 150 Ohms.
Both input and output caps are ceramic and close to chip.
3.3V in and 135 degree ambient temp. Junction temp is 150 degrees.
TQFN = 47 degree/W. Power dissipation < 0.31W.

DEVICES: MAX 8556/7 (PN29Z) PACKAGE: 16-QFN (5x5) THIN MAX. EXPECTED CURRENT = 20mA	NOTES: Ave. expected current = 8mA