



# Dual Universal Switched-Capacitor Filters

MAX7490/MAX7491

## General Description

The MAX7490/MAX7491 consist of two identical low-power, low-voltage, wide dynamic range, Rail-to-Rail<sup>®</sup>, 2nd-order switched-capacitor building blocks. Each of the two filter sections, together with two to four external resistors, can generate all standard 2nd-order functions: bandpass, lowpass, highpass, and notch (band reject). Three of these functions are simultaneously available. Fourth-order filters can be obtained by cascading the two 2nd-order filter sections. Similarly, higher order filters can easily be created by cascading multiple MAX7490/MAX7491s.

Two clocking options are available: self-clocking (through the use of an external capacitor) or external clocking for tighter cutoff frequency control. The clock-to-center frequency ratio is 100:1. Sampling is done at twice the clock frequency, further separating the cutoff frequency and Nyquist frequency.

The MAX7490/MAX7491 have an internal rail splitter that establishes a precise common voltage needed for single-supply operation. The MAX7490 operates from a single +5V supply and the MAX7491 operates from a single +3V supply. Both devices feature a low-power shutdown mode and come in a 16-pin QSOP package.

## Applications

Tunable Active Filters  
 Multipole Filters  
 ADC Anti-Aliasing  
 Post-DAC Filtering  
 Adaptive Filtering  
 Phase-Locked Loops (PLLs)  
 Set-Top Boxes

*Typical Application Circuit appears at end of data sheet.*

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

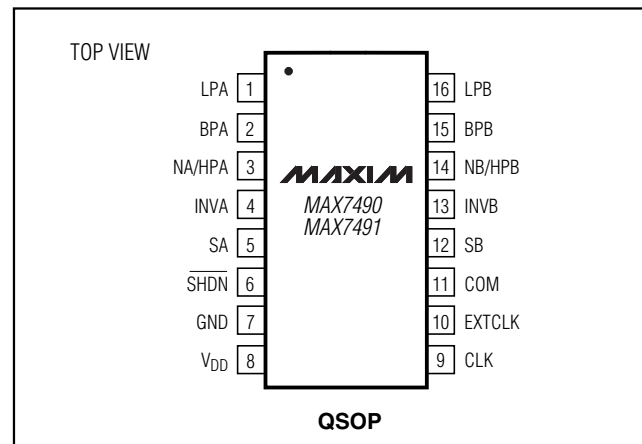
## Features

- ◆ Dual 2nd-Order Filter in a 16-Pin QSOP Package
- ◆ High Accuracy
  - Q Accuracy:  $\pm 0.2\%$
  - Clock-to-Center Frequency Error:  $\pm 0.2\%$
- ◆ Rail-to-Rail Input and Output Operation
- ◆ Single-Supply Operation: +5V (MAX7490) or +3V (MAX7491)
- ◆ Internal or External Clock
- ◆ Highpass, Lowpass, Bandpass, and Notch Filters
- ◆ Clock-to-Center Frequency Ratio of 100:1
- ◆ Internal Sampling-to-Center Frequency Ratio of 200:1
- ◆ Center Frequency up to 40kHz
- ◆ Easily Cascaded for Multipole Filters
- ◆ Low-Power Shutdown:  $< 1\mu\text{A}$  Supply Current

## Ordering Information

| PART       | TEMP. RANGE    | PIN-PACKAGE | SUPPLY VOLTAGE (+V) |
|------------|----------------|-------------|---------------------|
| MAX7490CEE | 0°C to +70°C   | 16 QSOP     | 5                   |
| MAX7490EEE | -40°C to +85°C | 16 QSOP     | 5                   |
| MAX7491CEE | 0°C to +70°C   | 16 QSOP     | 3                   |
| MAX7491EEE | -40°C to +85°C | 16 QSOP     | 3                   |

## Pin Configuration



# Dual Universal Switched-Capacitor Filters

## ABSOLUTE MAXIMUM RATINGS

|   |                                   |
|---|-----------------------------------|
| V <sub>DD</sub> to GND                                | -0.3V to +6V                      |
| EXTCLK, $\overline{\text{SHDN}}$ to GND               | -0.3V to +6V                      |
| INV_, LP_, BP_, N_/HP_, S_, COM,<br>CLK to GND        | -0.3V to (V <sub>DD</sub> + 0.3V) |
| Maximum Current into Any Pin                          | 50mA                              |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                                   |
| 16-Pin QSOP (derate 8.30mW/°C above +70°C)            | 667mW                             |

|                                   |                 |
|-----------------------------------|-----------------|
| Operating Temperature Range       |                 |
| MAX749_CEE                        | 0°C to +70°C    |
| MAX749_EEE                        | -40°C to +85°C  |
| Die Temperature                   | +150°C          |
| Storage Temperature               | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—MAX7490

(V<sub>DD</sub> = EXTCLK = +5V, f<sub>CLK</sub> = 625kHz, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, 10k $\Omega$  || 50pF load to V<sub>DD</sub>/2 at LP\_, BP\_, and N\_/HP\_,  $\overline{\text{SHDN}}$  = V<sub>DD</sub>, 0.1 $\mu$ F from COM to GND, 50% duty-cycle clock input, COM = V<sub>DD</sub>/2. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER                              | SYMBOL                           | CONDITIONS   | MIN                      | TYP                | MAX                      | UNITS                  |
|--|----------------------------------|--|--------------------------|--------------------|--------------------------|------------------------|
| <b>FILTER</b>                          |                                  |  |                          |                    |                          |                        |
| Center Frequency Range                 | f <sub>O</sub>                   | Mode 1   |                          | 0.001 to 40        |                          | kHz                    |
| Clock-to-Center Frequency Accuracy     | f <sub>CLK</sub> /f <sub>O</sub> | Mode 1, R1 = R3 = 50k $\Omega$ , R2 = 10k $\Omega$ , Q = 5, deviation from 100:1 |                          | ±0.2               | ±0.7                     | %                      |
| Q Accuracy                             |                                  | Mode 1, R1 = R3 = 50k $\Omega$ , R2 = 10k $\Omega$ , Q = 5                       |                          | ±0.2               | ±2                       | %                      |
| f <sub>O</sub> Temperature Coefficient |                                  |  |                          | ±1                 |                          | ppm/°C                 |
| Q Temperature Coefficient              |                                  |  |                          | ±5                 |                          | ppm/°C                 |
| DC Lowpass Gain Accuracy               |                                  | Mode 1, R1 = R2 = 10k $\Omega$   |                          | ±0.1               | ±0.5                     | %                      |
| DC Offset Voltage (Figure 8)           | V <sub>OS1</sub>                 | DC offset of input inverter  |                          | ±3                 | ±12.5                    | mV                     |
|  | V <sub>OS2</sub>                 | DC offset of 1st integrator  |                          | ±4                 | ±15                      |                        |
|  | V <sub>OS3</sub>                 | DC offset of 2nd integrator  |                          | ±4                 | ±30                      |                        |
| Crosstalk (Note 2)                     |                                  | f <sub>IN</sub> = 10kHz  |                          | -60                |                          | dB                     |
| COM Voltage Range                      | V <sub>COM</sub>                 | Input: COM externally driven   | V <sub>DD</sub> /2 - 0.5 | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 + 0.5 | V                      |
|  |                                  | Output: COM internally driven  | V <sub>DD</sub> /2 - 0.2 | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 + 0.2 |                        |
| Input Resistance at COM                | R <sub>COM</sub>                 |  | 140                      | 250                | 325                      | k $\Omega$             |
| Clock Feedthrough                      |                                  | Up to 5th harmonic of f <sub>CLK</sub>   |                          | 200                |                          | $\mu$ V <sub>RMS</sub> |
| Noise (Note 3)                         |                                  | Mode 1, R1 = R2 = R3 = 10k $\Omega$ , LP output, Q = 1                           |                          | 60                 |                          | $\mu$ V <sub>RMS</sub> |
| Output Voltage Swing                   |                                  |  | 0.2                      |                    | V <sub>DD</sub> - 0.2    | V                      |
| Input Leakage Current at COM           |                                  | $\overline{\text{SHDN}}$ = GND, V <sub>COM</sub> = 0 to V <sub>DD</sub>          |                          | ±0.1               | ±10                      | $\mu$ A                |
| <b>CLOCK</b>                           |                                  |  |                          |                    |                          |                        |
| Maximum Clock Frequency                | f <sub>CLK</sub>                 |  |                          | 4                  |                          | MHz                    |
| Internal Oscillator Frequency (Note 4) | f <sub>OSC</sub>                 | EXTCLK = GND, C <sub>OSC</sub> = 1000pF  | 95                       | 135                | 175                      | kHz                    |
|  |                                  | EXTCLK = GND, C <sub>OSC</sub> = 100pF   |                          | 1.35               |                          | MHz                    |
| Clock Input High                       |                                  |  | V <sub>DD</sub> - 0.5    |                    |                          | V                      |

# Dual Universal Switched-Capacitor Filters

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## ELECTRICAL CHARACTERISTICS—MAX7490 (continued)

( $V_{DD} = EXTCLK = +5V$ ,  $f_{CLK} = 625kHz$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $10k\Omega$  ||  $50pF$  load to  $V_{DD}/2$  at  $LP_-$ ,  $BP_-$ , and  $N_/HP_-$ ,  $\overline{SHDN} = V_{DD}$ ,  $0.1\mu F$  from  $COM$  to  $GND$ , 50% duty-cycle clock input,  $COM = V_{DD}/2$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 1)

| PARAMETER                               | SYMBOL     | CONDITIONS   | MIN            | TYP        | MAX      | UNITS      |
|---|------------|--|----------------|------------|----------|------------|
| Clock Input Low                         |            |  |                |            | 0.5      | V          |
| Clock Duty Cycle                        |            |  |                | $50 \pm 5$ |          | %          |
| <b>SHDN AND EXTCLK</b>                  |            |  |                |            |          |            |
| Input High                              | $V_{IH}$   |  | $V_{DD} - 0.5$ |            |          | V          |
| Input Low                               | $V_{IL}$   |  |                |            | 0.5      | V          |
| Input Leakage Current                   |            | $V_{INPUT} = 0$ to $V_{DD}$  |                | $\pm 0.4$  | $\pm 10$ | $\mu A$    |
| <b>POWER REQUIREMENTS</b>               |            |  |                |            |          |            |
| Supply Voltage                          | $V_{DD}$   |  | 4.5            |            | 5.5      | V          |
| Power-Supply Current                    | $I_{DD}$   | No external load, mode 1, $R_1 = R_3 = 50k\Omega$ ,<br>$R_2 = 10k\Omega$ , $Q = 5$ |                | 3.5        | 4.0      | mA         |
| Shutdown Current                        | $I_{SHDN}$ | $\overline{SHDN} = GND$  |                |            | 1        | $\mu A$    |
| <b>INTERNAL OP AMPS CHARACTERISTICS</b> |            |  |                |            |          |            |
| Output Short-Circuit Current            |            |  |                | $\pm 18$   |          | mA         |
| DC Open-Loop Gain                       |            | $R_L \geq 10k\Omega$ , $C_L \leq 50pF$   |                | 130        |          | dB         |
| Gain Bandwidth Product                  | GBW        | $R_L \geq 10k\Omega$ , $C_L \leq 50pF$   |                | 7          |          | MHz        |
| Slew Rate                               | SR         | $R_L \geq 10k\Omega$ , $C_L \leq 50pF$   |                | 6.4        |          | V/ $\mu s$ |

# Dual Universal Switched-Capacitor Filters

## ELECTRICAL CHARACTERISTICS—MAX7491

( $V_{DD} = \text{EXTCLK} = +3V$ ,  $f_{CLK} = 625\text{kHz}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $10\text{k}\Omega$  ||  $50\text{pF}$  load to  $V_{DD}/2$  at  $LP_{-}$ ,  $BP_{-}$ , and  $N_{-}/HP_{-}$ ,  $\overline{\text{SHDN}} = V_{DD}$ ,  $0.1\mu\text{F}$  from COM to GND, 50% duty-cycle clock input, COM =  $V_{DD}/2$ . Typical values are at  $T_A = +25^{\circ}\text{C}$ , unless otherwise noted.) (Note 1)

| PARAMETER                              | SYMBOL        | CONDITIONS   | MIN              | TYP         | MAX              | UNITS                   |
|--|---------------|--|------------------|-------------|------------------|-------------------------|
| <b>FILTER</b>                          |               |  |                  |             |                  |                         |
| Center Frequency Range                 | $f_0$         | Mode 1   |                  | 0.001 to 40 |                  | kHz                     |
| Clock-to-Center Frequency Accuracy     | $f_{CLK}/f_0$ | Mode 1, $R_1 = R_3 = 50\text{k}\Omega$ , $R_2 = 10\text{k}\Omega$ , $Q = 5$ , deviation from 100:1 |                  | $\pm 0.2$   | $\pm 0.7$        | %                       |
| Q Accuracy                             |               | Mode 1, $R_1 = R_3 = 50\text{k}\Omega$ , $R_2 = 10\text{k}\Omega$ , $Q = 5$                        |                  | $\pm 0.2$   | $\pm 2$          | %                       |
| $f_0$ Temperature Coefficient          |               |  |                  | $\pm 1$     |                  | ppm/ $^{\circ}\text{C}$ |
| Q Temperature Coefficient              |               |  |                  | $\pm 5$     |                  | ppm/ $^{\circ}\text{C}$ |
| DC Lowpass Gain Accuracy               |               | Mode 1, $R_1 = R_2 = 10\text{k}\Omega$   |                  | $\pm 0.1$   | $\pm 0.5$        | %                       |
| DC Offset Voltage (Figure 8)           | $V_{OS1}$     | DC offset of input inverter  |                  | $\pm 3$     | $\pm 12.5$       | mV                      |
|  | $V_{OS2}$     | DC offset of 1st integrator  |                  | $\pm 4$     | $\pm 15$         |                         |
|  | $V_{OS3}$     | DC offset of 2nd integrator  |                  | $\pm 4$     | $\pm 25$         |                         |
| Crosstalk (Note 2)                     |               | $f_{IN} = 10\text{kHz}$  |                  | -60         |                  | dB                      |
| COM Voltage Range                      | $V_{COM}$     | Input: COM externally driven   | $V_{DD}/2 - 0.1$ | $V_{DD}/2$  | $V_{DD}/2 + 0.1$ | V                       |
|  |               | Output: COM internally driven  | $V_{DD}/2 - 0.1$ | $V_{DD}/2$  | $V_{DD}/2 + 0.1$ |                         |
| Input Resistance at COM                | $R_{COM}$     |  | 60               | 80          | 120              | $\text{k}\Omega$        |
| Clock Feedthrough                      |               | Up to 5th harmonic of $f_{CLK}$  |                  | 200         |                  | $\mu\text{VRMS}$        |
| Noise (Note 3)                         |               | Mode 1, $R_1 = R_2 = R_3 = 10\text{k}\Omega$ , LP output, $Q = 1$                                  |                  | 60          |                  | $\mu\text{VRMS}$        |
| Output Voltage Swing                   |               |  | 0.2              |             | $V_{DD} - 0.2$   | V                       |
| Input Leakage Current at COM           |               | $\overline{\text{SHDN}} = \text{GND}$ , $V_{COM} = 0$ to $V_{DD}$                                  |                  | $\pm 0.1$   | $\pm 10$         | $\mu\text{A}$           |
| <b>CLOCK</b>                           |               |  |                  |             |                  |                         |
| Maximum Clock Frequency                | $f_{CLK}$     |  |                  | 4           |                  | MHz                     |
| Internal Oscillator Frequency (Note 4) | $f_{OSC}$     | EXTCLK = GND, $C_{OSC} = 1000\text{pF}$  | 95               | 135         | 175              | kHz                     |
|  |               | EXTCLK = GND, $C_{OSC} = 100\text{pF}$   |                  | 1.35        |                  | MHz                     |
| Clock Input High                       |               |  | $V_{DD} - 0.5$   |             |                  | V                       |
| Clock Input Low                        |               |  |                  |             | 0.5              | V                       |
| Clock Duty Cycle                       |               |  |                  | $50 \pm 5$  |                  | %                       |
| <b>SHDN AND EXTCLK</b>                 |               |  |                  |             |                  |                         |
| Input High                             | $V_{IH}$      |  | $V_{DD} - 0.5$   |             |                  | V                       |
| Input Low                              | $V_{IL}$      |  |                  |             | 0.5              | V                       |
| Input Leakage Current                  |               | $V_{INPUT} = 0$ to $V_{DD}$  |                  | $\pm 0.4$   | $\pm 10$         | $\mu\text{A}$           |

# Dual Universal Switched-Capacitor Filters

MAX7490/MAX7491

## ELECTRICAL CHARACTERISTICS—MAX7491 (continued)

( $V_{DD} = \text{EXTCLK} = +3\text{V}$ ,  $f_{\text{CLK}} = 625\text{kHz}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ ,  $10\text{k}\Omega \parallel 50\text{pF}$  load to  $V_{DD}/2$  at  $\text{LP}_-$ ,  $\text{BP}_-$ , and  $\text{N}_-/ \text{HP}_-$ ,  $\overline{\text{SHDN}} = V_{DD}$ ,  $0.1\mu\text{F}$  from COM to GND, 50% duty-cycle clock input, COM =  $V_{DD}/2$ . Typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (Note 1)

| PARAMETER                               | SYMBOL            | CONDITIONS  | MIN | TYP      | MAX | UNITS            |
|---|-------------------|---|-----|----------|-----|------------------|
| <b>POWER REQUIREMENTS</b>               |                   |   |     |          |     |                  |
| Supply Voltage                          | $V_{DD}$          |   | 2.7 |          | 3.6 | V                |
| Power-Supply Current                    | $I_{DD}$          | No load, mode 1, $R_1 = R_3 = 50\text{k}\Omega$ ,<br>$R_2 = 10\text{k}\Omega$ , $Q = 5$ |     | 3.5      | 4.0 | mA               |
| Shutdown Current                        | $I_{\text{SHDN}}$ | $\overline{\text{SHDN}} = \text{GND}$   |     |          | 1   | $\mu\text{A}$    |
| <b>INTERNAL OP AMPS CHARACTERISTICS</b> |                   |   |     |          |     |                  |
| Output Short-Circuit Current            |                   |   |     | $\pm 11$ |     | mA               |
| DC Open-Loop Gain                       |                   | $R_L \geq 10\text{k}\Omega$ , $C_L \leq 50\text{pF}$                                    |     | 130      |     | dB               |
| Gain Bandwidth Product                  | GBW               | $R_L \geq 10\text{k}\Omega$ , $C_L \leq 50\text{pF}$                                    |     | 7        |     | MHz              |
| Slew Rate                               | SR                | $R_L \geq 10\text{k}\Omega$ , $C_L \leq 50\text{pF}$                                    |     | 6        |     | V/ $\mu\text{s}$ |

**Note 1:** Resistive loading of the  $\text{N}_-/ \text{HP}_-$ ,  $\text{LP}_-$ ,  $\text{BP}_-$  outputs includes the resistors used for the filter implementation.

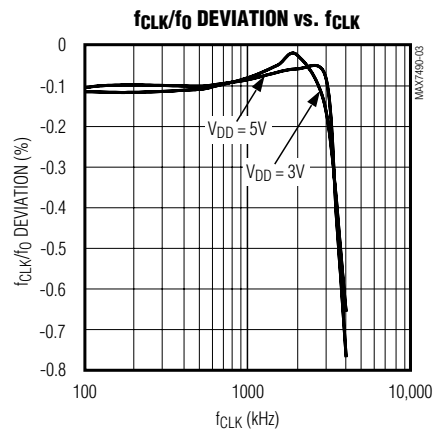
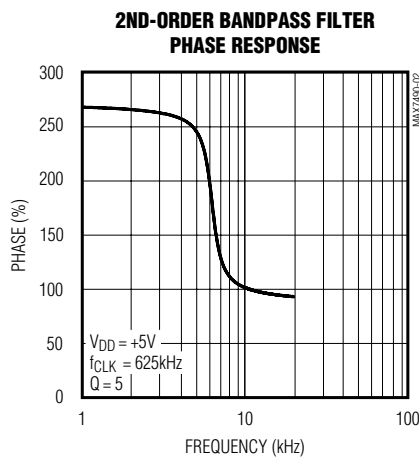
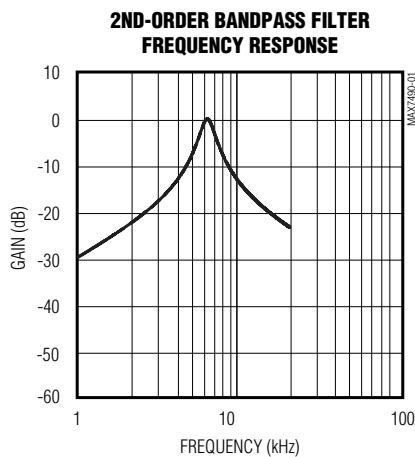
**Note 2:** Crosstalk between internal filter sections is measured by applying a  $1V_{\text{RMS}}$  10kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the  $1V_{\text{RMS}}$  input signal of the other section.

**Note 3:** Bandwidth of noise measurement is 80kHz.

**Note 4:**  $f_{\text{OSC}} (\text{kHz}) = 135 \times 10^3 / C_{\text{OSC}}$  ( $C_{\text{OSC}}$  in pF)

## Typical Operating Characteristics

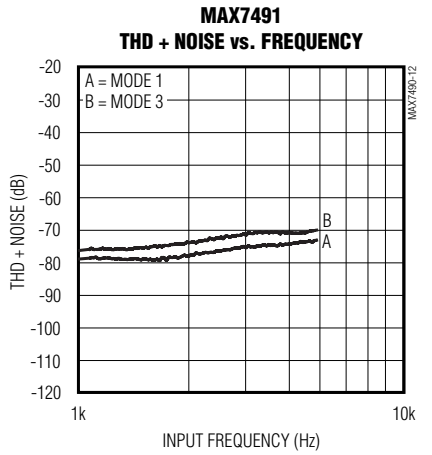
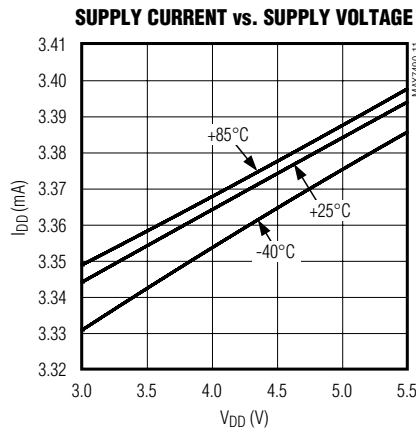
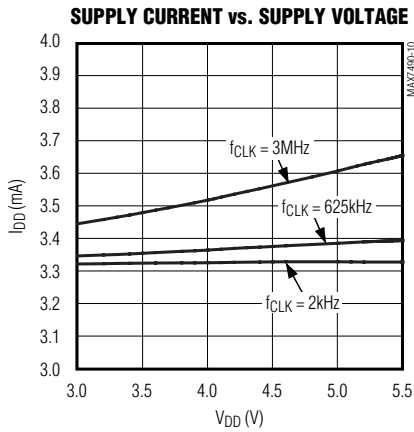
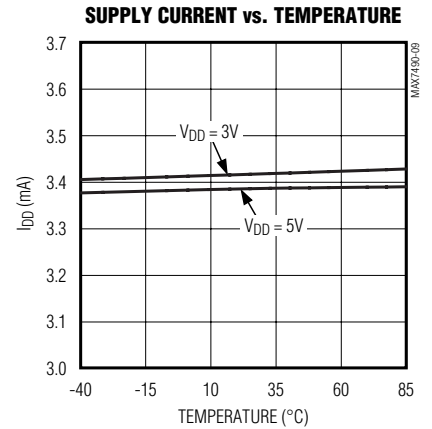
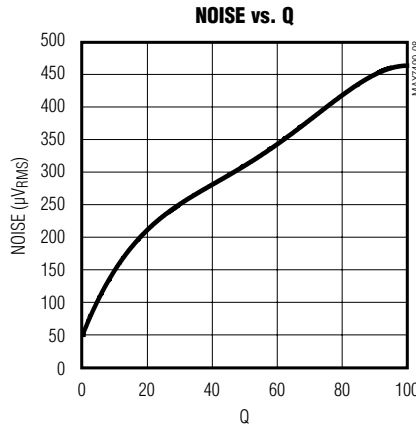
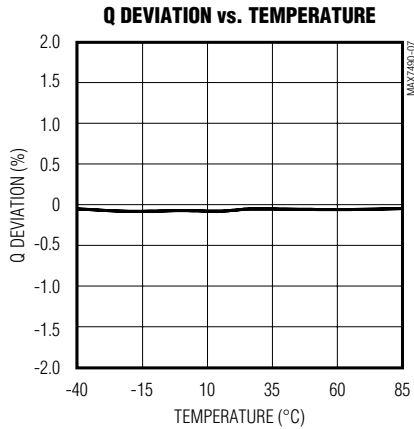
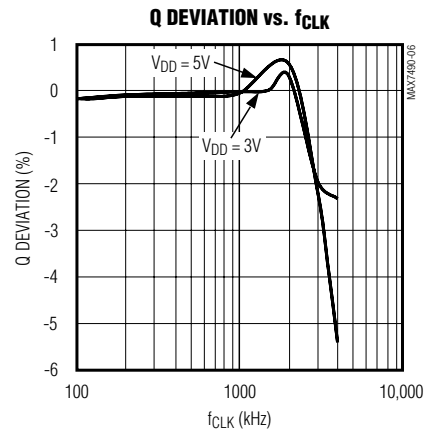
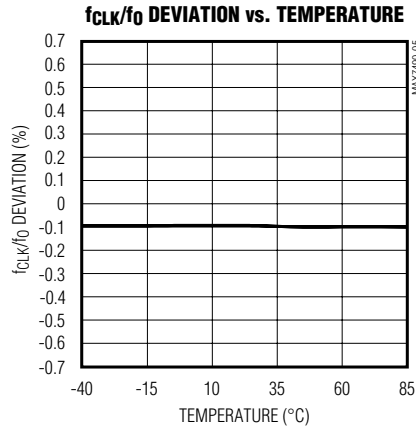
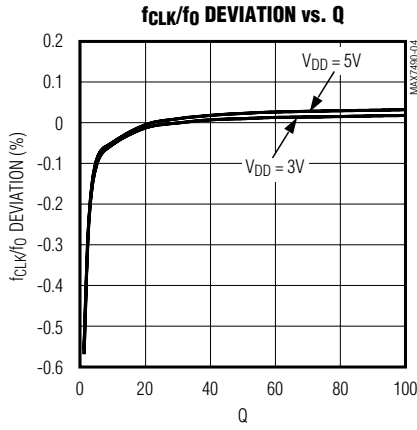
( $V_{DD} = +5\text{V}$  for MAX7490,  $V_{DD} = +3\text{V}$  for MAX7491,  $f_{\text{CLK}} = 625\text{kHz}$ ,  $\overline{\text{SHDN}} = \text{EXTCLK} = V_{DD}$ , COM =  $V_{DD}/2$ , Mode 1,  $R_3 = R_1 = 50\text{k}\Omega$ ,  $R_2 = 10\text{k}\Omega$ ,  $Q = 5$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Dual Universal Switched-Capacitor Filters

## Typical Operating Characteristics (continued)

( $V_{DD} = +5V$  for MAX7490,  $V_{DD} = +3V$  for MAX7491,  $f_{CLK} = 625kHz$ ,  $\overline{SHDN} = EXTCLK = V_{DD}$ ,  $COM = V_{DD}/2$ , Mode 1,  $R3 = R1 = 50k\Omega$ ,  $R2 = 10k\Omega$ ,  $Q = 5$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

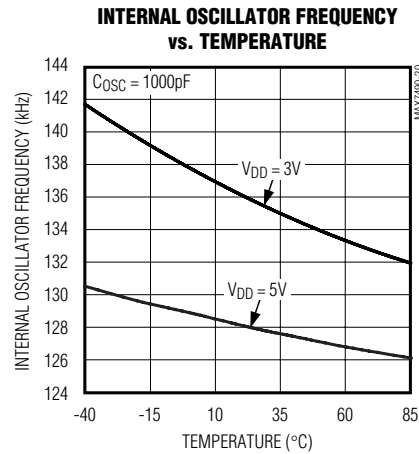
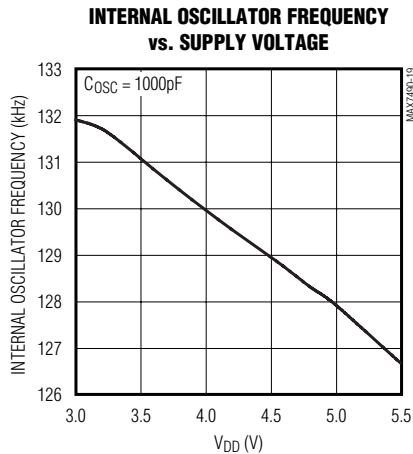
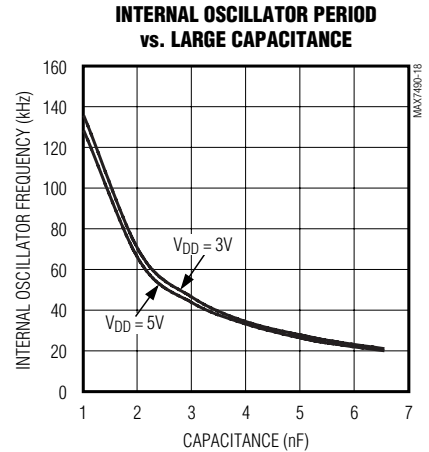
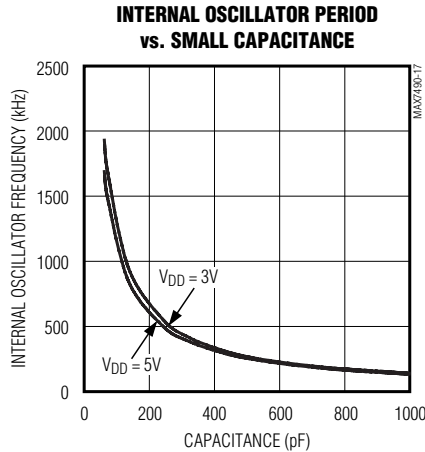
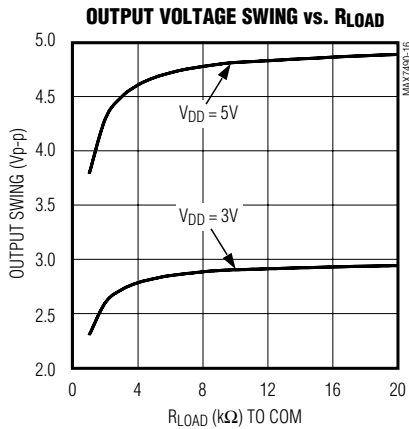
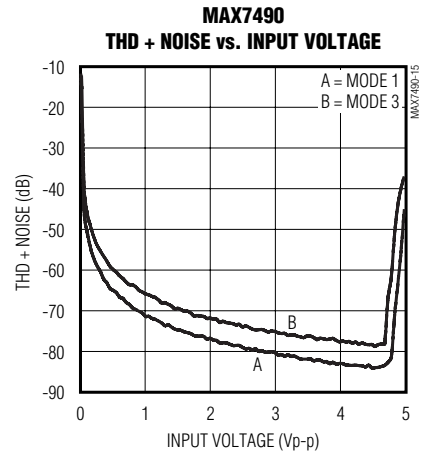
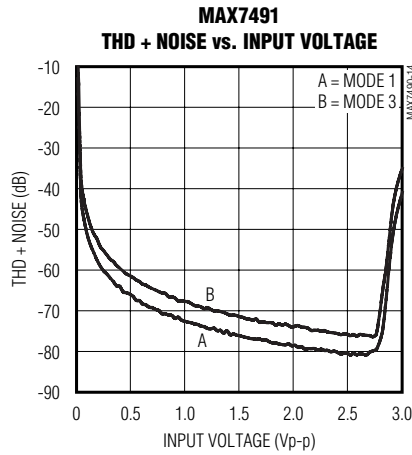
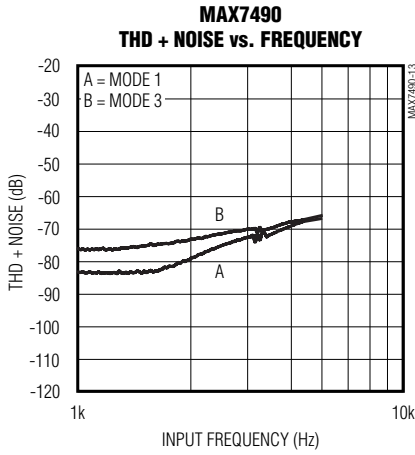


# Dual Universal Switched-Capacitor Filters

## Typical Operating Characteristics (continued)

( $V_{DD} = +5V$  for MAX7490,  $V_{DD} = +3V$  for MAX7491,  $f_{CLK} = 625kHz$ ,  $\overline{SHDN} = \overline{EXTCLK} = V_{DD}$ ,  $COM = V_{DD}/2$ , Mode 1,  $R3 = R1 = 50k\Omega$ ,  $R2 = 10k\Omega$ ,  $Q = 5$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX7490/MAX7491



# Dual Universal Switched-Capacitor Filters

## Pin Description

| PIN                      | NAME     |          | FUNCTION   |
|--------------------------|----------|----------|--|
|                          | FILTER A | FILTER B |  |
| LP_                      | 1        | 16       | 2nd-Order Lowpass Filter Output  |
| BP_                      | 2        | 15       | 2nd-Order Bandpass Filter Output   |
| N_/HP_                   | 3        | 14       | 2nd-Order Notch/Highpass Filter Output   |
| INV_                     | 4        | 13       | Inverting Input of Filter Summing Op Amp   |
| S_                       | 5        | 12       | Summing Input. The connection of the summing input, along with the other resistor connections, determine the circuit topology (mode) of each 2nd-order section. S_ must never be left floating.  |
| $\overline{\text{SHDN}}$ | 6        |          | Shutdown Input. Drive $\overline{\text{SHDN}}$ low to enable shutdown mode; drive high or connect to $V_{DD}$ for normal operation.  |
| GND                      | 7        |          | Ground Pin   |
| $V_{DD}$                 | 8        |          | Positive Supply. $V_{DD}$ should be bypassed with a 0.1 $\mu$ F capacitor to GND. A low-noise supply is recommended. Input +5V for MAX7490 or +3V for MAX7491.   |
| CLK                      | 9        |          | Clock Input. Connect to an external capacitor ( $C_{OSC}$ ) between CLK and ground to set the internal oscillator frequency. For external clock operation, drive with a CMOS-level clock. The duty cycle of the external clock should be between 45% and 55% for best performance. |
| EXTCLK                   | 10       |          | External/Internal Clock Select Input. Connect EXTCLK to $V_{DD}$ when driving CLK externally. Connect to GND when using the internal oscillator.   |
| COM                      | 11       |          | Common Pin. Biased internally at $V_{DD}/2$ . Bypass externally to GND with 0.1 $\mu$ F capacitor. To override the internal biasing, drive with an external low-impedance source.  |

### Detailed Description

The MAX7490/MAX7491 are universal switched-capacitor filters designed with a fixed internal  $f_{CLK}/f_0$  ratio of 100:1. Operating modes use external resistors connected in different arrangements to realize different filter functions (highpass, lowpass, bandpass, notch) in all of the classical filter topologies (Butterworth, Bessel, elliptic, Chebyshev). Figure 1 shows a block diagram.

#### Clock Signal

##### External Clock

The MAX7490/MAX7491 switched-capacitor filters are designed for use with external clocks that have a 50%  $\pm$ 5% duty cycle. When using an external clock, drive the EXTCLK pin high or connect to  $V_{DD}$ . Drive CLK with CMOS logic levels (GND and  $V_{DD}$ ). Varying the rate of

the external clock adjusts the center frequency of the filter:

$$f_0 = f_{CLK} / 100$$

##### Internal Clock

When using the internal oscillator, drive the EXTCLK pin low or connect to GND and connect a capacitor ( $C_{OSC}$ ) between CLK and GND. The value of the capacitor ( $C_{OSC}$ ) determines the oscillator frequency as follows:

$$f_{OSC} \text{ (kHz)} = 135 \times 10^3 / C_{OSC} \text{ (pF)}$$

Since  $C_{OSC}$  is in the low picofarads, minimize the stray capacitance at CLK so that it does not affect the internal oscillator frequency. Varying the frequency of the internal oscillator adjusts the filter's center frequency by a 100:1 clock-to-center frequency ratio. For example, an internal oscillator frequency of 135kHz produces a nominal center frequency of 1.35kHz.



# Dual Universal Switched-Capacitor Filters

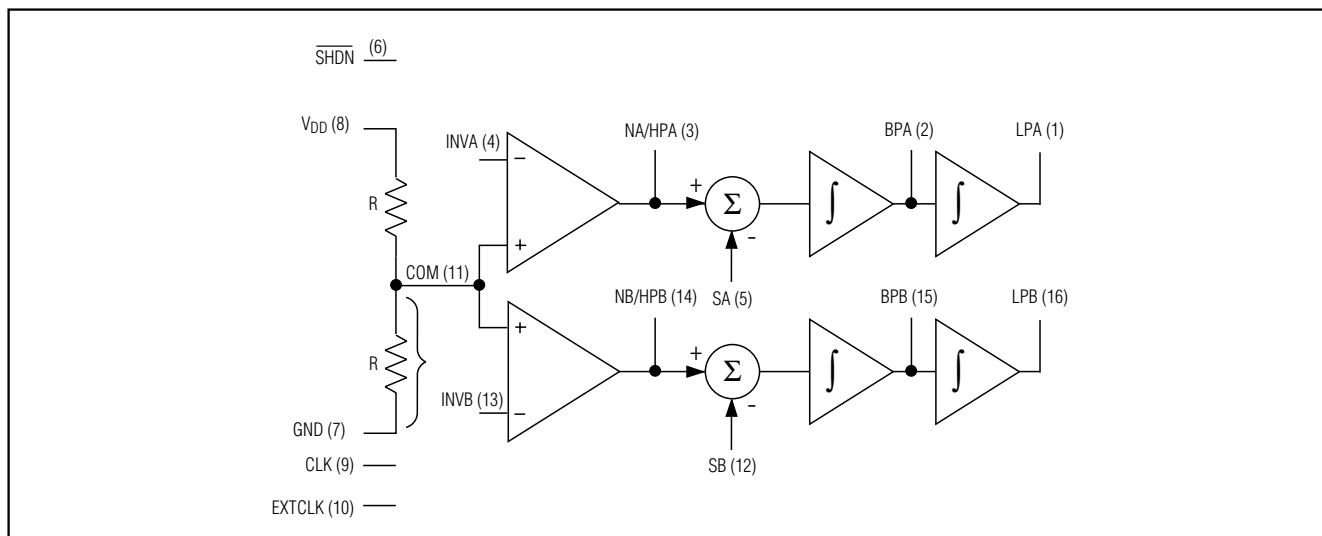


Figure 1. Block Diagram

## 2nd-Order Filter Stage

The MAX7490/MAX7491 are dual biquad filters. The biquad topology allows the use of standard filter tables and equations to implement simultaneous lowpass, bandpass, and notch or highpass filters. Topologies such as Butterworth, Chebyshev, Bessel, elliptic, as well as custom algorithms are possible.

## Internal Common Voltage

The COM pin sets the common-mode input voltage and is internally biased to  $V_{DD}/2$  with a resistor-divider. The resistors used are typically  $250k\Omega$  for the MAX7490, and typically  $80k\Omega$  for the MAX7491. The common-mode voltage is easily overdriven by an external voltage supply if desired. The COM pin should be bypassed to the analog ground with at least a  $0.1\mu F$  capacitor.

## Inverting Inputs

Locate resistors that are connected to INV\_ as close as possible to INV\_ to reduce stray capacitance and noise pickup. INV\_ are inverting inputs to continuous-time op amps, and behave like a virtual ground. There is no sampling energy present on these inputs.

## Outputs

Each switched-capacitor section, together with two to four external resistors, can generate all standard 2nd-order functions: bandpass, lowpass, highpass, and notch (band-reject) functions. Three of these functions are simultaneously available. The maximum signal swing is limited by the power-supply voltages used. The amplifiers' outputs in the MAX7490/MAX7491 are

able to swing to within approximately 0.2V of either supply.

Driving coaxial cable, large capacitive loads, or total resistive loads less than  $10k\Omega$  will degrade the total harmonic distortion (THD) performance. Note that the effective resistive load at the output must include both the feedback resistors and any external load resistors.

## Low-Power Shutdown Mode

The MAX7490/MAX7491 have a shutdown mode that is activated by driving  $\overline{SHDN}$  low. In shutdown mode, the filter supply current reduces to  $<1\mu A$  (max), and the filter outputs become high impedance. The COM input also becomes high impedance during shutdown. For normal operation, drive  $\overline{SHDN}$  high or connect to  $V_{DD}$ .

## Applications Information

Designing with the MAX7490/MAX7491 begins by selecting the mode that best fits the desired circuit requirements. Table 1 lists the available modes and their relative advantages and disadvantages. Table 2 lists the different nomenclature used in the explanations that follow.

### Mode 1

Figure 2 shows the MAX7490/MAX7491s' configuration of Mode 1. This mode provides 2nd-order notch, lowpass, and bandpass filter functions. The gain at all three outputs is inversely proportional to the value of R1. The center frequency,  $f_0$ , is fixed at  $f_{CLK}/100$ . High-Q bandpass filters can be built without exceeding the bandpass amplifier's output swing (i.e., HOBP does not

# Dual Universal Switched-Capacitor Filters

**Table 1. Filter Operating Modes**

| MODE | LP | HP | BP | N | LP-N* | HP-N* | COMMENTS  |
|------|----|----|----|---|-------|-------|---|
| 1    | •  |    | •  | • |       |       | $f_{CLK}/f_0$ ratio is the nominal value. Good for bandpass filters with identical sections cascaded, higher order Butterworth filters, high-Q bandpass, low-Q notches.   |
| 1B   | •  |    | •  | • |       |       | Same as Mode 1 with $f_{CLK}/f_0$ ratios greater than the nominal value.  |
| 2    | •  |    | •  | • |       |       | Combination of Mode 1 and Mode 3; $f_{CLK}/f_0$ ratios always less than the nominal value. Less sensitivity to resistor tolerances than Mode 3.                           |
| 2N   |    |    |    |   | •     |       | Extension of Mode 2 that allows higher frequencies. Highpass and lowpass outputs are summed with external op amp and two resistors. Good for lowpass elliptic filters.    |
| 3    | •  | •  | •  |   |       |       | Adjustable $f_0$ above and below the nominal frequency. Commonly used for multiple-pole Chebyshev filters, all-pole higher order bandpass, lowpass, and highpass filters. |
| 3A   | •  | •  | •  |   | •     | •     | Extension of Mode 3 that needs an external op amp and two additional resistors. Commonly used for lowpass or higher elliptic or Cauer filters.                            |

\* LP-N = lowpass notch, HP-N = highpass notch. Both require an external op amp. See Definition of Terms (Table 2).

**Table 2. Definition of Terms**

| TERM        | DEFINITION   |
|-------------|--|
| $f_{CLK}$   | The clock frequency applied to the switched-capacitor filter.  |
| $f_0$       | The center frequency of the 2nd-order complex pole pair, $f_0$ , is determined by measuring the peak response frequency at the bandpass output.  |
| $f_{NOTCH}$ | The frequency of minimum amplitude response at the notch output.   |
| Q           | Quality factor, or Q, is the ratio of $f_0$ to the -3dB bandwidth of the 2nd-order bandpass filter. Q also determines the amount of amplitude peaking at the lowpass and highpass outputs, but is not measured at these outputs. |
| HOBP        | The gain in V/V of the bandpass output at $f = f_0$ .  |
| HOLP        | The gain in V/V of the lowpass output at $f \rightarrow 0$ Hz.   |
| HOHP        | The gain in V/V of the highpass output at $f \rightarrow f_{CLK}/2$ .  |
| HON1        | The notch output gain as $f \rightarrow 0$ Hz.   |
| HON2        | The notch output gain at $f = f_{CLK}/2$ .   |
| LP-N        | A notch output with $H_{ON1} > H_{ON2}$ .  |
| HP-N        | A notch output with $H_{ON1} < H_{ON2}$ .  |

# Dual Universal Switched-Capacitor Filters

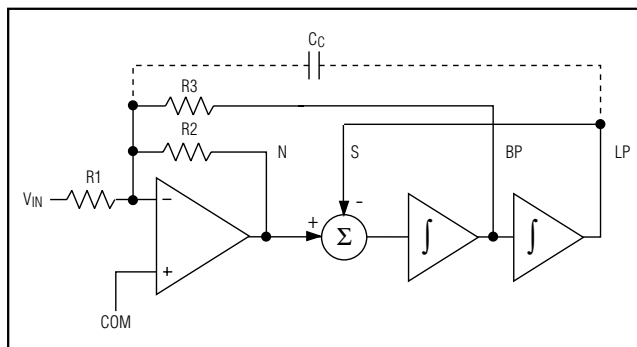


Figure 2. Mode 1, 2nd-Order Filter Providing Notch, Bandpass, and Lowpass Outputs

have to track Q). The notch and bandpass center frequencies are identical. The notch output gain is the same above and below the notch center frequency. Mode 1 can also be used to make high-order Butterworth lowpass filters, low Q notches, and multiple-order bandpass filters obtained by cascading identical switched-capacitor sections.

### Mode 1 Design Equations

$$f_0 = \frac{f_{CLK}}{100}$$

$$f_{notch} = f_0$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = \frac{-R2}{R1}$$

$$H_{OBP} = \frac{-R3}{R1}$$

$$H_{ON1}(as\ f \rightarrow 0Hz) = \frac{-R2}{R1}$$

$$H_{ON2}(at\ f = f_{CLK} / 2) = \frac{-R2}{R1}$$

### Mode 1B

Figure 3 shows the configuration of Mode 1B. R5 and R6 are added to lower the feedback voltage from the lowpass output to the summing input. This allows the clock-to-center frequency to be adjusted beyond the nominal value. This mode essentially has the same functions and speed as Mode 1 while providing a high-Q with  $f_{CLK}/f_0$  ratios greater than the nominal value.

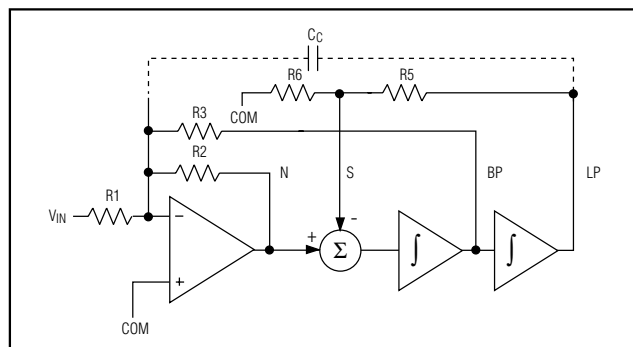


Figure 3. Mode 1B, 2nd-Order Filter Providing Notch, Bandpass, and Lowpass Outputs

### Mode 1B Design Equations

$$f_0 = \frac{f_{CLK}}{100} \sqrt{\frac{R6}{R6 + R5}}$$

$$f_n = f_0$$

$$Q = \frac{R3}{R2} \sqrt{\frac{R6}{R6 + R5}}$$

$$H_{OLP} = \frac{-R2}{R1} \frac{R6 + R5}{R6}$$

$$H_{OBP} = \frac{-R3}{R1}$$

$$H_{ON1}(as\ f \rightarrow 0Hz) = \frac{-R2}{R1}$$

$$H_{ON2}(at\ f = f_{CLK} / 2) = \frac{-R2}{R1}$$

### Mode 2

Figure 4 shows the configuration of Mode 2. Mode 2 is a combination of Mode 1 and Mode 3. In this mode,  $f_{CLK}/f_0$  is always less than the part's nominal ratio. However, it provides less sensitivity to resistor tolerances than does Mode 3. It has a highpass notch output where the notch frequency depends solely on the clock frequency.

# Dual Universal Switched-Capacitor Filters

## Mode 2 Design Equations

$$f_O = \frac{f_{CLK}}{100} \sqrt{1 + \frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100}$$

$$Q = \frac{R3}{R2} \sqrt{1 + \frac{R2}{R4}}$$

$$H_{OLP} = \frac{-R2}{R1} \left( \frac{R4}{R4 + R2} \right)$$

$$H_{OBP} = \frac{-R3}{R1}$$

$$H_{ON1}(f \rightarrow 0Hz) = \frac{-R2}{R1} \left( \frac{R4}{R4 + R2} \right)$$

$$H_{ON2}(at f = f_{CLK} / 2) = \frac{-R2}{R1}$$

### Mode 2N

Figure 5 shows the configuration of Mode 2N. This mode extends the topology of Mode 3A to Mode 2, where the highpass and lowpass outputs are summed through two external resistors,  $R_H$  and  $R_L$ , to create a lowpass notch filter that has higher frequency than the one in Mode 2. Mode 2 is most useful in lowpass elliptic designs. When cascading the sections of the MAX7490/MAX7491, the highpass and lowpass outputs can be summed directly into the inverting input of the next section. Only one external op amp is needed.

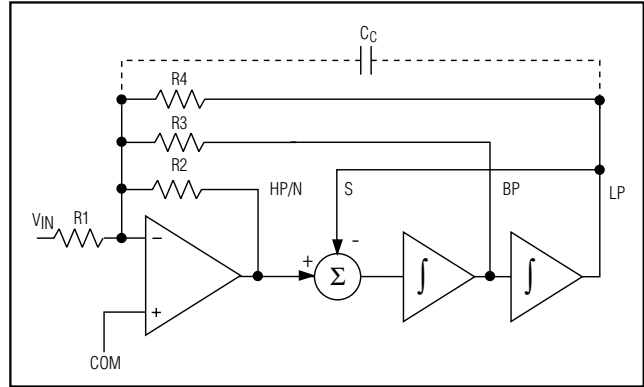


Figure 4. Mode 2, 2nd-Order Filter Providing a Highpass Notch, Bandpass, and Lowpass Outputs

## Mode 2N Design Equations

$$f_O = \frac{f_{CLK}}{100} \sqrt{1 + \frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100} \sqrt{1 + \frac{R_H}{R_L}}$$

$$Q = \frac{R3}{R2} \sqrt{1 + \frac{R2}{R4}}$$

$$H_{ON1}(f \rightarrow 0Hz) = \left( \frac{R_G}{R_H} + \frac{R_G}{R_L} \right) \left( \frac{R2}{R1} \right) \left( \frac{R4}{R4 + R2} \right)$$

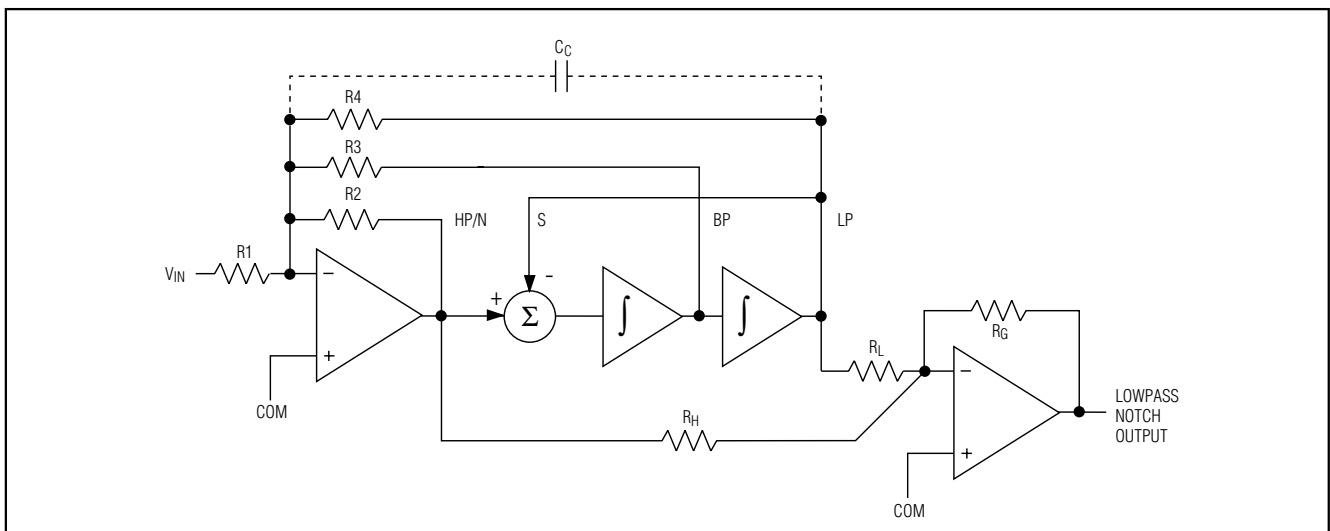


Figure 5. Mode 2N, 2nd-Order Filter Providing a Lowpass Notch Output

# Dual Universal Switched-Capacitor Filters

## Mode 3

Figure 6 shows the configuration of Mode 3. This mode is a sampled time (Z transform) equivalent of the classical 2nd-order state variable filter. In this versatile mode, the ratio of resistors R2 and R4 can move the center frequency both above and below the nominal ratio. Mode 3 is commonly used to make multiple-pole Chebyshev filters with a single clock frequency. This mode can also be used to make high-order all-pole bandpass, lowpass, and highpass filters.

### Mode 3 Design Equations

$$f_0 = \frac{f_{CLK}}{100} \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \sqrt{\frac{R2}{R4}}$$

$$H_{OHP} = \frac{-R2}{R1}$$

$$H_{OLP} = \frac{-R4}{R1}$$

$$H_{OBP} = \frac{-R3}{R1}$$

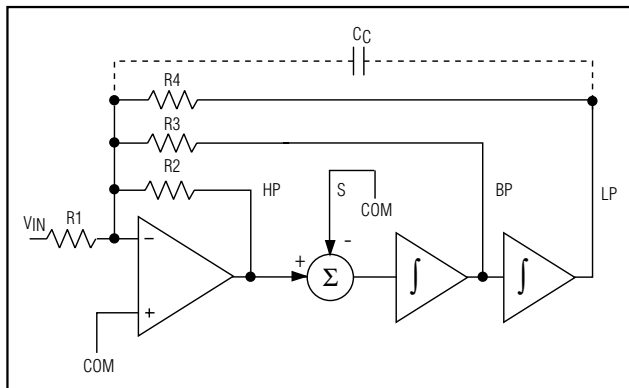


Figure 6. Mode 3, 2nd-Order Section Providing Highpass, Bandpass, and Lowpass Outputs

the highpass and lowpass outputs through two external resistors, R<sub>H</sub> and R<sub>L</sub>. The ratio of resistors R<sub>H</sub> and R<sub>L</sub> adjusts the notch frequency, while R<sub>2</sub> and R<sub>4</sub> adjust the bandpass center frequency, since the notch (zero pair) frequency can be adjusted to both above and below f<sub>0</sub>. Mode 3A is suitable for both lowpass and highpass elliptic or Cauer filters. In multipole elliptic filters, only one external op amp is needed. Use the inverting input of the internal op amp as the summing node for all but the final section of the filter.

## Mode 3A

Figure 7 shows the configuration of Mode 3A. Similar to Mode 2, this mode adds an external op amp. See Table 3 for op amp selection ideas. This op amp creates a highpass notch and lowpass notch by summing

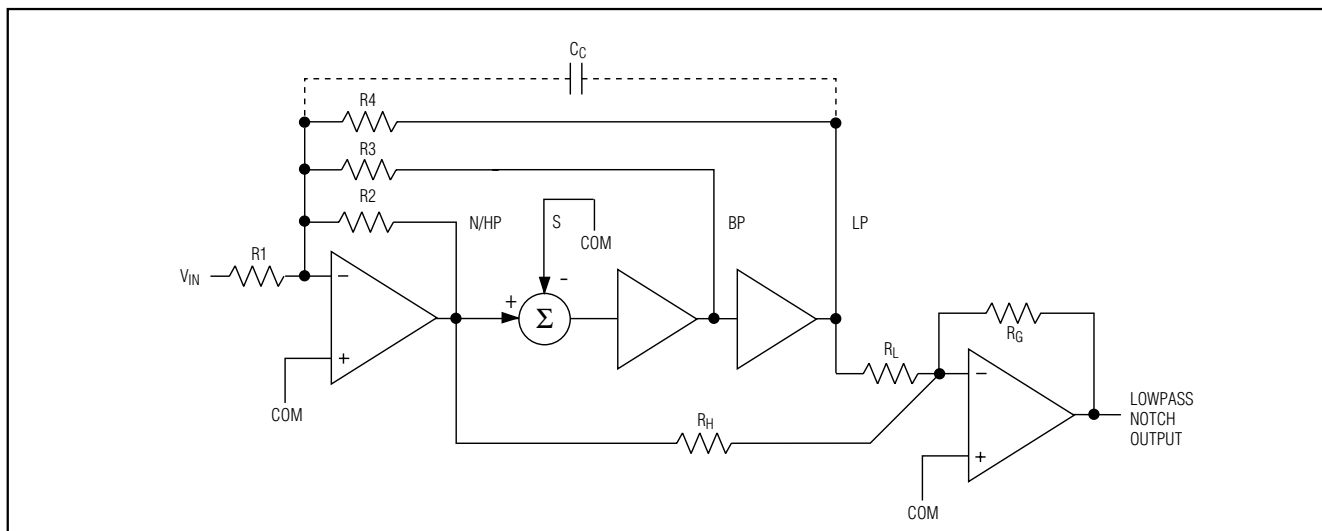


Figure 7. Mode 3A, 2nd-Order Filter Providing Highpass Notch or Lowpass Notch Outputs

# Dual Universal Switched-Capacitor Filters

**Table 3. Suggested External Op Amps**

| PART    | GBW (MHz) | SLEW RATE (V/μs) | ISUPPLY/AMP (mA) | PIN-PACKAGE |
|---------|-----------|------------------|------------------|-------------|
| MAX4281 | 2         | 0.7              | 0.5              | 5 SOT23     |
| MAX4322 | 5         | 2.0              | 1.1              | 5 SOT23     |
| MAX4130 | 10        | 4.0              | 1.15             | 5 SOT23     |
| MAX4490 | 10        | 10.0             | 2.0              | 5 SOT23     |

**Mode 3A Design Equations**

$$f_o = \frac{f_{CLK}}{100} \sqrt{\frac{R_2}{R_4}}$$

$$f_h = \frac{f_{CLK}}{100} \sqrt{\frac{R_H}{R_L}}$$

$$Q = \frac{R_3}{R_2} \sqrt{\frac{R_2}{R_4}}$$

$$H_{OHP} = \frac{-R_2}{R_1}$$

$$H_{OLP} = \frac{-R_4}{R_1}$$

$$H_{OBP} = \frac{-R_3}{R_1}$$

$$H_{ON1}(f \rightarrow 0Hz) = \frac{R_G}{R_L} \left( \frac{R_4}{R_1} \right)$$

$$H_{ON2}(at f = f_{CLK} / 2) = \frac{R_G}{R_H} \left( \frac{R_2}{R_1} \right)$$

**Note:** When the passband gain error exceeds 1dB, the use of capacitor C<sub>C</sub> between the lowpass output and the inverting input will reduce the gain error. The value can best be determined experimentally. Typically, it should be about 5pF/dB (C<sub>C</sub>-MAX = 15pF).

**Offset Voltage**

Switched-capacitor integrators generally exhibit higher input offsets than discrete RC integrators. The larger offset is mainly due to the charge injection of the CMOS switches into the integrating capacitors. The internal op amp offset also adds to the overall offset value. Figure 8 shows the input offsets from a single 2nd-order section. Table 4 lists the formula for the output offset voltage for various modes and output pins.

**Power Supplies**

The MAX7490 operates from a single +5V supply, and the MAX7491 operates from a single +3V supply. Bypass V<sub>DD</sub> to GND with at least a 0.1μF capacitor. V<sub>DD</sub> should be isolated from other digital or high-voltage analog supplies. If dual supplies are required, connect the COM pin to the system ground and the GND pin to the negative supply. Figure 9 shows an example of dual-supply operation. Single-supply and dual-supply performances are equivalent. For dual-supply operation, drive CLK, SHDN, and EXTCLK from GND (which is now V<sub>-</sub>) to V<sub>DD</sub>. If using the internal oscillator in dual-supply mode, COSC can be returned to either GND or the actual ground voltage. Use the MAX7490 for ±2.5V and use the MAX7491 for ±1.5V.

For most applications, a 0.1μF bypass capacitor from COM to GND is sufficient. If the V<sub>DD</sub> supply has significant 60Hz energy, increase this capacitor to 1μF or greater to provide better power-supply rejection.

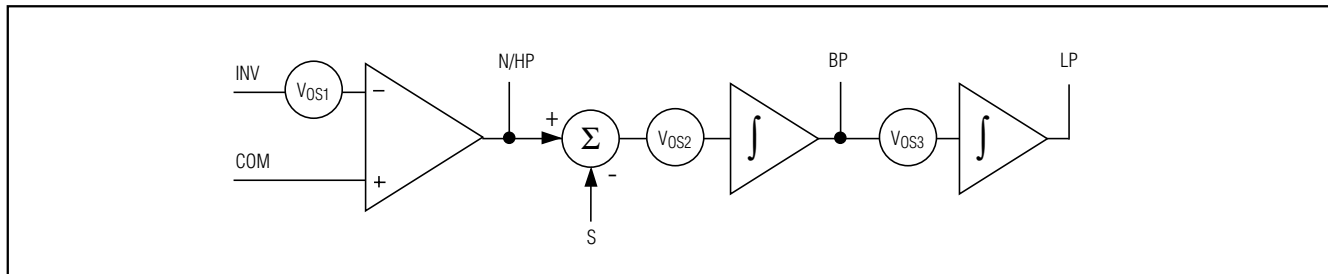


Figure 8. Block Diagram of a 2nd-Order Section Showing the Input Offsets

# Dual Universal Switched-Capacitor Filters

**Table 4. Output DC Offsets for a 2nd-Order Section**

| MODE | VOSN/HP   | VOSBP     | VOSLP   |
|------|---|-----------|---|
| 1    | $V_{OS1}[1 + (R2 / R3) + (R2 / R1)] - (V_{OS3}) (R2 / R3)$  | $V_{OS3}$ | $V_{OSN/HP} - V_{OS2}$  |
| 1b   | $V_{OS1}[1 + (R2 / R3) + (R2 / R1)] - (V_{OS3}) (R2 / R3)$  | $V_{OS3}$ | $(V_{OSN/HP} - V_{OS2})[1 + R5 / R6]$   |
| 2    | $V_{OS1}[1 + (R2 / R3) + (R2 / R1) + (R2 / R4) - (V_{OS3})(R2 / R3)][R4 / R2 + R4] + (V_{OS2})[R2 / R2 + R4]$ | $V_{OS3}$ | $V_{OSN/HP} - V_{OS2}$  |
| 3    | $V_{OS2}$   | $V_{OS3}$ | $V_{OS1}[1 + (R4 / R1) + (R4 / R2) + (R4 / R3)] - (V_{OS2}) (R4 / R2) - (V_{OS3})(R4 / R3)$ |

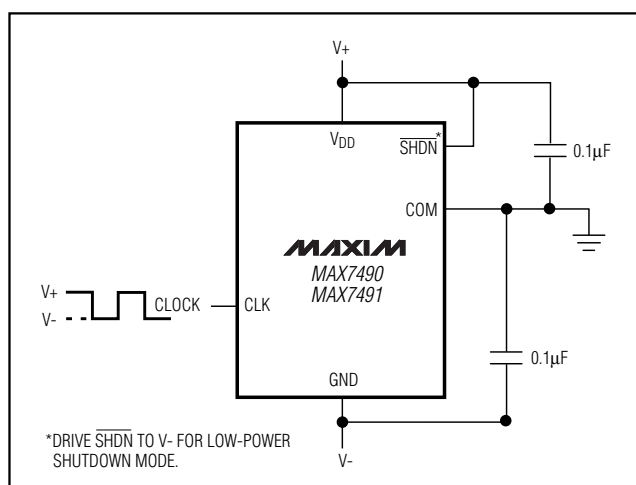


Figure 9. Dual-Supply Operation

### Input Signal Amplitude Range

The optimal input signal range is determined by observing the voltage level at which the signal-to-noise plus distortion (SINAD) ratio is maximized for a given corner frequency. The *Typical Operating Characteristics* show the THD + Noise response as the input signal's peak-to-peak amplitude is varied. In most systems, the input signal should be kept as large as possible to maximize the signal-to-noise ratio (SNR). Allow sufficient headroom to ensure no signal clipping under expected operating conditions.

### Anti-Aliasing and Post-DAC Filtering

When using the MAX7490/MAX7491 for anti-aliasing or post-DAC filtering, synchronize the DAC (or ADC) and the filter clocks. If the clocks are not synchronized, beat frequencies may alias into the desired passband.

### Aliasing

Aliasing is an inherent phenomenon of most switched-capacitor filters. As with all sampled systems, frequency components of the input signal above one half the sampling rate will be aliased. The MAX7490/MAX7491 sample at twice the clock frequency, yielding a 200:1 sampling to cutoff frequency ratio.

In particular, input signal components ( $f_{IN}$ ) near the sampling rate generate a difference frequency ( $f_{SAMPLING} - f_{IN}$ ) that often falls within the passband of the filter. Such aliased signals, when they appear at the output, are indistinguishable from real input information. For example, the aliased output signal generated when a 99kHz waveform is applied to a filter sampling at 100kHz, ( $f_{CLK} = 50kHz$ ) is 1kHz. This waveform is an attenuated version of the output that would result from a true 1kHz input. Since sampling is done at twice the clock frequency, the Nyquist frequency is the same as the clock frequency.

A simple passive RC lowpass input filter is usually sufficient to remove input frequencies that can be aliased. In many cases, the input signal itself may be band limited and require no special anti-alias filtering. Selecting a passive filter cutoff frequency equal to  $f_C/2$  gives 12dB rejection at the Nyquist frequency.

### Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pins, even without input signal. The clock feedthrough can be greatly reduced by adding a simple RC lowpass network at the final filter output. Choose a cutoff frequency as low as possible to provide maximum noise attenuation. The attenuation and phase shift of the external filter will limit the actual frequency selected.

# Dual Universal Switched-Capacitor Filters

**Table 5. Cascading Identical Bandpass Filter Sections**

| TOTAL SECTIONS | TOTAL BW | TOTAL Q |
|----------------|----------|---------|
| 1              | 1.000 B  | 1.00 Q  |
| 2              | 0.644 B  | 1.55 Q  |
| 3              | 0.510 B  | 1.96 Q  |
| 4              | 0.435 B  | 2.30 Q  |
| 5              | 0.386 B  | 2.60 Q  |

### Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and is used to determine the operating SNR. Most of its frequency contents lie within the filter's passband and cannot be reduced with postfiltering. The total noise depends mainly on the Q of each filter section and the cascade sequence. Therefore, in multistage filters, the section with the highest Q should be placed first for lower output noise.

### Multiple Filter Stages

In some designs, such as very narrow band filters, or in modes where  $f_0$  cannot be tuned with resistors, several 2nd-order sections with identical  $f_0$  may be cascaded without multiple feedback. The total Q of the resultant filter ( $Q_T$ ) is:

$$\text{Total } Q_T = Q / (2^N - 1)^{1/2}$$

Q is the Q of each individual filter section, and N is the number of 2nd-order sections. In Table 5, the total Q and total bandwidth (BW) are listed for up to five identical 2nd-order sections. B is the bandwidth of each section.

### Chip Information

TRANSISTOR COUNT: 1439

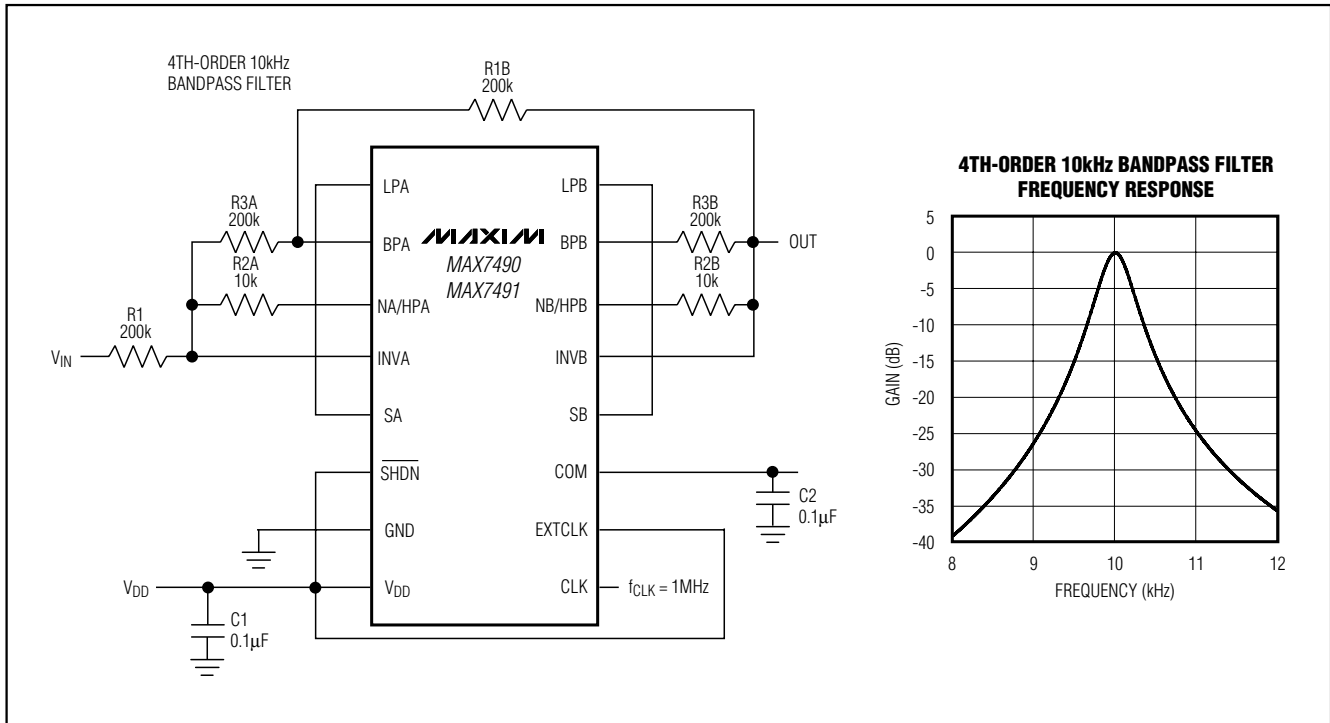
TECHNOLOGY: BiCMOS



# Dual Universal Switched-Capacitor Filters

## Typical Application Circuit

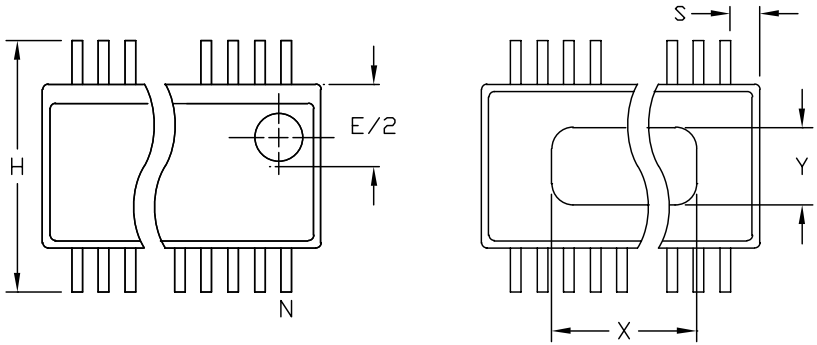
MAX7490/MAX7491



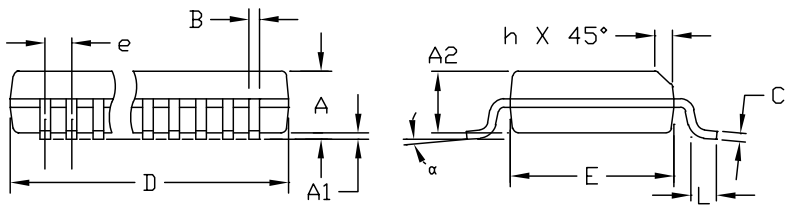
# Dual Universal Switched-Capacitor Filters

## Package Information

QSOP-EPS



| DIM | INCHES         |       | MILLIMETERS |       |
|-----|----------------|-------|-------------|-------|
|     | MIN            | MAX   | MIN         | MAX   |
| A   | .061           | .068  | 1.55        | 1.73  |
| A1  | .004           | .0098 | 0.102       | 0.249 |
| A2  | .055           | .061  | 1.40        | 1.55  |
| B   | .008           | .012  | 0.20        | 0.31  |
| C   | .0075          | .0098 | 0.191       | 0.249 |
| D   | SEE VARIATIONS |       |             |       |
| E   | .150           | .157  | 3.81        | 3.99  |
| e   | .025 BSC       |       | 0.635 BSC   |       |
| H   | .230           | .244  | 5.84        | 6.20  |
| h   | .010           | .016  | 0.25        | 0.41  |
| L   | .016           | .035  | 0.41        | 0.89  |
| N   | SEE VARIATIONS |       |             |       |
| X   | SEE VARIATIONS |       |             |       |
| Y   | .071           | .087  | 1.803       | 2.209 |
| α   | 0°             | 8°    | 0°          | 8°    |



**NOTES:**

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

**VARIATIONS:**

| DIM | INCHES |       | MILLIMETERS |       | N  |
|-----|--------|-------|-------------|-------|----|
|     | MIN.   | MAX.  | MIN.        | MAX.  |    |
| D   | .189   | .196  | 4.80        | 4.98  | 16 |
| S   | .0020  | .0070 | 0.05        | 0.18  |    |
| X   | .107   | .123  | 2.72        | 3.12  |    |
| D   | .337   | .344  | 8.56        | 8.74  | 20 |
| S   | .0500  | .0550 | 1.270       | 1.397 |    |
| D   | .337   | .344  | 8.56        | 8.74  | 24 |
| S   | .0250  | .0300 | 0.635       | 0.762 |    |
| D   | .386   | .393  | 9.80        | 9.98  | 28 |
| S   | .0250  | .0300 | 0.635       | 0.762 |    |
| X   | .271   | .287  | 6.88        | 7.29  |    |

**MAXIM**

PROPRIETARY INFORMATION

TITLE:  
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

|          |                      |     |     |
|----------|----------------------|-----|-----|
| APPROVAL | DOCUMENT CONTROL NO. | REV |     |
|          | 21-0055              | B   | 1/1 |

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