19-2126; Rev 1; 10/01

MAXIM

12-Bit, Low-Power, Rail-to-Rail Voltage-Output Serial DAC in SOT23

General Description

The MAX5712 is a small footprint, low-power, 12-bit digital-to-analog converter (DAC) that operates from a single +2.7V to +5.5V supply. The MAX5712 on-chip precision output amplifier provides Rail-to-Rail® output swing. Drawing only 85µA supply current at +3V, the MAX5712 is ideally suited for portable battery-operated equipment.

The MAX5712 utilizes a 3-wire serial-interface that is compatible with SPI™/QSPI™/MICROWIRE™ and DSP-interface standards. All logic inputs are CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers. The MAX5712 incorporates a power-on reset (POR) circuit that ensures the DAC begins in a zero-volt-state upon power-up. A power-down mode that reduces current consumption to 0.3µA may be initiated through a software command.

The MAX5712 is available in a small 6-pin SOT23 package. For dual and quad 12-bit versions, see the MAX5722 and MAX5742 data sheets. For single, dual, and quad 10-bit versions, see the MAX5711, MAX5721 and MAX5741 data sheets. The MAX5712 is specified over the automotive temperature range of -40°C to +125°C.

Applications

Automatic Tuning
Gain and Offset Adjustment
Power Amplifier Control
Process Control I/O Boards
Battery-Powered Equipment
VCO Control

Features

- **Wide -40°C to +125°C Operating Temperature Range**
- **Low 85µA Supply Current**
- **Ultra Low 0.3µA Power-Down Supply Current**
- **Single +2.7V to +5.5V Supply Voltage**
- **Fast 20MHz 3-Wire SPI/QSPI/MICROWIRE and DSP-Compatible Serial Interface**
- **Schmitt-Triggered Inputs for Direct Interfacing to Optocouplers**
- **Rail-to-Rail Output Buffer**
- **Tiny 6-Pin SOT23 Package**
- **Power-On Reset to 0V**
- **Three Software-Selectable Power-Down Output Impedances (100kΩ, 1kΩ, Hi-Z)**

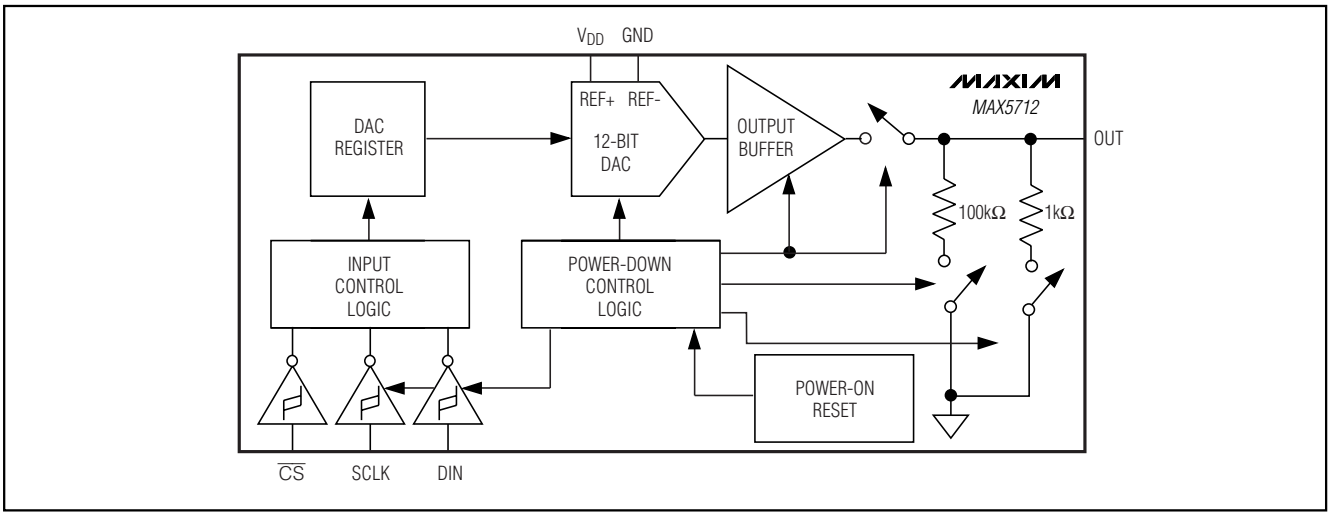
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX5712EUT	-40°C to +85°C	6 SOT23	ABCQ
MAX5712AUT	-40°C to +125°C	6 SOT23	AAUD

Pin Configuration appears at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.
SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor, Corp.

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

12-Bit, Low-Power, Rail-to-Rail Voltage-Output Serial DAC in SOT23

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUT, SCLK, DIN, $\overline{CS}$ to GND .....-0.3V to (V_{DD}+ 0.3V)
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V. T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (NOTE 1)						
Resolution	N		12			Bits
Differential Nonlinearity Error	DNL	Guaranteed monotonic (Note 2)			±1	LSB
Integral Nonlinearity Error	INL	(Note 2)		±2	±16	LSB
Zero-Code Error	OE	Code = 000		0.4	1.5	% of FS
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = FFF hex			-3	% of FS
Gain-Error Tempco		Integral		0.26		ppm/°C
DAC OUTPUT						
Output Voltage Range		No-load (Note 3)	0		V_{DD}	V
DC Output Impedance		Code = 800 hex		0.8		Ω
Short Circuit Current		V_{DD} = +3V		15		mA
		V_{DD} = +5V		48		
Wake-Up Time		V_{DD} = +3V		8		µs
		V_{DD} = +5V		8		
Output Leakage Current		Power-down mode = output high-impedance		±18	±33	nA
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)						
Input High Voltage	V_{IH}	V_{DD} = +3V, +5V	0.7 x V_{DD}			V
Input Low Voltage	V_{IL}	V_{DD} = +3V, +5V			0.3 x V_{DD}	V
Input Leakage Current	I_{IN}	Digital Inputs = 0 or V_{DD}		±0.1	±1	µA
Input Capacitance	C_{IN}			5		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.5		V/µs
Voltage-Output Settling Time		400 hex to C00 hex (Note 4)		4	10	µs
Digital Feedthrough		Any digital inputs from 0 to V_{DD}		0.2		nV-s
Digital-Analog Glitch Impulse		Major carry transition (code 7FF hex to code 800 hex)		12		nV-s

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +5V. T_A = +25°C)

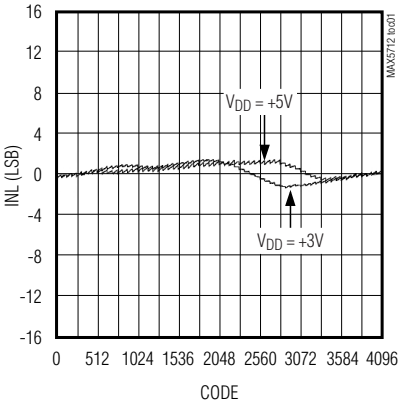
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No-Load	I_{DD}	All digital inputs at 0 or V_{DD}, V_{DD} = +3.6V		85	150	µA
		All digital inputs at 0 or V_{DD}, V_{DD} = +5.5V		105	187	
Power-Down Supply Current	I_{DDPD}	All digital inputs at 0 or V_{DD}, V_{DD} = +5.5V		0.29	1	µA
TIMING CHARACTERISTICS (FIGURE 2) (TIMING IS TESTED WITH NO-LOAD)						
SCLK Clock Frequency	f_{SCLK}		0		20	MHz
SCLK Pulse Width High	t_{CH}		20			ns
SCLK Pulse Width Low	t_{CL}		20			ns
$\overline{CS}$ Fall-to-SLCK Rise Setup	t_{CSS}		15			ns
DIN Setup Time	t_{DS}		15			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Falling Edge-to-$\overline{CS}$ Rising Edge	t_{CSH}		10			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		80			ns

Note 1: DC Specifications are tested without output loads.
Note 2: Linearity guaranteed from code 115 to code 3981.
Note 3: Offset and gain error limit the FSR.
Note 4: Guaranteed by design.

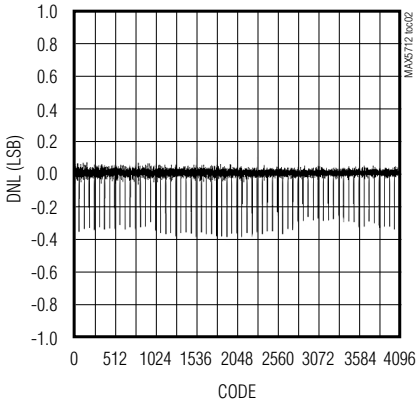
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

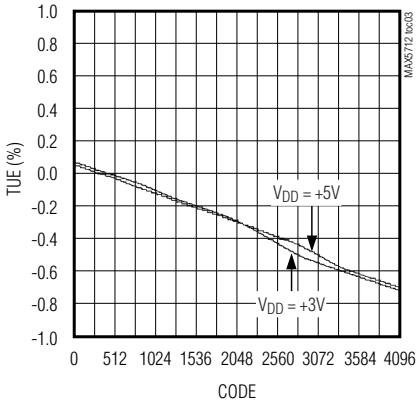
INTEGRAL NONLINEARITY vs. CODE, T_A = +25°C



DIFFERENTIAL NONLINEARITY vs. CODE, T_A = +25°C



TOTAL UNADJUSTED ERROR vs. CODE, T_A = +25°C

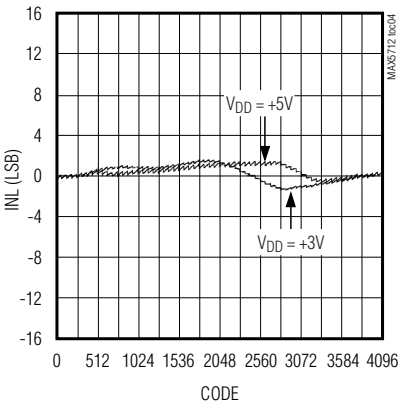


12-Bit, Low-Power, Rail-to-Rail Voltage-Output Serial DAC in SOT23

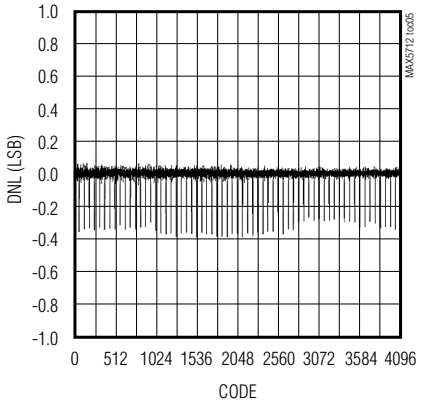
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

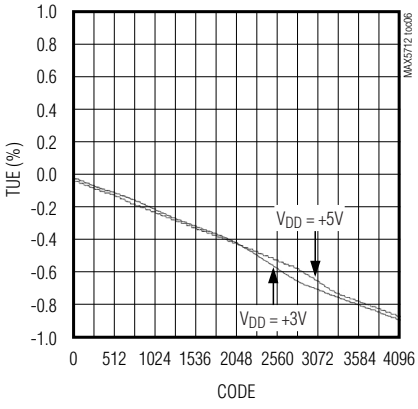
INTEGRAL NONLINEARITY vs. CODE, T_A = -40°C



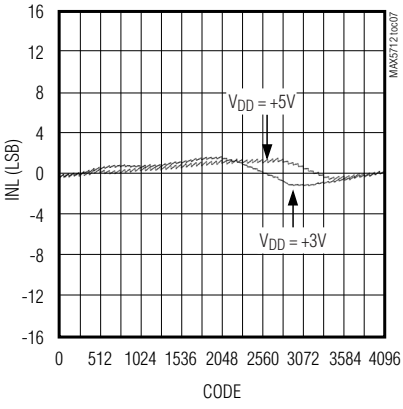
DIFFERENTIAL NONLINEARITY vs. CODE, T_A = -40°C



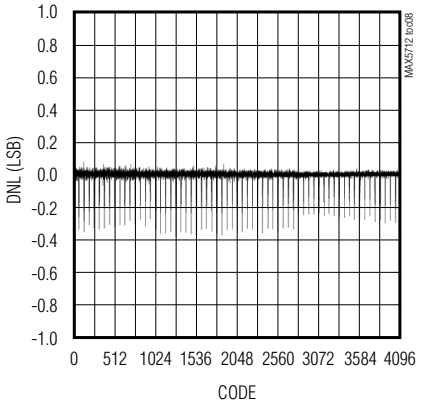
TOTAL UNADJUSTED ERROR vs. CODE, T_A = -40°C



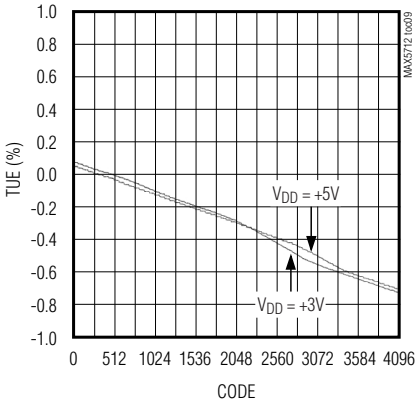
INTEGRAL NONLINEARITY vs. CODE, T_A = +125°C



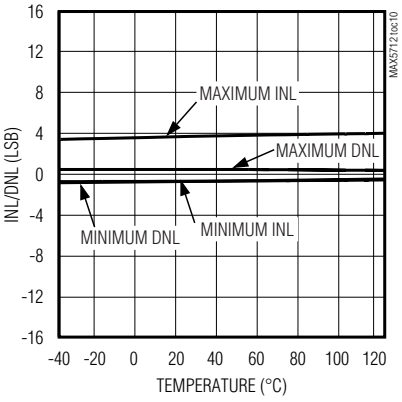
DIFFERENTIAL NONLINEARITY vs. CODE, T_A = +125°C



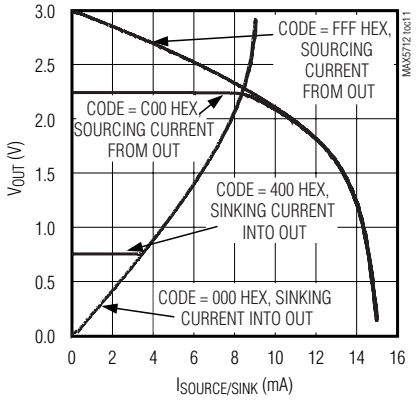
TOTAL UNADJUSTED ERROR vs. CODE, T_A = +125°C



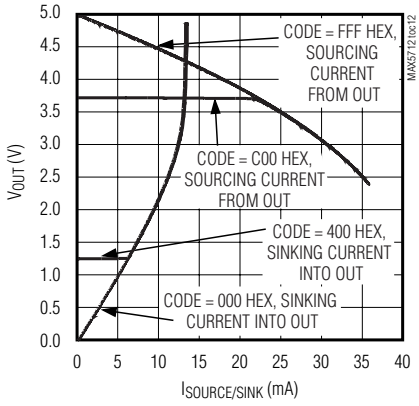
WORST CASE INL AND DNL vs. TEMPERATURE



SOURCE-AND-SINK CURRENT CAPABILITY (V_{DD} = +3V)



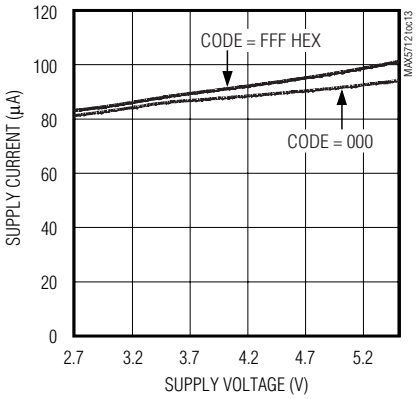
SOURCE-AND-SINK CURRENT CAPABILITY (V_{DD} = +5V)



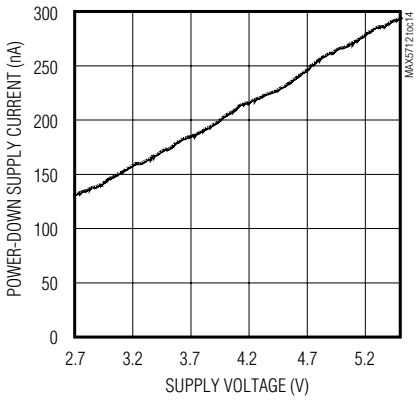
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

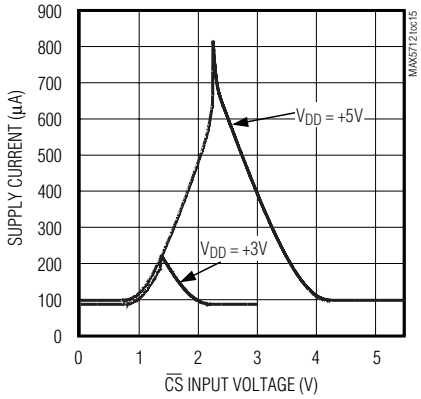
SUPPLY CURRENT vs. SUPPLY VOLTAGE



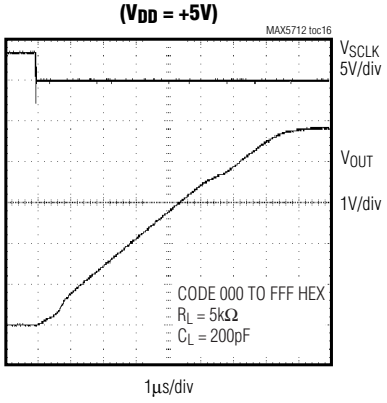
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



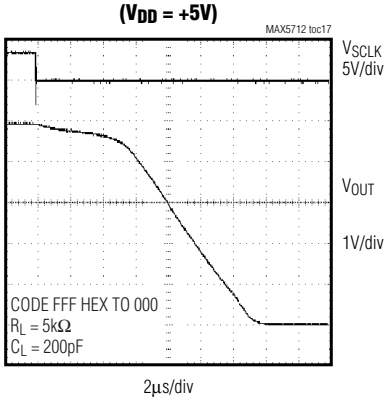
SUPPLY CURRENT vs. $\overline{CS}$ INPUT VOLTAGE



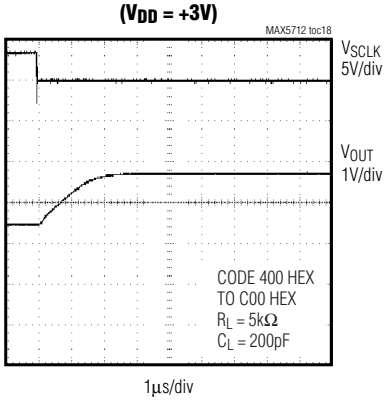
FULL-SCALE SETTLING TIME (V_{DD} = +5V)



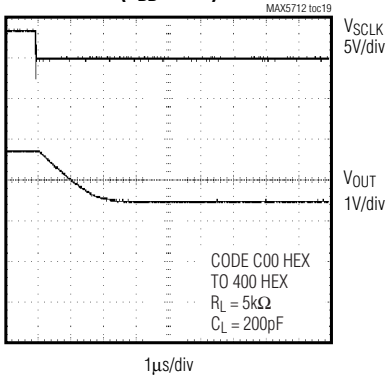
FULL-SCALE SETTLING TIME (V_{DD} = +5V)



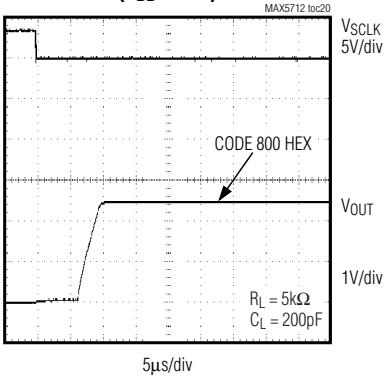
HALF-SCALE SETTLING TIME (V_{DD} = +3V)



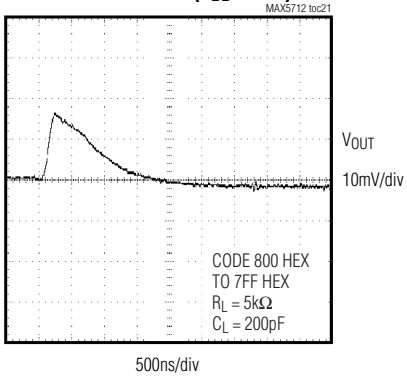
HALF-SCALE SETTLING TIME (V_{DD} = +3V)



EXITING POWER-DOWN (V_{DD} = +5V)



DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +5V)

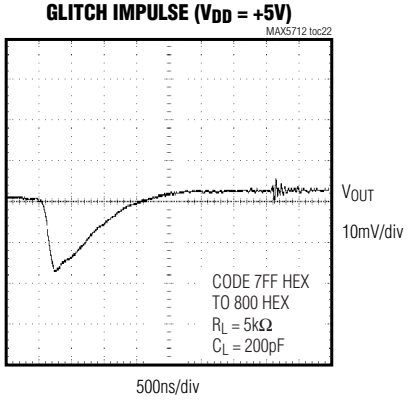


12-Bit, Low-Power, Rail-to-Rail Voltage-Output Serial DAC in SOT23

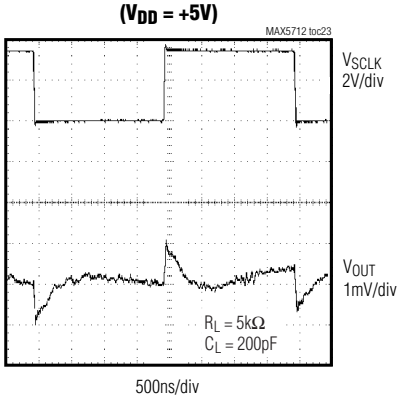
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +5V)



CLOCK FEEDTHROUGH (V_{DD} = +5V)



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power-Supply Input
2	GND	Ground
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	$\overline{CS}$	Active Low Chip-Select Input
6	OUT	DAC Output Voltage

Detailed Description

The MAX5712 voltage output, 12-bit DAC, offers a full 12-bit performance in a small 6-pin SOT23 package. The SOT23 footprint is less than 9mm^2. The MAX5712 has less than 1LSB differential nonlinearity error, ensuring monotonic performance. The device uses a simple 3-wire, SPI/QSPI/MICROWIRE and DSP-compatible serial interface that operates up to 20MHz. The MAX5712 incorporates three shutdown modes, making it ideal for low-power.

Analog Section

The MAX5712 consists of a resistor string, an output buffer, and a POR circuit. Monotonic digital to analog conversion is achieved using a resistor string architecture. Since V_{DD} is the reference for the MAX5712, the accuracy of the DAC depends on the accuracy of V_{DD}. The low bias current of the MAX5712 allows its power to be supplied by a voltage reference such as the MAX6030. The 12-bit DAC code is binary-unipolar with 1LSB = V_{DD}/4096.

Output Buffer

The DAC output buffer has a rail-to-rail output and is capable of driving a 5kΩ resistive load in parallel with a 200pF capacitive load. With a capacitive load of 200pF, the output buffer slews 0.5V/µs. With a 1/4FS to 3/4FS output transition, the amplifier output settles to 1/2LSB in less than 10µs when loaded with 5kΩ in parallel with 200pF. The buffer amplifier is stable with any combination of resistive loads greater than 5kΩ and capacitive loads less than 200pF.

Program the input register bits to power-down the device. The DAC registers are preserved during power-down and upon wake-up, the DAC output is restored to its pre-power-down voltage.

Power-On Reset

The MAX5712 has a POR circuit to set the DACs output to zero when V_{DD} is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system start-up, such as after a loss of power. Upon initial power-up, an internal power-on-reset circuit ensures that all DAC registers are cleared, the DAC is powered-down, and its output is terminated to GND by a 100kΩ resistor. An 8µs recovery time after issuing a wake-up command is needed before writing to the DAC registers.

Digital Section

3-Wire Serial Interface

The MAX5712 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE/DSP interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at DIN. Immediately following $\overline{CS}$ high-to-low transition, the data is shifted synchronously and latched into the input register on the falling edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial input register, it transfers its contents to the DAC latch. $\overline{CS}$ may then either be held low or brought high. $\overline{CS}$ must be brought high for a minimum of 80ns before the next write sequence, since a write sequence is initiated on a falling edge of $\overline{CS}$. Not keeping $\overline{CS}$ low during the first 15 SCLK cycles discards input data. The serial clock (SCLK) can idle either high or low between transitions. Figure 1 shows the complete 3-wire serial interface transmission. Table 1 lists serial-interface mapping.

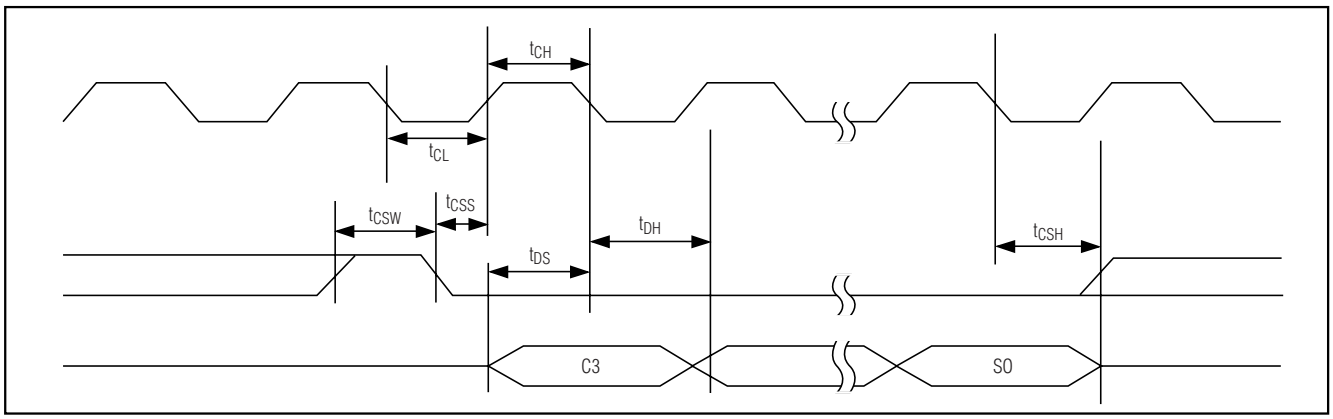


Figure 1. Timing Diagram

12-Bit, Low-Power, Rail-to-Rail Voltage-Output Serial DAC in SOT23

Table 1. Serial Interface Mapping

16-BIT SERIAL WORD																MODE	OUTPUT
MSB															LSB		
C3	C2	C1	C0	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00		
0	0	0	0	12-Bit DAC Code												Set and update DAC	$V_{OUT} = V_{DD} \times CODE/4096$
1	1	1	1	X	X	X	X	X	X	X	X	X	X	0	0	Wake-Up	Current DAC setting (initially 0)
1	1	1	1	X	X	X	X	X	X	X	X	X	X	0	1	Power-Down	Floating
1	1	1	1	X	X	X	X	X	X	X	X	X	X	1	0	Power-Down	1kΩ to GND
1	1	1	1	X	X	X	X	X	X	X	X	X	X	1	1	Power-Down	100kΩ to GND

Shutdown Modes

The MAX5712 includes three software-controlled shutdown modes that reduce the supply current to below 1µA. In two of the three shutdown modes, OUT is connected to GND through a resistor. Table 1 lists the three shutdown modes of operation.

Applications Information

Device Powered by an External Reference

The MAX5712 generates an output voltage proportional to V_{DD}, coupling power supply noise to the output. The circuit in Figure 2 rejects this power-supply noise by powering the device directly with a precision voltage reference, improving overall system accuracy. The MAX6030 (+3V, 75ppm) or the MAX6050 (+5V, 75ppm) precision voltage references are ideal choices due to the low-power requirements of the MAX5712. This solution is also useful when the required full-scale output voltage is less than the available supply voltages.

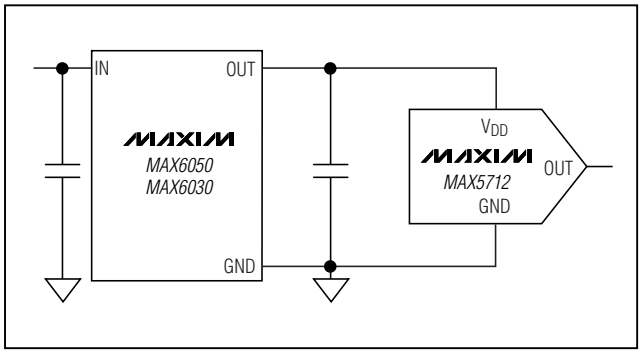


Figure 2. MAX5712 Powered By Reference

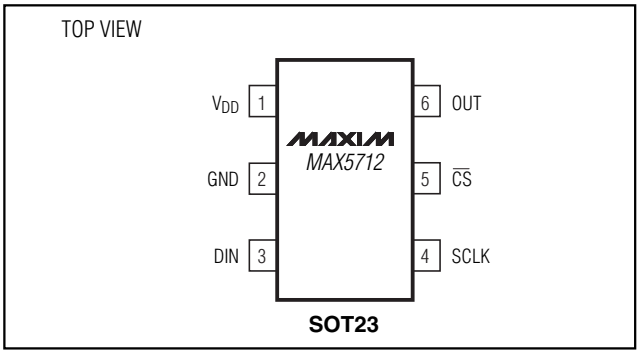
Digital Inputs and Interface Logic

The 3-wire digital interface for the MAX5712 is compatible with SPI, QSPI, MICROWIRE, and DSP. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input serially into the DAC. All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This allows optocouplers to interface directly to the MAX5712 without additional external logic. The digital inputs are compatible with CMOS-logic levels.

Power-Supply Bypassing and Layout

Careful PC board layout is important for optimal system performance. Keep analog and digital signals separate to reduce noise injection and digital feedthrough. Use a ground plane to ensure that the ground return from GND to the supply ground is short and low impedance. Bypass V_{DD} with a 0.1µF capacitor to ground as close as possible to the device.

Pin Configuration



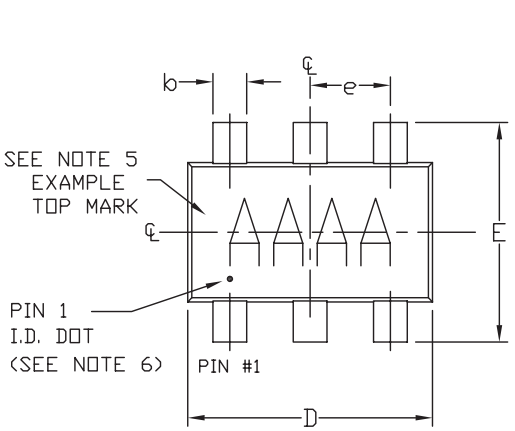
Chip Information

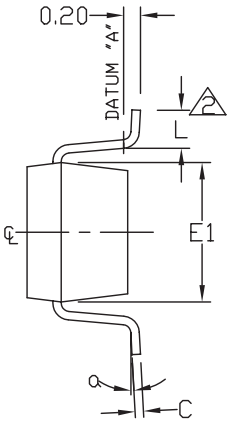
TRANSISTOR COUNT: 3856

PROCESS: BiCMOS

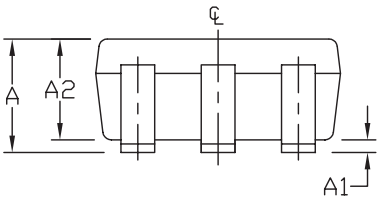
Package Information

6LSOT.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
a	0°	10°



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0058	E	1/1

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