19-3346; Rev 1; 9/05

4A, 20ns, MOSFET Driver

General Description

The MAX5078A/MAX5078B high-speed MOSFET drivers source and sink up to 4A peak current. These devices feature a fast 20ns propagation delay and 20ns rise and fall times while driving a 5000pF capacitive load. Propagation delay time is minimized and matched between the inverting and noninverting inputs. High sourcing/sinking peak currents, low propagation delay, and thermally enhanced packages make the MAX5078A/MAX5078B ideal for high-frequency and high-power circuits.

The MAX5078A/MAX5078B operate from a 4V to 15V single power supply and consume 40µA (typ) of supply current when not switching. These devices have an internal logic circuitry that prevents shoot-through during output state changes to minimize the operating current at a high switching frequency. The logic inputs are protected against voltage spikes up to +18V, regardless of the V_{DD} voltage. The MAX5078A has CMOS input logic levels while the MAX5078B has TTL-compatible input logic levels.

The MAX5078A/MAX5078B feature both inverting and noninverting inputs for greater flexibility in controlling the MOSFET. They are available in a 6-pin TDFN (3mm x 3mm) package and operate over the automotive temperature range of -40°C to +125°C.

Applications

Power MOSFET Switching
Switch-Mode Power Supplies
DC-DC Converters
Motor Control
Power-Supply Modules

Features

- ♦ 4V to 15V Single Power Supply
- ♦ 4A Peak Source/Sink Drive Current
- ♦ 20ns (typ) Propagation Delay
- ♦ Matching Delay Between Inverting and Noninverting Inputs
- ♦ V_{DD} / 2 CMOS (MAX5078A)/TTL (MAX5078B) Logic Inputs
- ♦ 0.1 x V_{DD} (CMOS) and 0.3V (TTL) Logic-Input Hysteresis
- ♦ Up to +18V Logic Inputs (Regardless of V_{DD} Voltage)
- ♦ Low Input Capacitance: 2.5pF (typ)
- ♦ 40µA (typ) Quiescent Current
- ♦ -40°C to +125°C Operating Temperature Range
- ♦ 6-Pin TDFN Package

Ordering Information

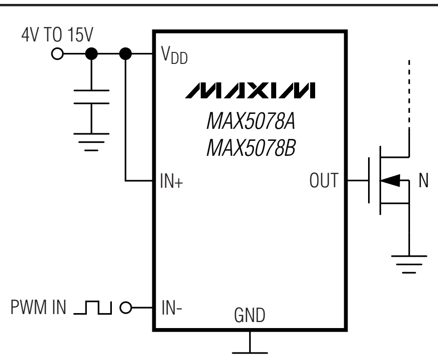
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX5078AATT	-40°C to +125°C	6 TDFN-EP*	AHL	T633-1
MAX5078BATT	-40°C to +125°C	6 TDFN-EP*	AHM	T633-1

*EP = Exposed pad.

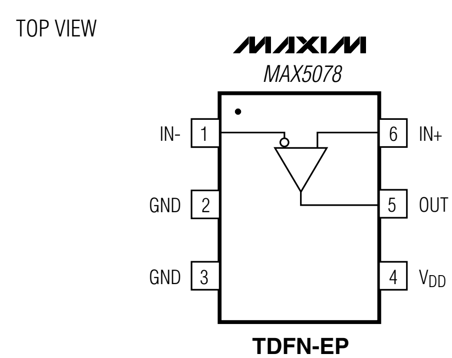
Selector Guide

PART	PIN-PACKAGE	LOGIC INPUT
MAX5078AATT	6 TDFN-EP	V_{DD} / 2 CMOS
MAX5078BATT	6 TDFN-EP	TTL

Typical Operating Circuit



Pin Configuration



4A, 20ns, MOSFET Driver

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{DD} ....-0.3V to +18V
IN+, IN- ....-0.3V to +18V
OUT ....-0.3V to (V_{DD} + 0.3V)
OUT Short-Circuit Duration....................10ms
Continuous Source/Sink Current at OUT_ (P_D < P_{DMAX}).....200mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN-EP (derate 18.2mW/°C above +70°C) 1454mW
Junction-to-Case Thermal Resistance (θ_{JC}) ....8.5°C/W
Operating Temperature Range....................-40°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature....................+150°C
Lead Temperature (soldering, 10s)....................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4V to 15V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 15V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
V_{DD} Operating Range	V_{DD}			4		15	V
V_{DD} Undervoltage Lockout	UVLO	V_{DD} rising		3.00	3.5	3.85	V
V_{DD} Undervoltage Lockout Hysteresis					200		mV
V_{DD} Undervoltage Lockout to Output Delay		V_{DD} rising			12		µs
V_{DD} Supply Current	I_{DD}	IN+ = 0V, IN- = V_{DD} (not switching)	V_{DD} = 4V		28	55	µA
			V_{DD} = 15V		40	75	
	I_{DD-SW}	Switching at 250kHz, C_L = 0		0.5	1.2	2.2	mA
DRIVER OUTPUT (SINK)							
Driver Output Resistance Pulling Down	R_{ON-N}	V_{DD} = 15V, I_{OUT} = -100mA	T_A = +25°C		1.1	1.8	Ω
			T_A = +125°C		1.5	2.4	
		V_{DD} = 4.5V, I_{OUT} = -100mA	T_A = +25°C		2.2	3.3	
			T_A = +125°C		3.0	4.5	
Peak Output Current (Sinking)	I_{PK-N}	V_{DD} = 15V, C_L = 10,000pF			4		A
Output-Voltage Low		I_{OUT} = -100mA	V_{DD} = 4.5V			0.45	V
			V_{DD} = 15V			0.24	
Latchup Protection	I_{LUP}	Reverse current I_{OUT} (Note 2)		400			mA
DRIVER OUTPUT (SOURCE)							
Driver Output Resistance Pulling Up	R_{ON-P}	V_{DD} = 15V, I_{OUT} = 100mA	T_A = +25°C		1.5	2.1	Ω
			T_A = +125°C		1.9	2.75	
		V_{DD} = 4.5V, I_{OUT} = 100mA	T_A = +25°C		2.75	4	
			T_A = +125°C		3.75	5.5	
Peak Output Current (Sourcing)	I_{PK-P}	V_{DD} = 15V, C_L = 10,000pF			4		A

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 4V to 15V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 15V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output-Voltage High		I_{OUT} = 100mA	V_{DD} = 4.5V	V_{DD} - 0.55			V
			V_{DD} = 15V	V_{DD} - 0.275			
LOGIC INPUT (Note 3)							
Logic 1 Input Voltage	V_{IH}	MAX5078A		0.7 x V_{DD}			V
		MAX5078B (Note 4)		2.1			
Logic 0 Input Voltage	V_{IL}	MAX5078A				0.3 x V_{DD}	V
		MAX5078B				0.8	
Logic-Input Hysteresis	V_{HYS}	MAX5078A			0.1 x V_{DD}		V
		MAX5078B			0.3		
Logic-Input-Current Leakage		IN+ = IN- = 0V or V_{DD}		-1	+0.1	+1	µA
Input Capacitance	C_{IN}				2.5		pF
SWITCHING CHARACTERISTICS FOR V_{DD} = 15V (Figure 1)							
OUT Rise Time	t_R	C_L = 1000pF			4		ns
		C_L = 5000pF			18		
		C_L = 10,000pF			32		
OUT Fall Time	t_F	C_L = 1000pF			4		ns
		C_L = 5000pF			15		
		C_L = 10,000pF			26		
Turn-On Delay Time	t_{D-ON}	C_L = 10,000pF (Note 2)		10	20	34	ns
Turn-Off Delay Time	t_{D-OFF}	C_L = 10,000pF (Note 2)		10	20	34	ns
SWITCHING CHARACTERISTICS FOR V_{DD} = 4.5V (Figure 1)							
OUT Rise Time	t_R	C_L = 1000pF			7		ns
		C_L = 5000pF			37		
		C_L = 10,000pF			85		
OUT Fall Time	t_F	C_L = 1000pF			7		ns
		C_L = 5000pF			30		
		C_L = 10,000pF			75		
Turn-On Delay Time	t_{D-ON}	C_L = 10,000pF (Note 2)		18	35	70	ns
Turn-Off Delay Time	t_{D-OFF}	C_L = 10,000pF (Note 2)		18	35	70	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 4V to 15V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 15V and T_A = +25°C.) (Note 1)

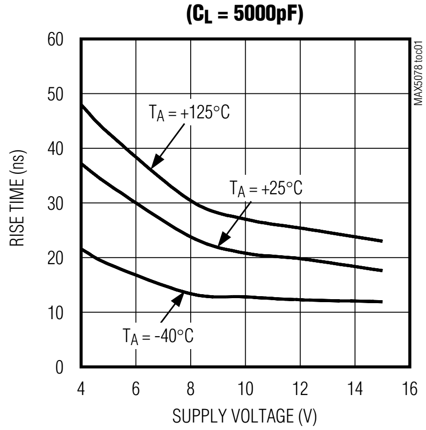
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MATCHING CHARACTERISTICS						
Mismatch Propagation Delays from Inverting and Noninverting Inputs to Output	Δt_{ON-OFF}	V_{DD} = 15V, C_L = 10,000pF		2		ns
		V_{DD} = 4.5V, C_L = 10,000pF		4		

Note 1: All devices are 100% tested at T_A = +25°C. Specifications over -40°C to +125°C are guaranteed by design.
Note 2: Limits are guaranteed by design, not production tested.
Note 3: The logic-input thresholds are tested at V_{DD} = 4V and V_{DD} = 15V.
Note 4: TTL compatible with reduced noise immunity.

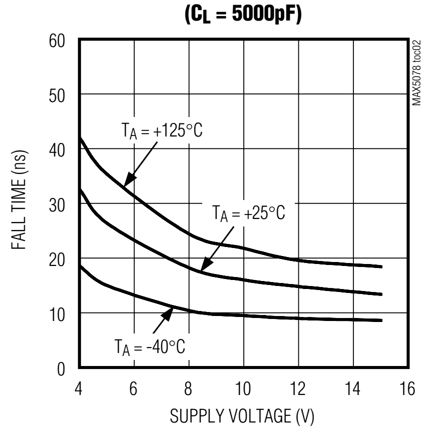
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

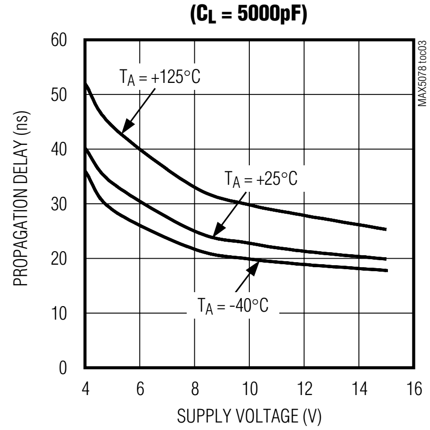
RISE TIME vs. SUPPLY VOLTAGE (C_L = 5000pF)



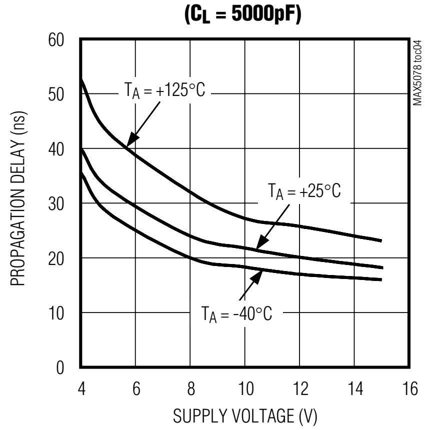
FALL TIME vs. SUPPLY VOLTAGE (C_L = 5000pF)



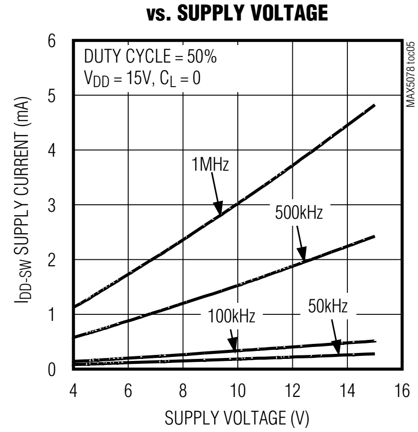
PROPAGATION DELAY TIME, LOW-TO-HIGH vs. SUPPLY VOLTAGE (C_L = 5000pF)



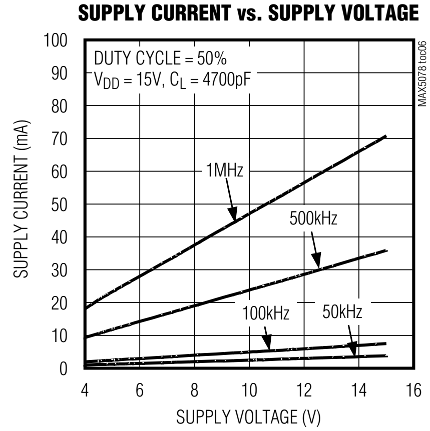
PROPAGATION DELAY TIME, HIGH-TO-LOW vs. SUPPLY VOLTAGE (C_L = 5000pF)



I_{DD-SW} SUPPLY CURRENT vs. SUPPLY VOLTAGE



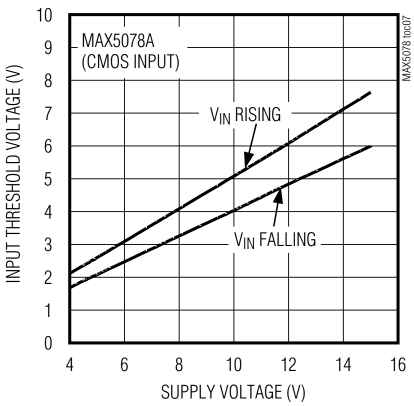
SUPPLY CURRENT vs. SUPPLY VOLTAGE



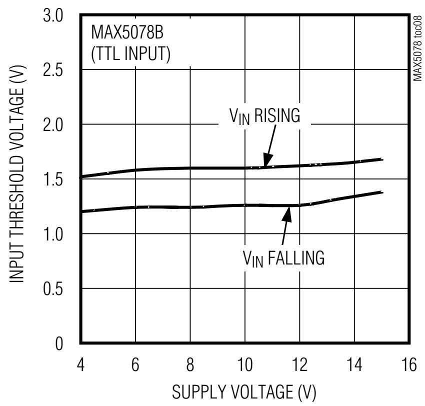
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

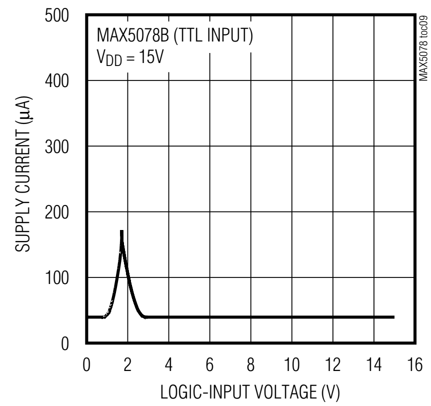
INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



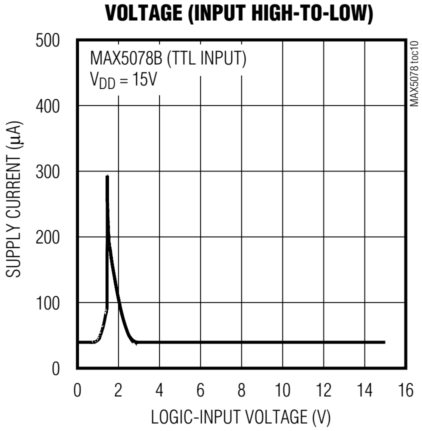
INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



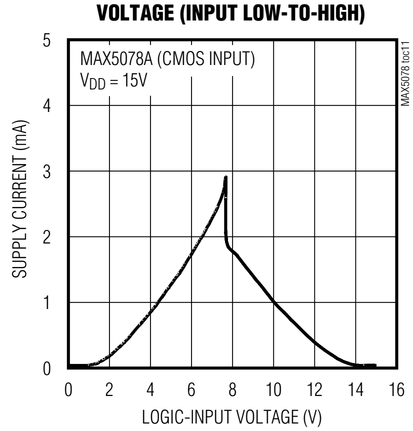
SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT LOW-TO-HIGH)



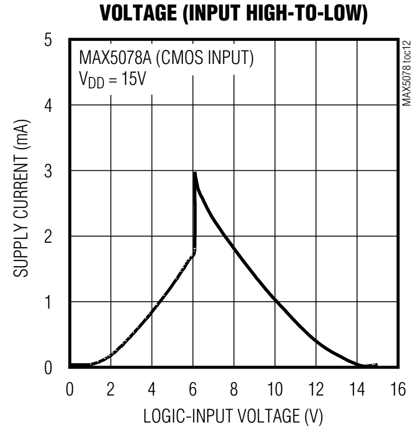
SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT HIGH-TO-LOW)



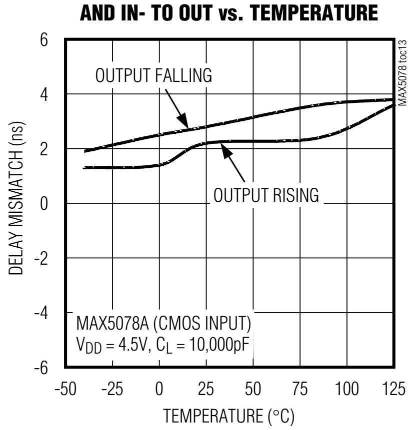
SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT LOW-TO-HIGH)



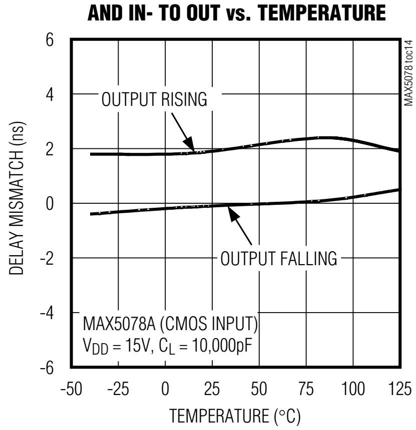
SUPPLY CURRENT vs. LOGIC-INPUT VOLTAGE (INPUT HIGH-TO-LOW)



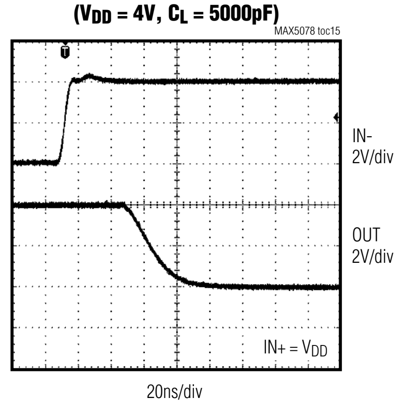
DELAY MISMATCH BETWEEN IN+ AND IN- TO OUT vs. TEMPERATURE



DELAY MISMATCH BETWEEN IN+ AND IN- TO OUT vs. TEMPERATURE



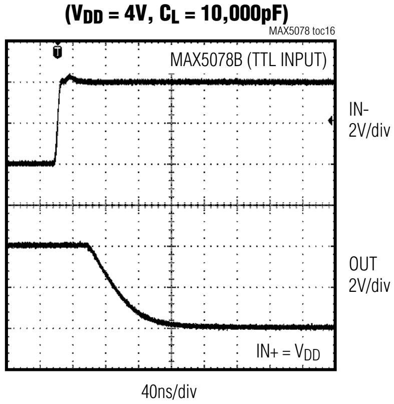
LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE (V_{DD} = 4V, C_L = 5000pF)



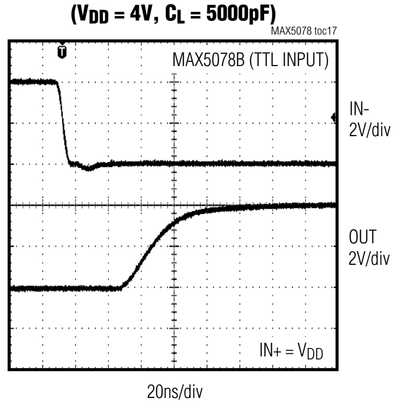
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

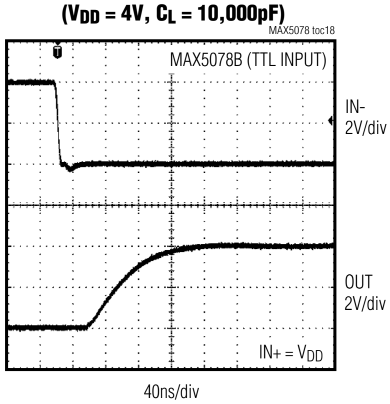
LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE (V_{DD} = 4V, C_L = 10,000pF)



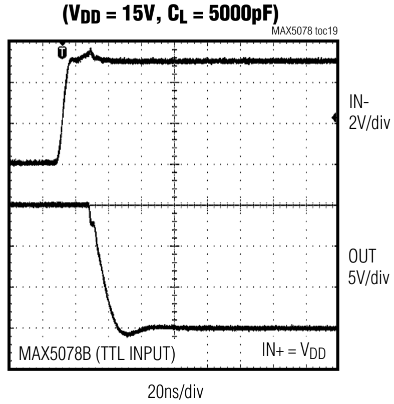
LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE (V_{DD} = 4V, C_L = 5000pF)



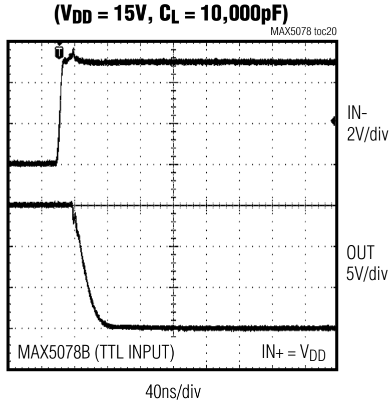
LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE (V_{DD} = 4V, C_L = 10,000pF)



LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE (V_{DD} = 15V, C_L = 5000pF)

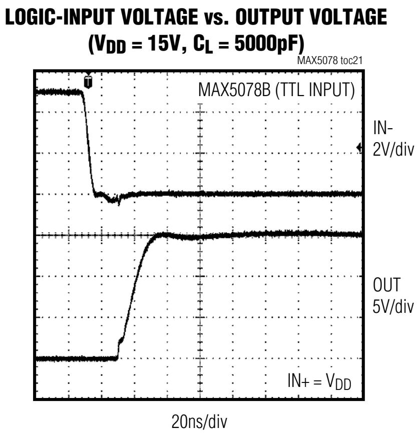


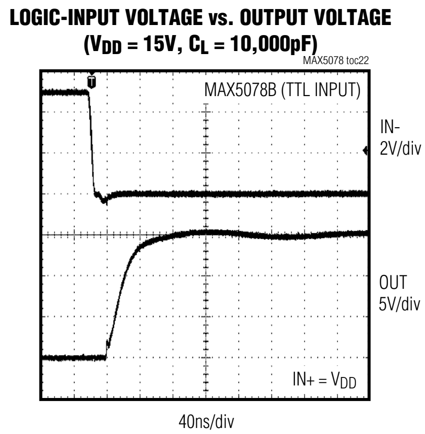
LOGIC-INPUT VOLTAGE vs. OUTPUT VOLTAGE (V_{DD} = 15V, C_L = 10,000pF)

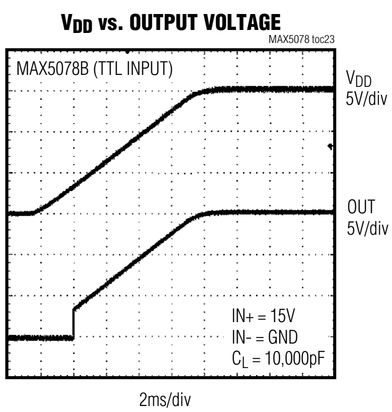


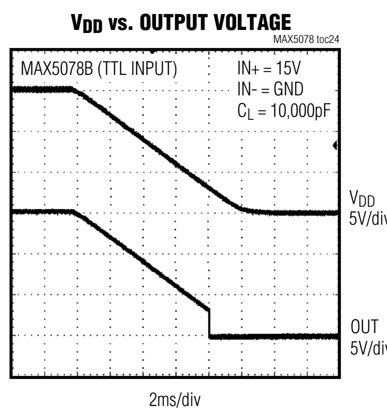
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)









Pin Description

PIN	NAME	FUNCTION
1	IN-	Inverting Logic-Input Terminal. Connect to GND when not used.
2, 3	GND	Ground
4	V_{DD}	Power Supply. Bypass to GND with one or more 0.1µF ceramic capacitors.
5	OUT	Driver Output. Sources or sinks current to turn the external MOSFET on or off.
6	IN+	Noninverting Logic-Input Terminal. Connect to V_{DD} when not used.
—	EP	Exposed Pad. Internally connected to GND. Do not use the exposed pad as the only electrical ground connection.

Detailed Description

V_{DD} Undervoltage Lockout (UVLO)

The MAX5078A/MAX5078B have internal undervoltage lockout (UVLO) for V_{DD}. When V_{DD} is below the UVLO threshold, OUT is pulled low independent of the state of the inputs. The undervoltage lockout is typically 3.5V with 200mV typical hysteresis to avoid chattering. When V_{DD} rises above the UVLO threshold, the output goes high or low depending upon the logic-input levels. Bypass V_{DD} using a low-ESR ceramic capacitor for proper operation (see the *Applications Information* section).

Logic Inputs

The MAX5078A has CMOS logic inputs while the MAX5078B has TTL-compatible logic inputs. The logic inputs are protected against the voltage spikes up to 18V, regardless of the V_{DD} voltage. The TTL and CMOS logic inputs have 300mV and 0.1 x V_{DD} hysteresis, respectively, to avoid double pulsing during transition. The low 2.5pF input capacitance reduces loading and increases switching speed.

The logic inputs are high impedance and must not be left floating. If the inputs are left open, OUT can go to an undefined state as soon as V_{DD} rises above the UVLO threshold. Therefore, the PWM output from the controller must assume proper state when powering up the device.

The MAX5078A/MAX5078B have two logic inputs, providing greater flexibility in controlling the MOSFET. Use IN+ for noninverting logic and IN- for inverting logic operation. Connect IN+ to V_{DD} and IN- to GND, if not used. Alternatively, the unused input can be used as an ON/OFF function. Use IN+ for active-low shutdown logic and IN- for active-high shutdown logic (see Figure 3). See Table 1 for all possible input combinations.

Driver Output

The MAX5078A/MAX5078B have low $R_{DS(ON)}$ p-channel and n-channel devices (totem pole) in the output stage for the fast turn-on/turn-off, high-gate-charge switching MOSFETs. The peak source or sink current is typically 4A. The output voltage (V_{OUT}) is approximately equal to V_{DD} when in high state and is ground when in low state. The driver $R_{DS(ON)}$ is lower at higher V_{DD} resulting in higher source-/sink-current capability and faster switching speeds. The propagation delays from the noninverting and inverting logic inputs to OUT are matched to 2ns typically. The break-before-make logic avoids any cross-conduction between the internal p- and n-channel devices, and eliminates shoot-through, thus reducing the quiescent supply current.

Applications Information

RLC Series Circuit

The driver's $R_{DS(ON)}$ (R_{ON}), internal bond/lead inductance (L_P), trace inductance (L_S), gate inductance (L_G), and gate capacitance (C_G) form a series RLC circuit with a second-order characteristic equation. The series RLC circuit has an undamped natural frequency (ϖ_0) and a damping ratio (ζ) where:

$$\varpi_0 = \frac{1}{\sqrt{(L_P + L_S + L_G) \times C_G}}$$

$$\xi = \frac{R_{ON}}{2 \times \sqrt{\frac{(L_P + L_S + L_G)}{C_G}}}$$

The damping ratio needs to be greater than 0.5 (ideally 1) to avoid ringing. Add a small resistor (R_{GATE}) in series with the gate when driving a very low gate-charge MOSFET, or when the driver is placed away from the MOSFET.

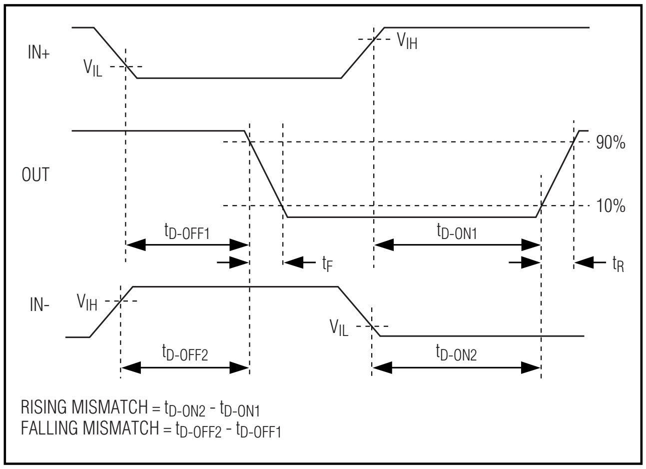


Figure 1. Timing Diagram

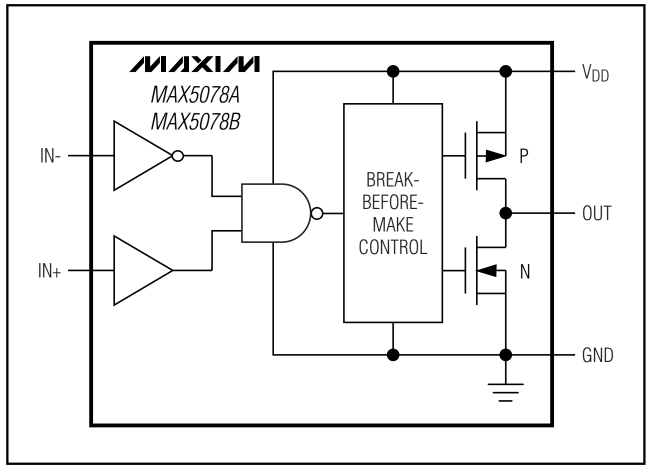


Figure 2. MAX5054 Simplified Diagram (1 Driver)

Use the following equation to calculate the series resistor:

$$R_{GATE} \geq \sqrt{\frac{(L_P + L_S + L_G)}{C_G}} - R_{ON}$$

L_P can be approximated as 2nH for the TDFN package. L_S is on the order of 20nH/in. Verify L_G with the MOSFET vendor.

Supply Bypassing and Grounding

Pay extra attention to bypassing and grounding the MAX5078A/MAX5078B. Peak supply and output currents may exceed 4A when driving large external capacitive loads. Supply voltage drops and ground shifts create negative feedback for inverters and may degrade the delay and transition times. Ground shifts due to poor device grounding may also disturb other circuits sharing the same AC ground return path. Any series inductance in the V_{DD}, OUT, and/or GND paths can cause oscillations due to the very high di/dt when switching the MAX5078A/MAX5078B with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass V_{DD} to GND. Use a ground plane to minimize ground return resistance and series inductance. Place the external MOSFET as close as possible to the MAX5078A/MAX5078B to further minimize board inductance and AC path impedance.

Power Dissipation

Power dissipation of the MAX5078A/MAX5078B consists of three components: caused by the quiescent current, capacitive charge/discharge of internal nodes, and the output current (either capacitive or resistive load). Maintain the sum of these components below the maximum power dissipation limit.

The current required to charge and discharge the internal nodes is frequency dependent (see the I_{DD-SW} Supply Current vs. Supply Voltage graph in the *Typical Operating Characteristics*). The power dissipation (P_Q) due to the quiescent switching supply current (I_{DD-SW}) can be calculated as:

$$P_Q = V_{DD} \times I_{DD-SW}$$

For capacitive loads, use the following equation to estimate the power dissipation:

$$P_{CLOAD} = C_{LOAD} \times (V_{DD})^2 \times f_{SW}$$

where C_{LOAD} is the capacitive load, V_{DD} is the supply voltage, and f_{SW} is the switching frequency.

Calculate the total power dissipation (P_T) as follows:

$$P_T = P_Q + P_{CLOAD}$$

Use the following equations to estimate the MAX5078A/MA5078B total power dissipation when driving a ground-referenced resistive load:

$$P_T = P_Q + P_{RLOAD}$$

$$P_{RLOAD} = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where D is the fraction of the period the MAX5078A/MA5078B's output pulls high, $R_{ON(MAX)}$ is the maximum on-resistance of the device with the output high, and I_{LOAD} is the output load current of the MAX5078A/MAX5078B.

Layout Information

The MAX5078A/MAX5078B MOSFET drivers source and sink large currents to create very fast rising and falling edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Table 1. MAX5078 Truth Table

IN+	IN-	OUT
Low	Low	Low
Low	High	Low
High	Low	High
High	High	Low

Use the following PC board layout guidelines when designing with the MAX5078A/MAX5078B:

- Place one or more 0.1µF decoupling ceramic capacitors from V_{DD} to GND as close to the device as possible. Connect V_{DD} and GND to large copper areas. Place one bulk capacitor of 10µF (min) on the PC board with a low resistance path to the V_{DD} input and GND of the MAX5078A/MAX5078B.
- Two AC current loops form between the device and the gate of the driven MOSFET. The MOSFET looks like a large capacitance from gate to source when the gate pulls low. The active current loop is from the MOSFET gate to OUT of the MAX5078A/MAX5078B, to GND of the MAX5078A/MAX5078B, and to the source of the MOSFET. When the gate of the MOSFET pulls high, the active current is from the V_{DD} terminal of the decoupling capacitor, to V_{DD} of the MAX5078A/MAX5078B, to OUT of the MAX5078A/MAX5078B, to the MOSFET gate, to the MOSFET source, and to the negative terminal of the decoupling capacitor. Both charging current and discharging current loops are important. Minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close to the MOSFET as possible.
- In a multilayer PC board, the inner layers should consist of a GND plane containing the discharging and charging current loops.
- Pay extra attention to the ground loop and use a low-impedance source when using a TTL logic-input device. Fast fall time at OUT may corrupt the input during transition.

Exposed Pad

The TDFN-EP package has an exposed pad on the bottom of its package. This pad is internally connected to GND. For the best thermal conductivity, solder the exposed pad to the ground plane in order to dissipate 1.9W. Do not use the ground-connected pad as the only electrical ground connection or ground return. Use GND (pins 2 and 3) as the primary electrical ground connection.

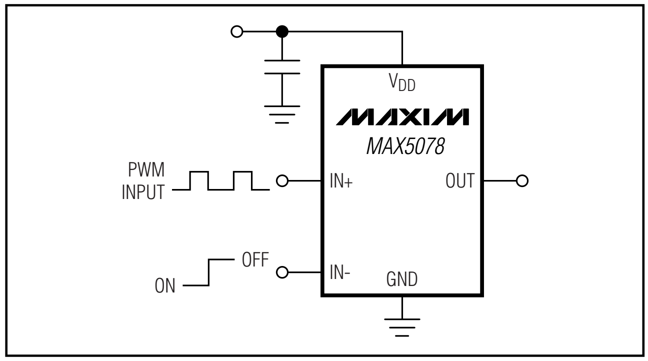


Figure 3. Unused Input as an ON/OFF Function

Additional Application Circuits

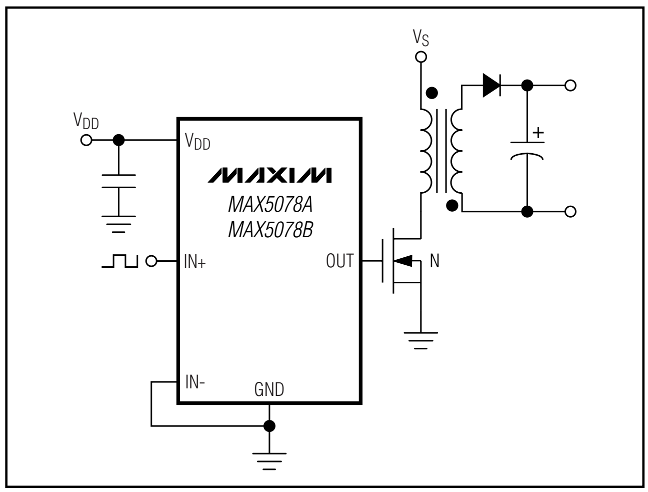


Figure 4. Noninverting Application

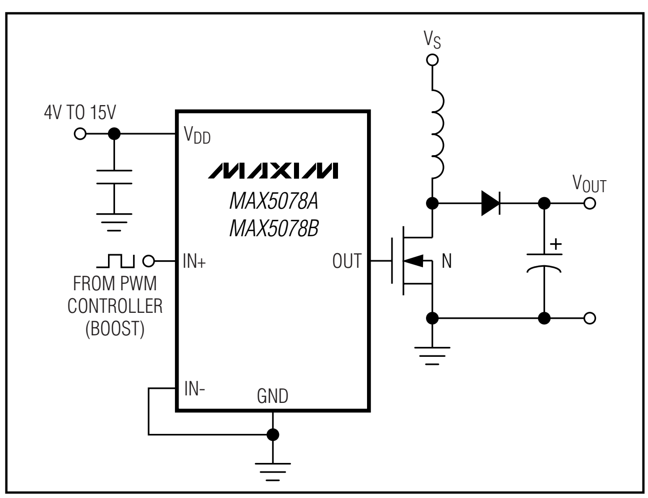


Figure 5. Boost Converter

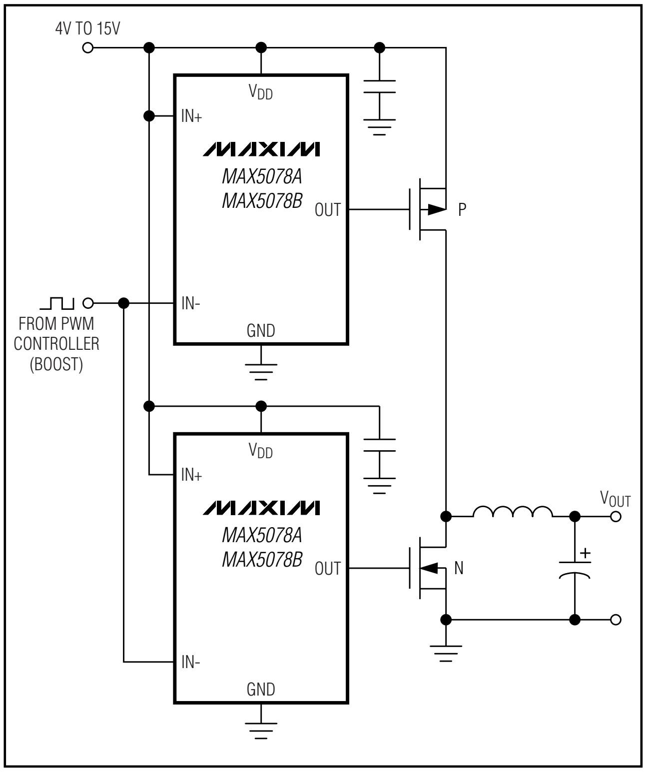


Figure 6. MAX5078A/MAX5078B In High-Power Synchronous Buck Converter

Chip Information

TRANSISTOR COUNT: 258

PROCESS: CMOS

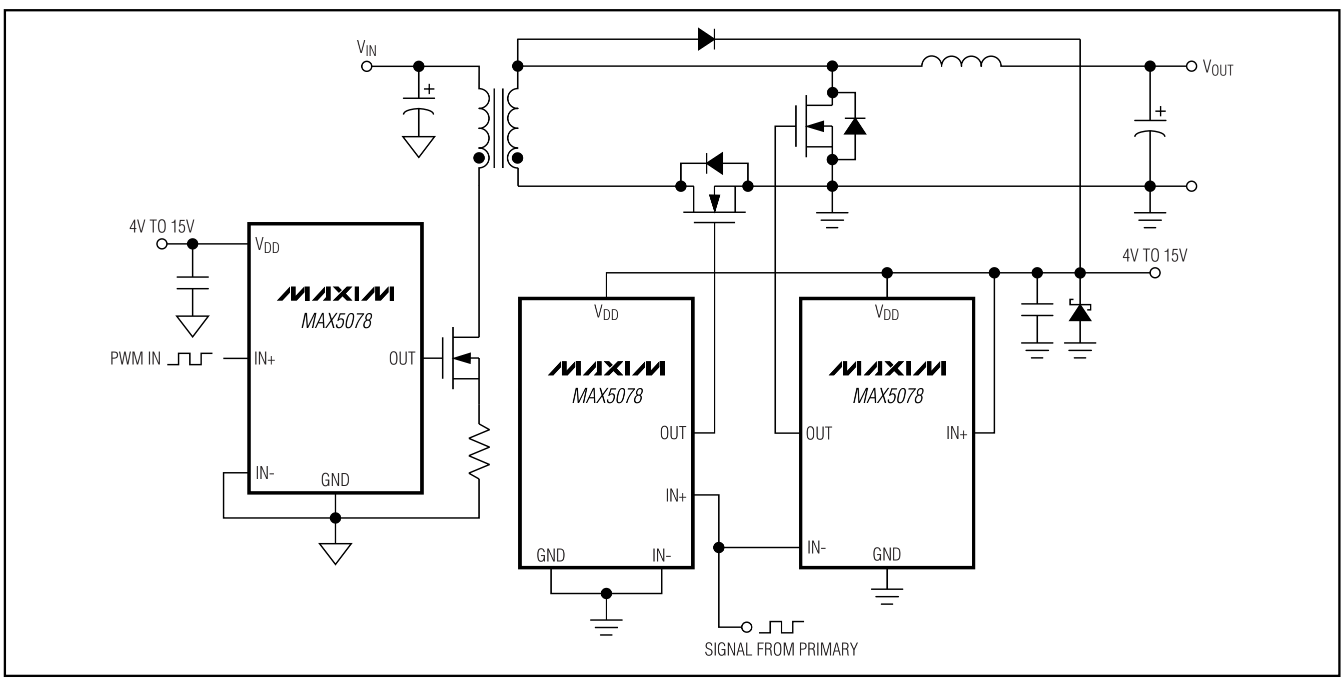
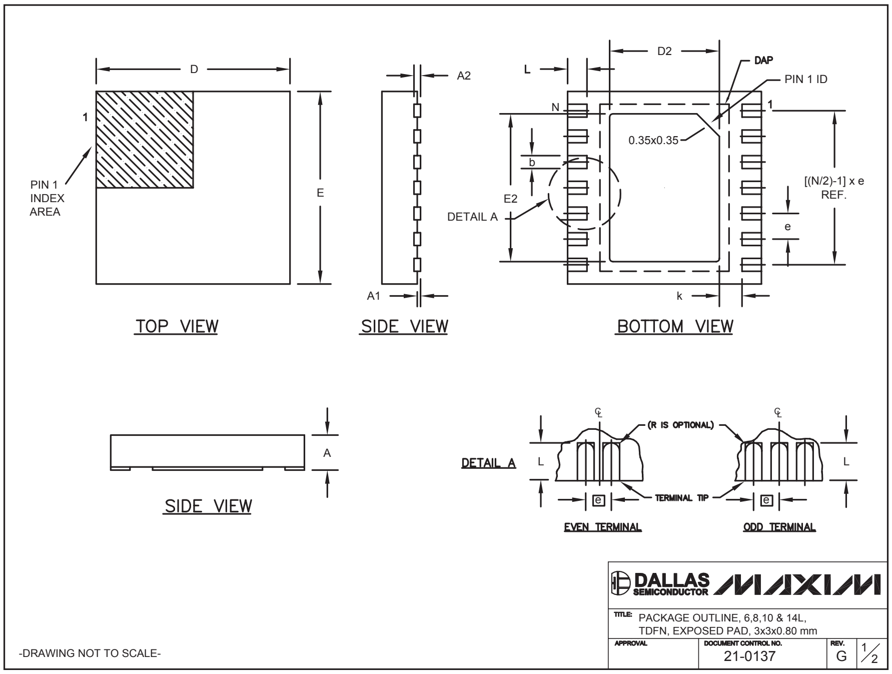


Figure 7. Forward Converter with Secondary-Side Synchronous Rectification

4A, 20ns, MOSFET Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



6, 8, &10L, DFN THIN.EPS

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS

PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. G | 2/2

-DRAWING NOT TO SCALE-

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