



0.75Ω, Dual SPDT Audio Switch with Integrated Comparators

MAX4855

General Description

The MAX4855 dual, single-pole/double-throw (SPDT) switch operates from a single +2V to +5.5V supply and features rail-to-rail signal handling. The MAX4855 has low on-resistance (0.75Ω) with a +3V supply making it ideal for audio switching applications in portable devices. The device also integrates two internal comparators that can be used for headphone detection or mute/send key functions.

The MAX4855 is available in the space-saving (3mm x 3mm), 16-pin thin QFN package and operates over the extended temperature range of -40°C to +85°C.

Applications

Speaker Headset Switching
 Audio-Signal Routing
 Cellular Phones
 Notebook Computers
 PDAs and Other Handheld Devices

Features

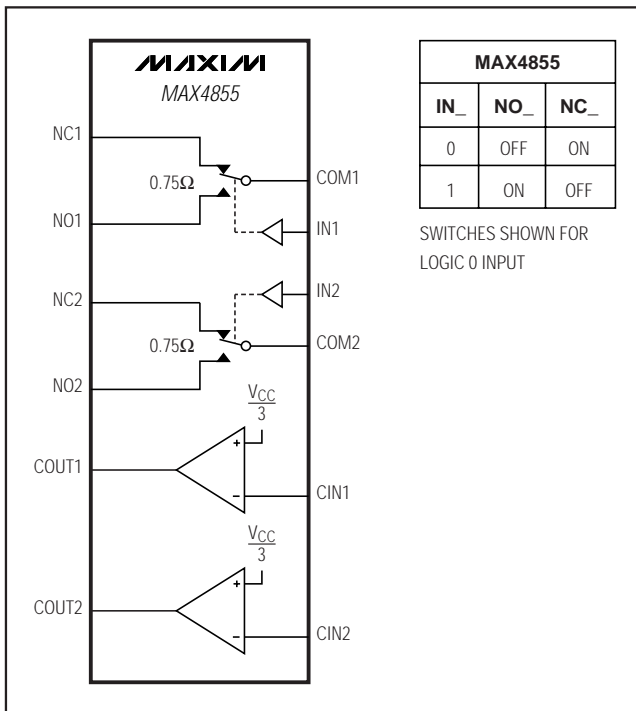
- ◆ **Audio Signal Routing**
- ◆ **0.75Ω On-Resistance**
- ◆ **0.18Ω On-Resistance Flatness**
- ◆ **0.07Ω Channel-to-Channel Matching**
- ◆ **Rail-to-Rail Signal Handling**
- ◆ **2 Integrated Comparators**
- ◆ **1.8V Logic Compatible**
- ◆ **2V to 5.5V Supply Range**
- ◆ **Available in a Space-Saving (3mm x 3mm), 16-Pin TQFN Package**

Ordering Information

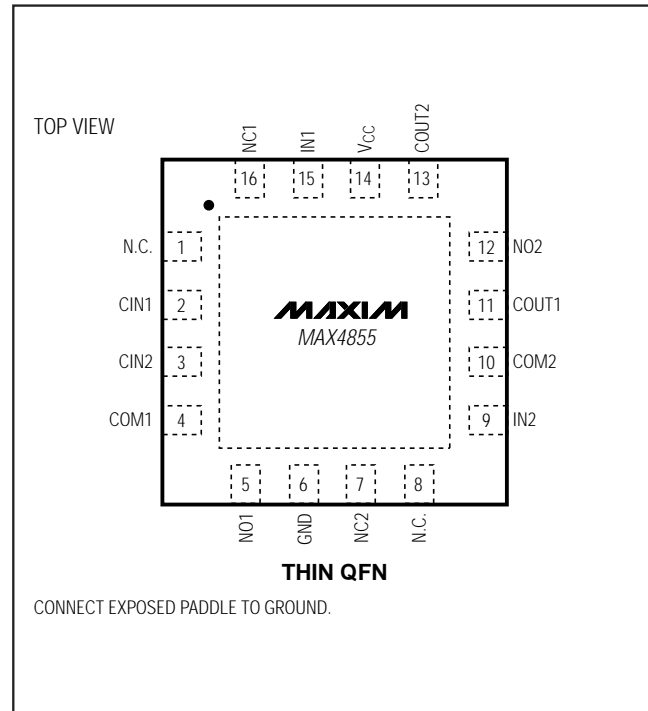
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4855ETE	-40°C to +85°C	16 TQFN-EP*	ABY

*EP = Exposed paddle.

Block Diagram/Truth Table



Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V _{CC} , IN ₋ , CIN ₋ to GND	-0.3V to +6.0V
NO ₋ , NC ₋ , COM ₋ , COUT ₋ (Note 1)	-0.3V to (V _{CC} + 0.3V)
COUT ₋ Continuous Current	±20mA
Closed Switch Continuous Current COM ₋ , NO ₋ , NC ₋	±300mA
Peak Current COM ₋ , NO ₋ , NC ₋ (pulsed at 1ms, 50% duty cycle)	±400mA
Peak Current COM ₋ , NO ₋ , NC ₋ (pulsed at 1ms, 10% duty cycle)	±500mA

Continuous Power Dissipation (T _A = +70°C) 16-Pin Thin QFN (derate 20.8mW/°C above +70°C)	1667mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO, NC, or COM exceeding V_{CC} or GND are clamped by internal diodes. Signals on IN exceeding GND are clamped by an internal diode. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V _{CC}		2		5.5	V
Supply Current	I _{CC}	V _{CC} = 5.5V, V _{IN-} = 0V or V _{CC}		5	10	μA
ANALOG SWITCH						
Analog Signal Range	V _{NO-} , V _{NC-} , V _{COM-}		0		V _{CC}	V
On-Resistance (Note 3)	R _{ON}	V _{CC} = 2.7V, I _{COM-} = 100mA, V _{NC-} or V _{NO-} = 0V to V _{CC}	T _A = +25°C	0.75	1	Ω
			T _A = -40°C to +85°C		1.1	
On-Resistance Match Between Channels (Notes 3, 4)	ΔR _{ON}	V _{CC} = 2.7V, I _{COM-} = 100mA, V _{NC-} or V _{NO-} = 1.5V	T _A = +25°C	0.075	0.120	Ω
			T _A = -40°C to +85°C		0.135	
On-Resistance Flatness (Note 5)	R _{FLAT}	V _{CC} = 2.7V, I _{COM-} = 100mA, V _{NC-} or V _{NO-} = 0.75V, 1.5V, 1.75V	T _A = +25°C	0.18	0.275	Ω
			T _A = -40°C to +85°C		0.3	
NO ₋ /NC ₋ Off-Leakage Current (Note 2)	I _{OFF}	V _{CC} = 5.5V, V _{NC-} or V _{NO-} = 1V or 4.5V, V _{COM-} = 4.5V or 1V	T _A = +25°C	-2	+2	nA
			T _A = -40°C to +85°C	-10	+10	
COM ₋ On-Leakage Current (Note 2)	I _{ON}	V _{CC} = 5.5V; V _{NC-} or V _{NO-} = 1V, 4.5V, or floating; V _{COM-} = 1V, 4.5V, or floating	T _A = +25°C	-2	+2	nA
			T _A = -40°C to +85°C	-15	+15	
DYNAMIC CHARACTERISTICS						
Turn-On Time	t _{ON}	V _{CC} = 2.7V, V _{NO-} or V _{NC-} = 1.5V, R _L = 300Ω, C _L = 50pF (Figure 1)	T _A = +25°C	40	60	ns
			T _A = -40°C to +85°C		100	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	$V_{CC} = 2.7V$, $V_{NO_}$ or $V_{NC_} = 1.5V$, $R_L = 300\Omega$, $C_L = 50pF$ (Figure 1)	$T_A = +25^{\circ}C$	30	40	ns
			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		60	
Break-Before-Make Time Delay (Note 3)	t_D	$V_{CC} = 2.7V$, $V_{NO_}$ or $V_{NC_} = 1.5V$, $R_L = 50\Omega$, $C_L = 50pF$ (Figure 2)	$T_A = +25^{\circ}C$	15		ns
			$T_A = -40^{\circ}C$ to $+85^{\circ}C$	2		
Charge Injection	Q	$V_{COM_} = 1.5V$, $R_S = 0\Omega$, $C_L = 1.0nF$ (Figure 3)		170		pC
Off-Isolation (Note 6)		$f = 100kHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 4)		-75		dB
Crosstalk	V_{CT}	$f = 100kHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 4)		-93		dB
-3dB Bandwidth	BW	Signal = 0dBm, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 4)		38		MHz
Total Harmonic Distortion	THD	$f = 20Hz$ to $20kHz$, $V_{COM_} = 1V + 2V_{P-P}$, $R_L = 32\Omega$		0.07		%
NO_/NC_ Off-Capacitance	C_{OFF}	$f = 1MHz$ (Figure 5)		50		pF
COM On-Capacitance	C_{ON}	$f = 1MHz$ (Figure 5)		150		pF
DIGITAL I/O (IN_)						
Input-Logic High Voltage	V_{IH}	$V_{CC} = 2V$ to $3.6V$	1.4			V
		$V_{CC} = 3.6V$ to $5.5V$	1.8			
Input-Logic Low Voltage	V_{IL}	$V_{CC} = 2V$ to $3.6V$			0.5	V
		$V_{CC} = 3.6V$ to $5.5V$			0.8	
Input Leakage Current	I_{IN}	$V_{IN_} = 0$ or $5.5V$	-0.5		+0.5	μA
COMPARATOR						
Comparator Range			0		5.5	V
Comparator Threshold		$V_{CC} = 2V$ to $5.5V$, falling input	$0.3 \times V_{CC}$	$0.33 \times V_{CC}$	$0.36 \times V_{CC}$	V
Comparator Hysteresis		$V_{CC} = 2V$ to $5.5V$		50		mV
Comparator Output High Voltage		$I_{SOURCE} = 1mA$	$V_{CC} - 0.4V$			V
Comparator Output Low Voltage		$I_{SINK} = 1mA$			0.4	V
Comparator Switching Time		Rising input (Figure 6)		2.5		μs
		Falling input (Figure 6)		0.5		

Note 2: Specifications are 100% tested at $T_A = +85^{\circ}C$ only, and guaranteed by design and characterization over the specified temperature range.

Note 3: Guaranteed by design and characterization; not production tested.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

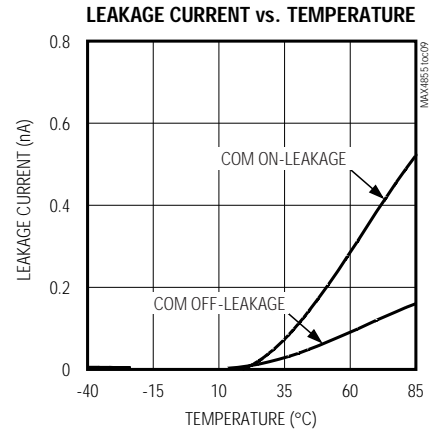
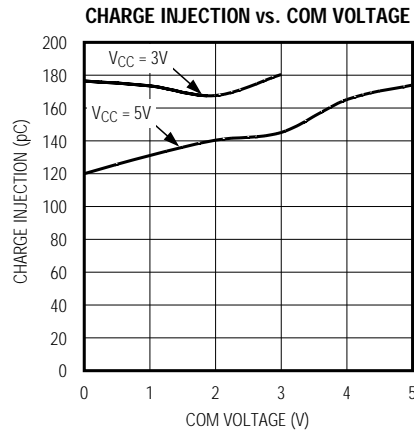
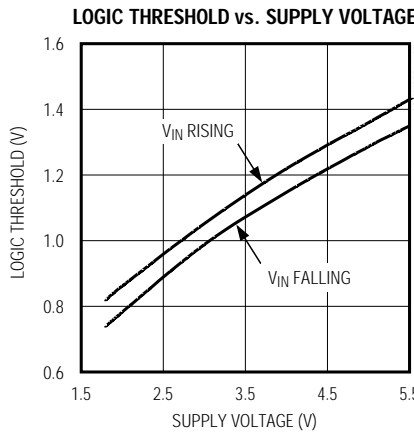
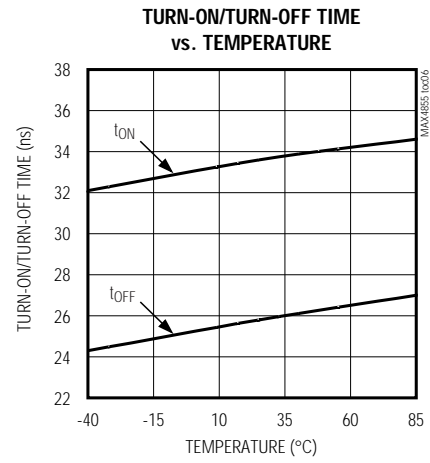
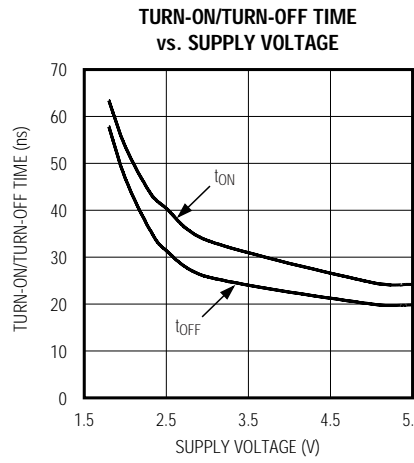
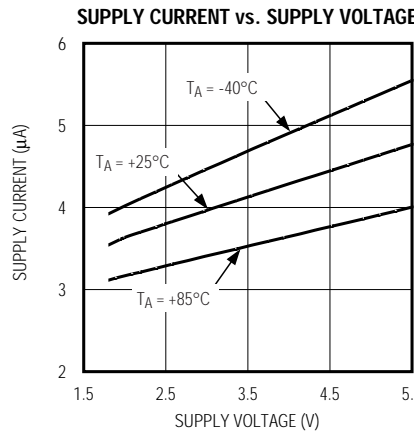
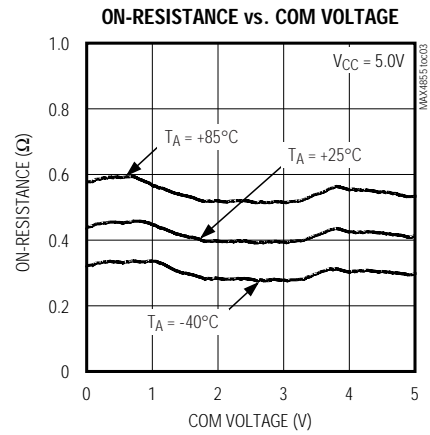
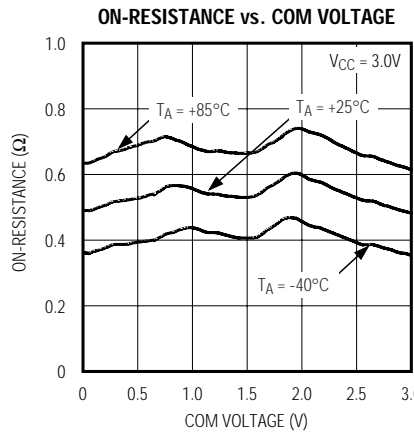
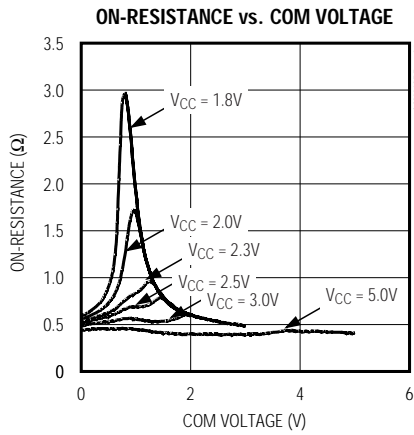
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 6: Off-Isolation = $20\log_{10}(V_{COM_} / V_{NO_})$, $V_{COM_}$ = output, $V_{NO_}$ = input to off switch.

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Typical Operating Characteristics

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

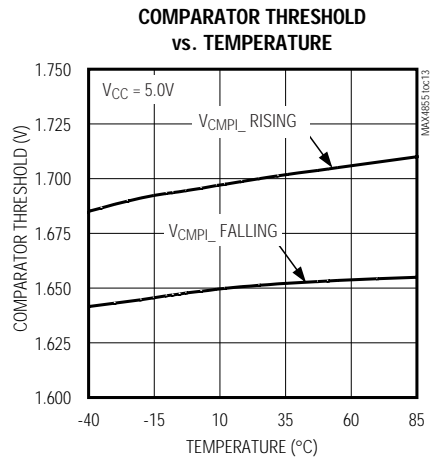
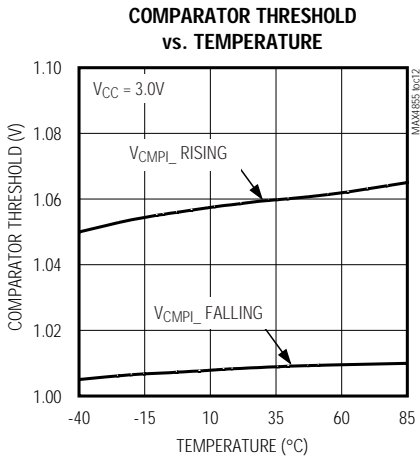
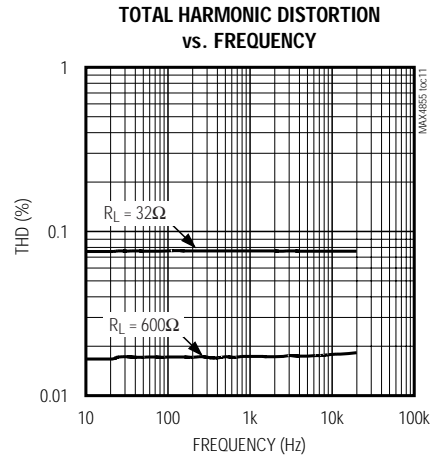
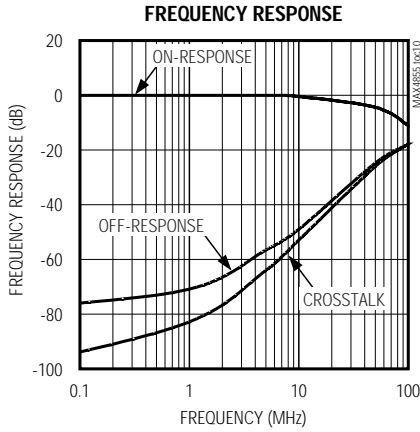


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Typical Operating Characteristics (continued)

($V_{CC} = 3.0V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	NAME	FUNCTION
1, 8	N.C.	No Connection. Not internally connected.
2	CIN1	Inverting Input for Comparator 1
3	CIN2	Inverting Input for Comparator 2
4	COM1	Common Terminal for Analog Switch 1
5	NO1	Normally Open Terminal for Analog Switch 1
6	GND	Ground
7	NC2	Normally Closed Terminal for Analog Switch 2
9	IN2	Digital Control Input for Analog Switch 2. A logic LOW on IN2 connects COM2 to NC2 and a logic HIGH connects COM2 to NO2.
10	COM2	Common Terminal for Analog Switch 2
11	COU1	Output for Comparator 1
12	NO2	Normally Open Terminal for Analog Switch 2
13	COU2	Output for Comparator 2
14	V _{CC}	Supply Voltage. Bypass to GND with a 0.01μF capacitor as close to the pin as possible.
15	IN1	Digital Control Input for Analog Switch 1. A logic LOW on IN1 connects COM1 to NC1 and a logic HIGH connects COM1 to NO1.
16	NC1	Normally Closed Terminal for Analog Switch 1
EP	—	Exposed Paddle. Connect to PC board ground plane.

Detailed Description

The MAX4855 dual SPDT, low on-resistance, low-voltage, analog switch operates from a +2V to +5.5V supply and can handle signals up to the power rails. In addition, the MAX4855 integrates two internal comparators that can be used for headphone or mute detection. The comparator threshold is internally generated to be approximately 1/3 of V_{CC}.

Applications Information

Digital Control Inputs

The logic inputs (IN_n) accept up to +5.5V even if the supply voltages are below this level. For example, with a +3.3V V_{CC} supply, IN_n can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving IN_n rail-to-rail minimizes power consumption. For a +2V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 1.8V (high).

Analog Signal Levels

The on-resistance of these switches changes very little for analog input signals across the entire supply voltage range (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_n, NC_n, and COM_n pins can be either inputs or outputs.

Comparator

The positive terminal of the comparator is internally set to V_{CC}/3. When the negative terminal (CIN_n) is below the threshold (V_{CC}/3), the comparator output (COU_n) is high. When CIN_n rises above V_{CC}/3, COU_n is low.

The comparator threshold allows for detection of headphones since headphone audio signals are typically biased to V_{CC}/2.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current-limited.

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Test Circuits/Timing Diagrams

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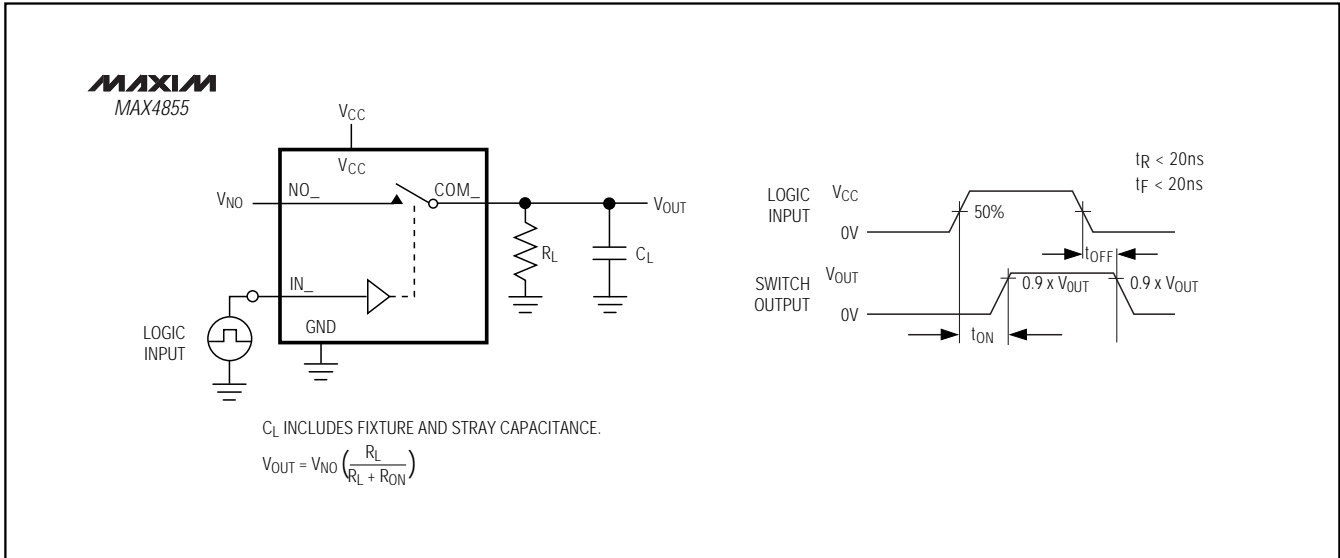


Figure 1. Switching Time

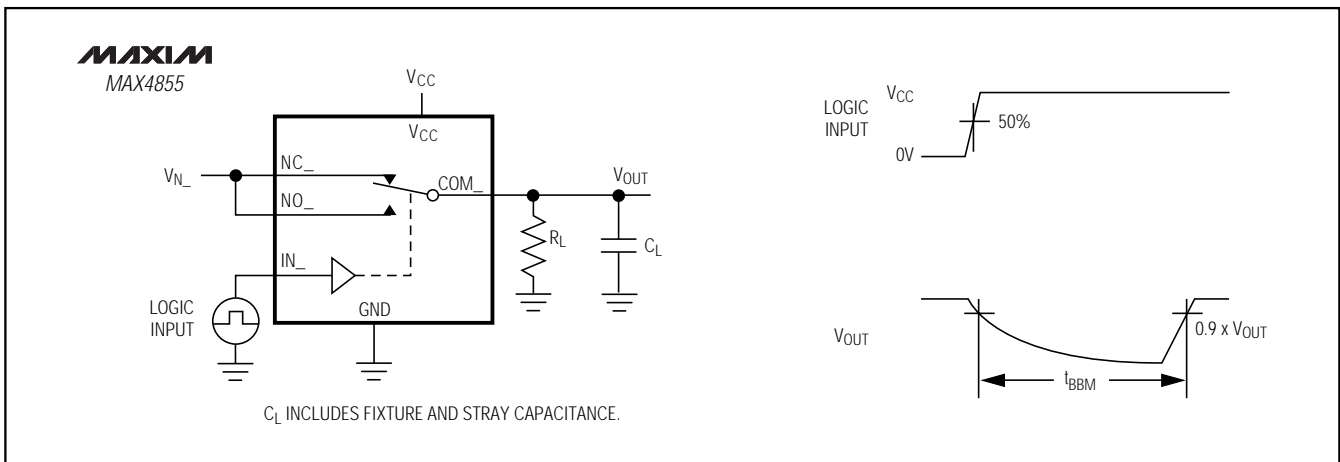


Figure 2. Break-Before-Make Interval

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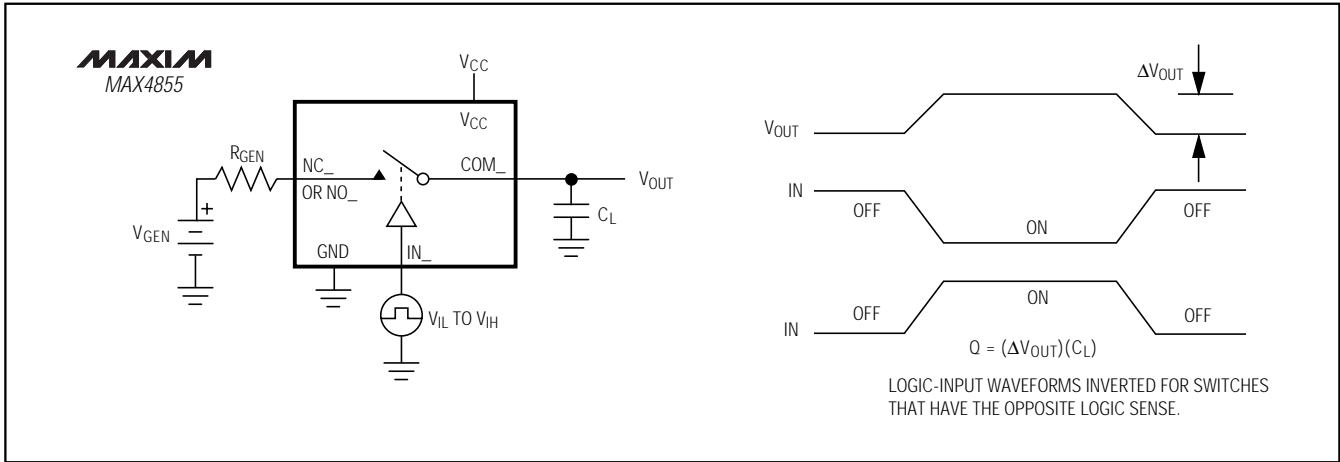


Figure 3. Charge Injection

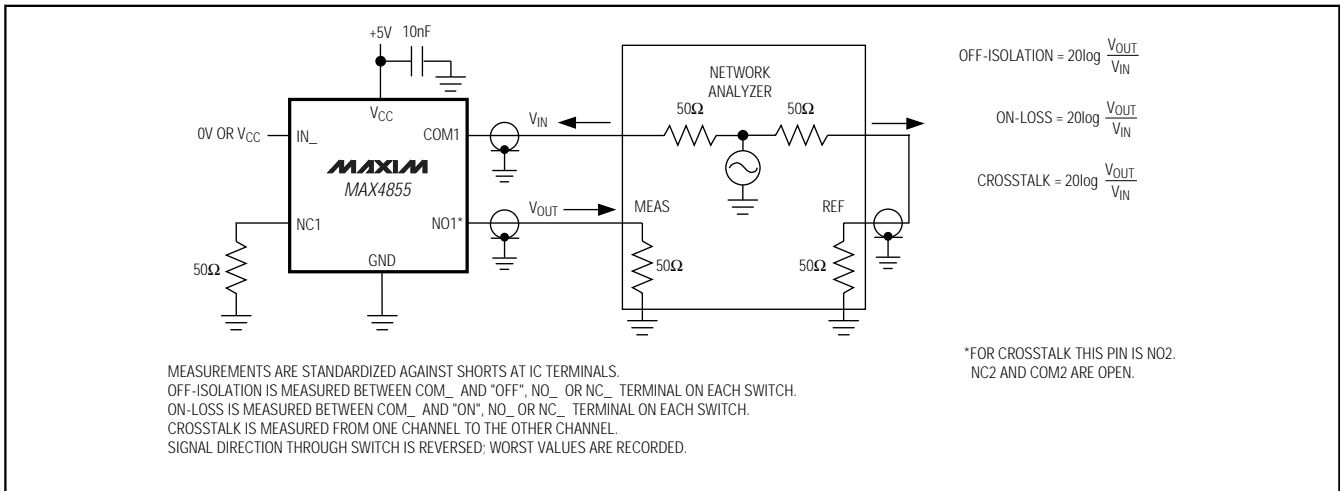


Figure 4. On-Loss, Off-Isolation, and Crosstalk

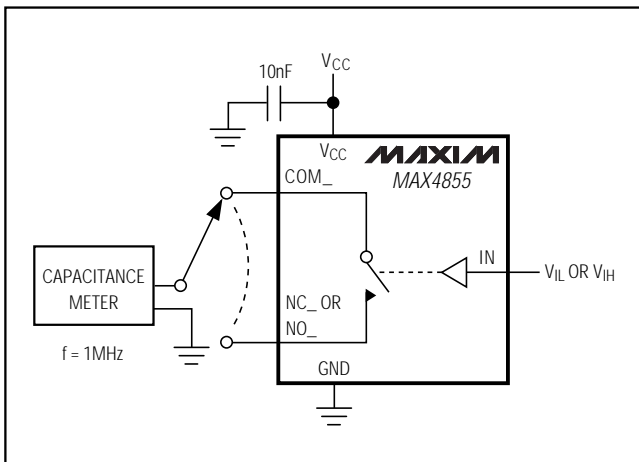


Figure 5. Channel Off-/On-Capacitance

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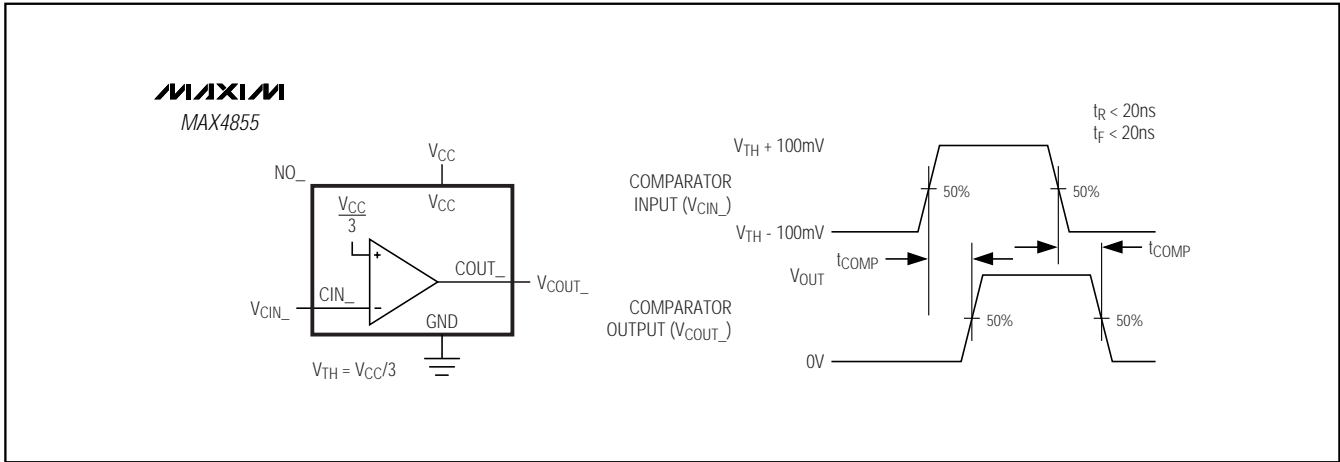
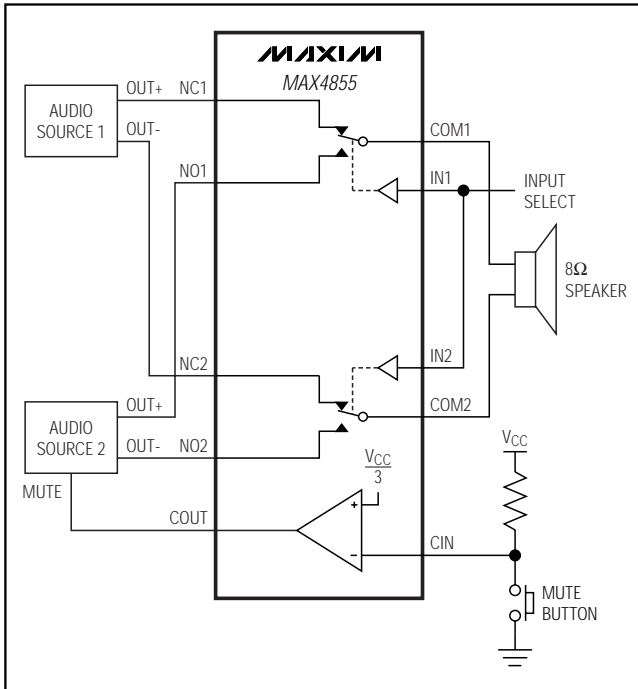


Figure 6. Comparator Switching Time

Typical Operating Circuit



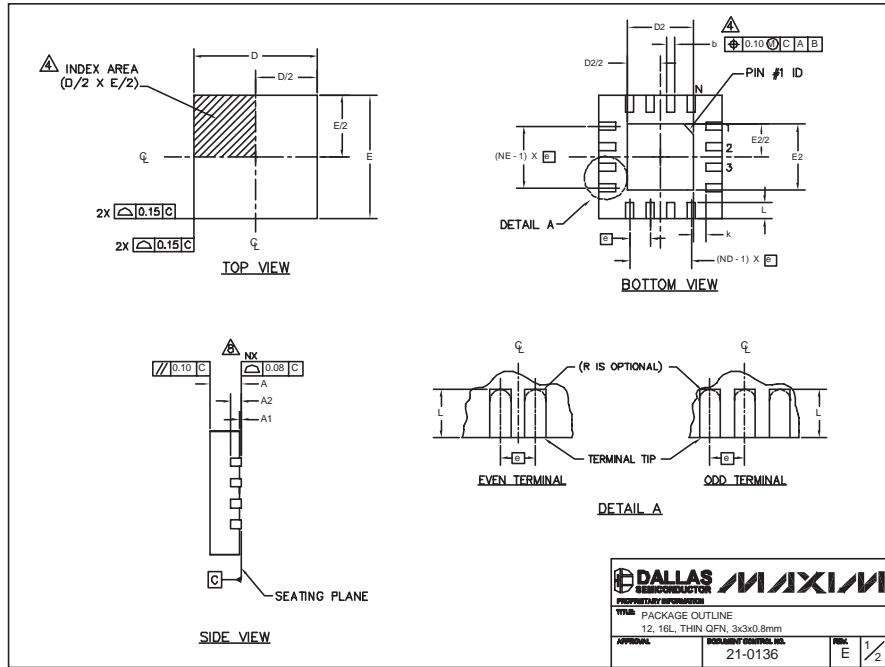
Chip Information

TRANSISTOR COUNT: 735
PROCESS: CMOS

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



12X16L OFN THINLEPS

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

PKG CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.85	0.80	0.85	0.85	0.80	0.85	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220 REVISION C.

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