19-1670; Rev 0; 4/00

MAXIM

Integrated GPS Receiver and Synthesizer

General Description

The MAX2740 is a complete global positioning system (GPS) receiver from antenna output to digitizer input. The signal path includes the LNA, two downconverters, and variable-gain and fixed-gain amplifiers. By utilizing a double-conversion superheterodyne architecture with external surface acoustic wave (SAW) filters, high levels of image rejection and blocking immunity are possible. Receiver linearity has been maximized to improve operation in hostile RFI environments found in cellular base stations. The MAX2740 also includes a high-performance voltage-controlled oscillator (VCO) with low phase noise for subcentimeter carrier phase applications, and a fixed-frequency synthesizer for generation of all required on-chip local oscillators.

The unique frequency plan captured in the MAX2740 is suitable for joint GPS/GLONASS receivers with minimal external components. This allows the MAX2740 to provide a cost-effective and high-performance solution for navigation and timing products that need maximum satellite availability.

The MAX2740 is compatible with a high-performance DSP engine capable of very fast time to first fix and excellent multipath rejection.

Applications

Base Station Timing

E911 Location Assistance

GPS Automotive and Consumer Receivers

Wireless Local-Loop Timing

Joint GPS/GLONASS Receivers

High-Precision Timing for SDH Networks

High-Positional-Accuracy Surveying Equipment

Features

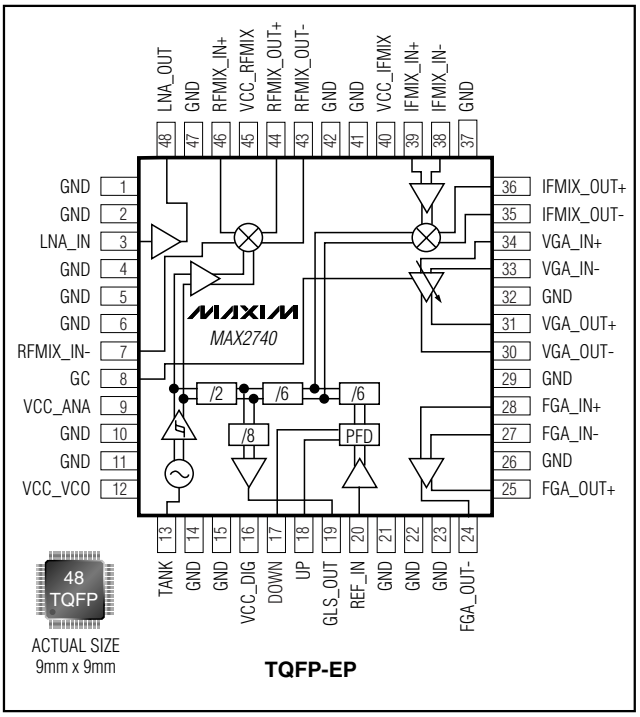
- ♦ **High Selectivity for Hostile Base Station Environments**
- ♦ **Complete Antenna-to-Baseband Receiver Solution**
- ♦ **>100dB Total Receiver Gain Including All Filter Losses**
- ♦ **>50dB Automatic Gain Control (AGC) Range**
- ♦ **Fully Balanced Topology for Minimum Spurious Responses**
- ♦ **Low Phase Noise VCO for Carrier Phase Applications**
- ♦ **Compatible with High-Performance Companion DSP**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2740ECM	-40°C to +85°C	48 TQFP-EP*

**Exposed paddle*

Pin Configuration/ Functional Diagram



For free samples and the latest literature, visit www.maxim-ic.com or phone 1-800-998-8800. For small orders, phone 1-800-835-8769.

ABSOLUTE MAXIMUM RATINGS

V_{CC} Pins to GND .....-0.3V to +4.3V
RF LNA Input Power .....+10dBm
LO Input Power.....+10dBm
GC Input Voltage .....-0.3 to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +85°C)
48-Pin TQFP-EP Package 800mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.3V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Supply Current			55.1	84.3	mA
AGC Voltage Range			0.5 to 2.5		V
AGC Current		-50		+25	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2740 EV kit, V_{CC} = +3.0V, 50Ω system impedance, F_{RF} = 1575.42MHz, F_{IF1} = 135.42MHz, F_{IF2} = 15.42MHz, F_{REF} = 20MHz at 600mVpp, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LNA					
LNA Gain	(Note 1)	13.1	16.0	17.2	dB
LNA Gain Variation Over Temperature	Relative to ambient (Note 1)	-1.3	±0.5	+1.0	dB
LNA Input Third-Order Intercept Point	(Note 2)		-9.4		dBm
LNA Noise Figure			2.6		dB
RF MIXER (Z_I = 100Ω differential)					
RF Mixer Conversion Gain	(Note 3)		22.6		dB
RF Mixer Input IP3			-22.4		dBm
RF Mixer Noise Figure (SSB)			11.0		dB
IF MIXER (Z_S = 100Ω differential, Z_I = 4kΩ differential)					
IF Mixer Conversion Gain			36.3		dB
VARIABLE-GAIN AMPLIFIER (VGA) (Z_I = 4kΩ differential)					
VGA Voltage Gain at Maximum Gain Setting	GC = 2.5V		15.1		dB
VGA Voltage Gain at Minimum Gain Setting	GC = 0.5V		-54.7		dB
FIXED GAIN AMPLIFIER (FGA)					
FGA Voltage Gain	Z_I = 4kΩ differential		39.8		dB
FGA 1dB Compression (Output)			2.05		Vp-p

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2740 EV kit, V_{CC} = +3.0V, 50Ω system impedance, F_{RF} = 1575.42MHz, F_{IF1} = 135.42MHz, F_{IF2} = 15.42MHz, F_{REF} = 20MHz at 600mVpp, T_A = +25°C, unless otherwise noted.)

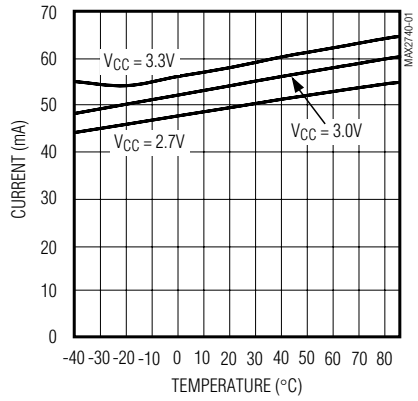
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE-CONTROLLED OSCILLATOR (VCO) (100kHz offset)					
Synthesizer VCO Phase Noise			-91.5		dBc/Hz
Output Frequency for External GLONASS Tuner			90		MHz
Magnitude GLS_OUT	R_l = 500Ω, C_l = 10pF		300		mVp-p
PFD Swing on Up and Down Outputs	Mag (UP-DOWN)		250		mV

Note 1: Guaranteed by design and characterization.
Note 2: Two tones at pin = -35dBm per tone, f1 = 1575MHz, f2 = 1576MHz.
Note 3: Two tones at pin = -40dBm per tone, f1 = 1575MHz, f2 = 1576MHz.

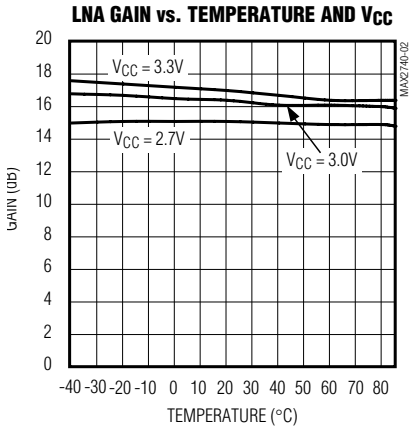
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

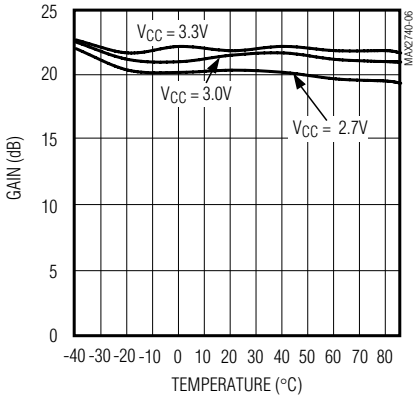
ICC vs. TEMPERATURE AND VCC



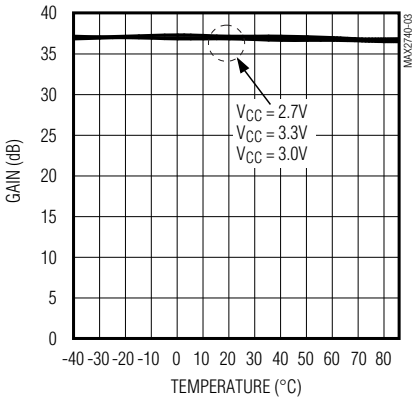
LNA GAIN vs. TEMPERATURE AND VCC



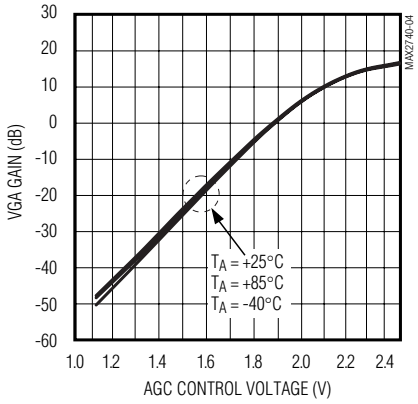
RF MIXER GAIN vs. TEMPERATURE AND VCC



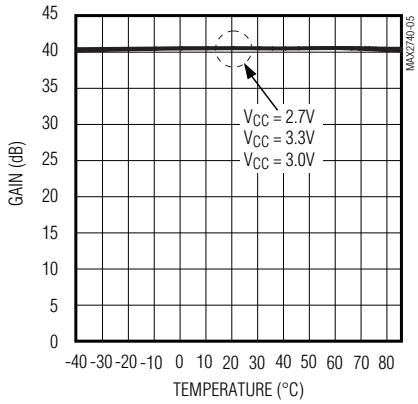
IF MIXER GAIN vs. TEMPERATURE AND VCC



VGA GAIN vs. VGC AND TEMPERATURE AT VCC = 3.0V



FGA GAIN vs. TEMPERATURE AND VCC



Pin Description

PIN	NAME	FUNCTION
1, 2, 4, 5, 6, 10, 11, 14, 15, 21, 22, 23, 26, 29, 32, 37, 41, 42, 47, paddle	GND	Ground. Connect pin to ground.
3	LNA_IN	Input of LNA Circuit. Matching network and blocking capacitor required.
7	RFMIX_IN-	Input to unused side of a differential pair that forms the RF section of a Gilbert cell mixer. This pin should be AC-grounded through 100pF.
8	GC	DC Control Voltage for Setting Gain Level of VGA. High input impedance. Voltage range of 0.5V to 2.5V.
9	VCC_ANA	Supply Voltage Pin for Analog Circuits. This pin requires external decoupling of typically 0.01µF.
12	VCC_VCO	Supply Voltage Pin for VCO Circuit. This pin requires external decoupling of typically 1000pF.
13	TANK	VCO Resonator Pin. A resonator is required at this pin.
16	VCC_DIG	Supply Voltage Pin for Digital Section of the IC. This pin requires external decoupling of typically 0.01µF.
17	DOWN	Down Output from the Phase-Frequency Detector. This pulses high whenever the phase of the VCO leads the phase of the reference.
18	UP	Up Output from the Phase-Frequency Detector. This pulses high whenever the phase of the VCO lags the phase of the reference.
19	GLS_OUT	Output of Buffer that Provides a 90MHz Clock Signal. Requires external blocking capacitor.
20	REF_IN	Reference Input for Synthesizer
24	FGA_OUT-	FGA Inverted Output. Blocking capacitor required.
25	FGA_OUT+	FGA Noninverted Output. Blocking capacitor required.
27	FGA_IN-	FGA Inverted Input. Blocking capacitor required.
28	FGA_IN+	FGA Noninverted Input. Blocking capacitor required.
30	VGA_OUT-	VGA Inverted Output. Blocking capacitor required.
31	VGA_OUT+	VGA Noninverted Output. Blocking capacitor required.
33	VGA_IN-	VGA Inverted Input. Blocking capacitor required.
34	VGA_IN+	VGA Noninverted Input. Blocking capacitor required.
35	IFMIX_OUT-	IF Mixer Inverted Output. Blocking capacitor required.
36	IFMIX_OUT+	IF Mixer Noninverted Output. Blocking capacitor required.
38	IFMIX_IN-	IF Mixer Inverted Input. Blocking capacitor required.
39	IFMIX_IN+	IF Mixer Noninverted Input. Blocking capacitor required.
40	VCC_IFMIX	Supply Voltage Pin for IF Downconverter. This pin requires external decoupling of typically 1000pF.

Pin Description (continued)

PIN	NAME	FUNCTION
43	RFMIX_OUT-	RF Mixer Inverted Input (same as *RFMIX_OUT+*)
44	RFMIX_OUT+	Open Emitter Output of the RF Downconverter. This pin requires an external pull-down resistor of 1.2kΩ to establish the correct on-chip bias conditions. Requires a blocking capacitor.
45	VCC_RFMIX	Supply Voltage Pin for RF Downconverter. This pin requires external decoupling of typically 100pF.
46	RFMIX_IN	Input to RF Mixer. Requires a blocking capacitor that may be used as part of the match network.
48	LNA_OUT	LNA Output. Requires a pull-up inductor and a blocking capacitor. These may be configured as the matching network.

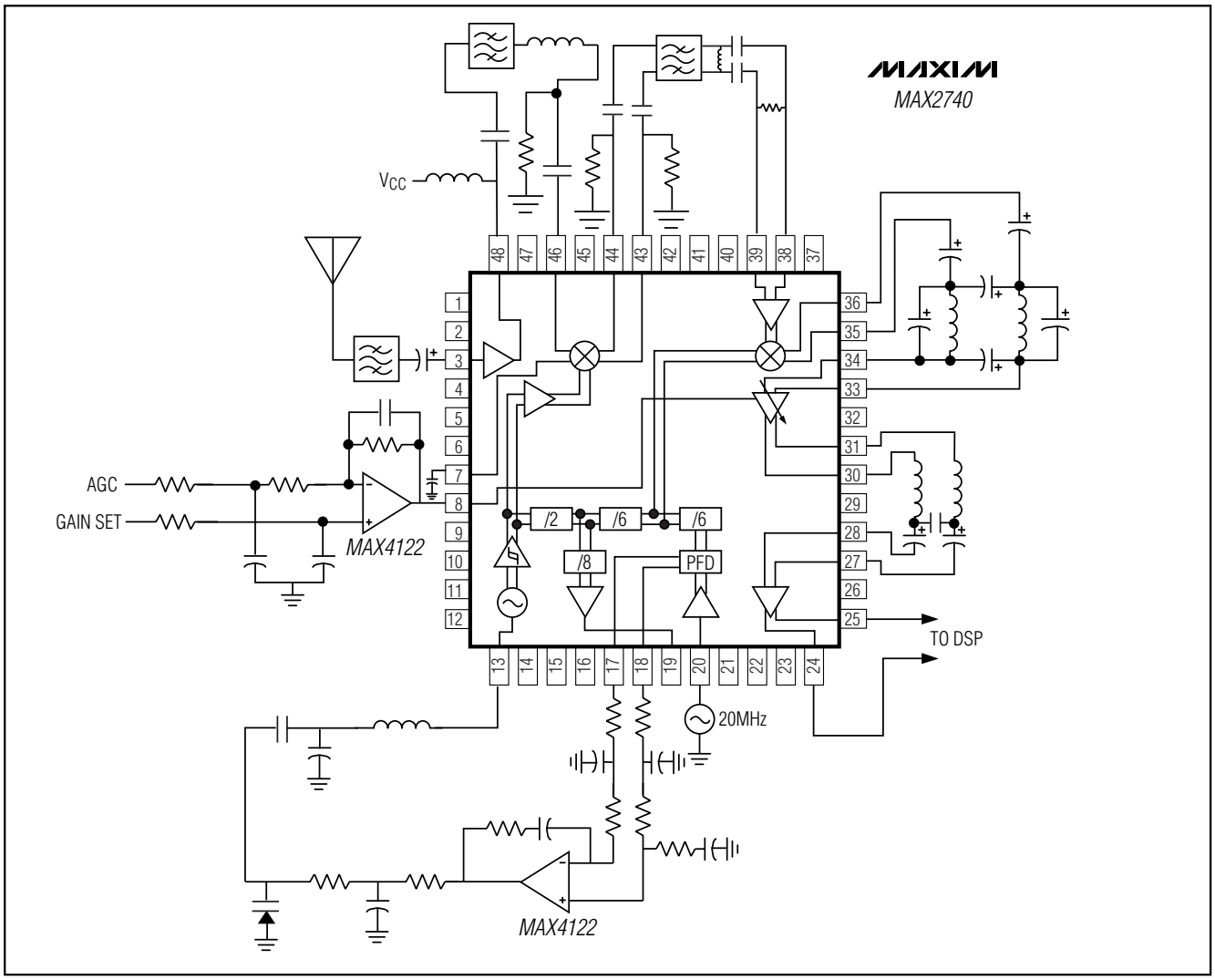


Figure 1. Typical Application Circuit

Integrated GPS Receiver and Synthesizer

Applications Information

Figure 1 shows a typical application diagram in which the MAX2740 should be used. The RF front end consists of the antenna interface, MAX2740, two control loops (one for the AGC, the other for the synthesizer), and appropriate external components, including filters for image rejection and channel selectivity, operational amplifiers for the control loops, and resonator and tuning network for the VCO.

Only the antenna input, an external 20MHz frequency reference, and an AGC input from the accompanying DSP are required. A differential output is provided from the MAX2740, which can be applied either to the external analog-to-digital conversion circuitry or directly to the companion DSP.

Low-Noise Amplifier

This subcircuit requires input and output matching. The input match is typically a series capacitor, and the output is typically a shunt inductor to V_{CC} and a series capacitor.

RF Mixer

The RF input is matched externally. The match consists of a series inductor and shunt capacitor. The source impedance for this circuit is the single-ended, 50Ω RF SAW used as an image reject filter. A second RF input is brought out to a separate pin for AC grounding. This ensures low ground impedance over a wide band and minimizes amplification of any noise at the IF frequency generated within the mixer structure.

The IF output is delivered through low-output-impedance emitter followers and is suitable for directly driving a 135MHz IF SAW with a typical impedance of 400Ω. The deliberate mismatch keeps the group delay distortion of the SAW within an acceptable level.

IF Mixer

The IF downconverter receives the differential 1st IF of 135.42MHz from the SAW and delivers a differential 2nd IF signal at 15.42MHz. The circuit has been optimized to deliver a high level of conversion gain with adequate IIP3 and noise figure. The circuit is terminated on the input with a differential 100Ω to establish the correct embedding impedance for the IF SAW. The emitter follower outputs drive directly into a high-impedance, differential, three-pole lowpass discrete lumped element filter.

Variable-Gain Amplifier

This circuit compensates for receiver gain variation and unknown antenna cable losses. Under these conditions, the receiver will exhibit minimum implementation loss. The circuit has a useful gain control range of greater than 50dB, with a maximum gain level of 16dB.

Fixed-Gain Amplifier

This circuit has been designed to deliver 40dB of differential gain at the 2nd IF frequency of 15.42MHz. The differential inputs are received from the VGA outputs through a balanced lowpass filter circuit. The circuit's differential output is designed to drive a digitizer with a typical load impedance of 4kΩ differential.

Voltage-Controlled Oscillator

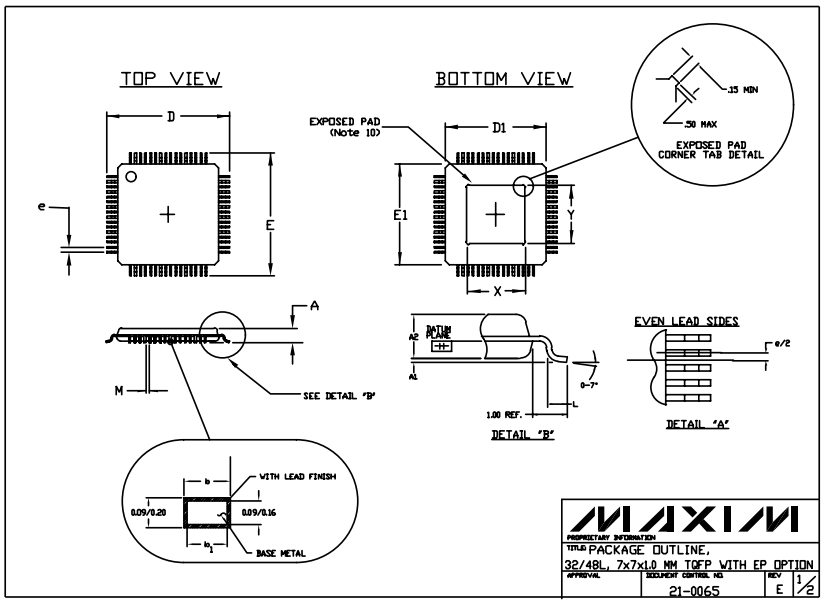
The core of the L-band VCO is based on a common-collector Colpitts topology. This circuit has been optimized for low thermal noise and high signal swing without asymmetrical clipping. The circuit is designed for use with a lumped inductor for low-cost applications. The self-resonance should be above 1440MHz so that parallel varactor tuning and the VCO internal capacitance produces resonance at 1440MHz.

Synthesizer

The digital prescaler accepts the output from the oscillator's differential digital buffer and divides the frequency from 1.44GHz to 120MHz for the 2nd LO, 20MHz for the phase-frequency detector, and 90MHz for the GLONASS reference output. Divider blocks are arranged to ensure that the 2nd LO drive has minimum duty cycle distortion. A simple output buffer is used to deliver the GLONASS reference signal to a typical external load impedance of 500Ω.

The phase-frequency detector is a classical dual flip-flop with ANDed feedback to a reset function. UP and DOWN outputs are provided through emitter follower buffers. These outputs deliver pulse-width-modulated signals that in phase-acquisition mode give a phase detector range of ±2π. With the PLL not in lock, either the UP or DOWN output will be active and drive the VCO frequency toward the reference frequency. The phase detector outputs feed directly into an active, lead-lag differential loop filter.

Package Information



NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~~	~~	1.20	~~	~~	1.20
A1	0.05	0.10	0.15	0.05	0.10	0.15
A2	0.95	1.00	1.05	0.95	1.00	1.05
D	9.00 BSC.			9.00 BSC.		
D1	7.00 BSC.			7.00 BSC.		
E	9.00 BSC.			9.00 BSC.		
E1	7.00 BSC.			7.00 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75
N	0.15	~~	~~	0.14	~~	~~
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,
32/48L, 7x7x1.0 MM TQFP WITH EP OPTION
APPROVAL
DOCUMENT CONTROL NO.
21-0065
REV
E
2/2

NOTES

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